ncm corporation

NCM 7000-SERIES Silicon Gate CMOS Master Arrays

FEATURES

- High Speed Iso-planar Silicon Gate Technology
- Metal Mask Programmable
- 3–12 Volts Power Supply Range
- TTL/CMOS/LTTL/STTL and LSTTL I/O Compatibility
- All Pads Configured as Either Inputs, Outputs, I/O's or Supplies
- On-chip Pull-ups and Pull-downs
- Commercial, Industrial and Military Applications
- Computer Aided Design (CAD) Adaptability
- Low Cost, Fast Turn-around
- Gate Mask Option for Higher Speed Applications
- On-chip Bipolar Transistors for Interface Drive
- Level Shift Capability

GENERAL DESCRIPTION

The NCM 7000-Series of Silicon-Gate CMOS Master Arrays is a low cost, versatile and dedicated family of gate arrays which offers a wide range of applications with complexity up to 1600 equivalent gates, premanufactured on chips which have up to 88 pads.

This family of master arrays is manufactured using a well-proven, iso-planar, silicon-gate, CMOS-process technology. It features the inherent advantages of low power consumption, high speed, wide operating voltage range and extremely high noise immunity.

The Master Arrays concept is an efficient approach to semi-custom implementation and manufacture of monolithic integrated circuits, especially for low volume. All components, tailored to meet practically a majority of circuit applications, are arranged in specific patterns and pre-manufactured, ready to be interconnected into a custom integrated circuit. Each wafer contains hundreds of such arrangements with a metal layer pre-deposited on its surface. Circuit customization can be achieved by means of a simple metal mask, programmed to a specific requirement. Since only one mask is needed to tailor the product, this circuit development approach is extremely efficient. A custom circuit can be developed in a few weeks at a very low development cost.

The NCM 7000-Series of Iso-planar 5 μm Silicon-Gate CMOS Master Arrays combines all the advantages of the cell placing technique, which NCM has used successfully in its full-custom design programs, and the versatility of a master-slice approach. Since there is often the need of a higher speed version once a circuit is customized, provision is made to provide a special 3 μm gate mask for the same metal interconnections. Practically all pads can be used either as an input, output, I/O or even power supply with appropriate connection of the components of the I/O cell. The input pad can be CMOS TTL compatible or level-shifted to accommodate specific requirements.

All input pads have protection against damages due to static discharge. This is achieved by utilizing the discrete P+/N– diode for clamping to V_{DD} thus providing a low impedance path for voltages higher than V_{DD} and the N+ underpath for clamping to V_{SS}, providing a similar low impedance path for voltages lower than V_{SS}. The extra guard-band also serves as a mechanism to help eliminate latch-up.

Each master arrays' I/O cell provides level shifting capabilities by making use of pull-ups or pull-downs of different resistance values and a discrete diode. The pull-up or pull-down networks can be used for a selected resistance value by connecting the gate of such a transistor to the appropriate power supply level. In addition, a number of bipolar transistors, intended for use as emitter follower in a high drive application, are fabricated on chip. There are also Zener diodes for applications which require usage of a voltage reference.

All underpaths are constructed using poly-silicon. These underpaths are arranged in both vertical and horizontal directions to allow for better usage, more efficient layout and higher packing density.

All cells including the basic gate and the I/O peripherals networks are designed to allow configuration of different functions, ranging from inverters, AND/NOR, OR/NAND, EX-OR, EX-NOR to different types of flip-flops with set, reset, and Q-to-D capabilities. Similarly, combinations of those are possible to provide more complex macro structures, including JK flip-flops, counters, shift-registers, comparators, adders, etc.

NCM 7000 SERIES FAMILY OUTLINE

Part No.	No. of Gates	No. of Pads	Hi-Z Cells	Bipolar Transistors	Zener	Die Size (mils)
NCM70013Z	780	62	62	2	1	191 x 206
NCM70015Z	780	62	62	2	1	191 x 206
NCM70023Z	1600	88	86	2	2	259 x 278
NCM70025Z	1600	88	86	2	2	259 x 278

Gate is defined as a structure of four or six complementary MOS transistors.

MAXIMUM RECOMMENDED OPERATING CONDITIONS

Parameters	Ratings Limits	Recommended Limits	Units
DC supply voltage	–0.5 to 12.0	3.0 to 10.0	Volts
Voltage to any pin	–0.5 to V_{DD} + 0.5		Volts
DC current to any input	±10		mA
Storage temperature	–65 to 150		°C
Maximum operating temperature		–55 to 125	°C

DESIGN PARAMETERS (@ 5.0V unless otherwise specified)

Components	Dimensions (μm)		Capacitance (pF)	
	Width	Length	Gate	Drain
N-channel array	46	5.0	0.09	0.02
P-channel array	46	5.0	0.08	0.02
P/N "LS" output cell	265/306	5.0	0.46/0.6	0.12/0.13
P/N 10kΩ pull-up/down, top/bottom	12/6	5.0	0.02/0.012	0.005/0.002
N-channel pull-up/down	8	85.0	0.267	0.06
P/N "T" output cell	527/862	5.0	0.92/1.69	0.23/0.37
P/N "Buffer" cell	215/162	5.0	0.37/0.32	0.09/0.07
P/N pull-up/down, on side	8	128/74	0.35/0.23	0.09/0.05
Level shifting, top/bottom	32	5.0	0.06	0.014
Level shifting, side	20	5.0	0.04	0.009
P/N 100 kΩ pull-up/down, corner	6	24/24	0.05/0.06	0.013
P/N 1 kΩ pull-up/down, corner	5	262/250	0.46/0.49	0.11/0.11

Bipolar Transistor: h_{FE} @ 1mA = 100; V_{CEST} = 0.5V, V_{EB} = 25V, Zener diode voltage 6.8-7.2 Volts

DC/AC CHARACTERISTICS (at 25°C and nominal supply voltage)

Parameter	Symbol	Test Condition	V_{DD} = 5.0V			V_{DD} = 10V			Unit
			Min	Typ	Max	Min	Typ	Max	
Low output voltage	V_{OL}	I_{OL} = 1.6mA		0.22	0.4		0.11	0.35	Volts
High output voltage	V_{OH}	I_{OH} = 0.4mA	4.65	4.95		9.25	9.95		Volts
Low input voltage	V_{IL}				1.5			3.0	Volts
High input voltage	V_{IH}		3.5			7.0			Volts
Input leakage current	I_{IN}				1.0			1.0	μA
Quiescent power consumption	I_{DD}			1			4		nW/gate
Logic cell propagation delay time (NCM 70015Z)	t_{pd}	@1pF							
Inverter				5			4		nsec
2-input NOR				7			5		nsec
2-input NAND				7			5		nsec
3-input NOR				10			8		nsec
3-input NAND				9			7		nsec
4-input NOR				18			14		nsec
4-input NAND				16			12		nsec
FF Toggle Frequency	f_T	ripple counter		20			29		MHz

Note: delay times of NCM 70013Z are approximately 35% less

PROCESSING PARAMETERS

Parameter	Min.	Max.	Unit	Conditions
Device threshold	0.6	1.4	Volts	@ 1.0 μA
Field threshold voltage	15.0	—	Volts	@ 1.0 μA
Breakdown voltage P+/N−	25.0	—	Volts	@ 1.0 μA
Breakdown voltage N+/P−	25.0	—	Volts	@ 1.0 μA
N+ thin oxide capacitance	0.30	0.33	pF/mil²	
P+ thin oxide capacitance	0.36	0.38	pF/mil²	
P+ resistivity	40	100	Ω/sq	
N+ resistivity	20	50	Ω/sq	
P− resistivity	2.0	4.0	kΩ/sq	

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