NCV7380

Advance Information

LIN Transceiver

The NCV7380 is a physical layer device for a single wire data link capable of operating in applications where high data rate is not required and a lower data rate can achieve cost reductions in both the physical media components and in the microprocessor which uses the network. The NCV7380 is designed in accordance to the physical layer definition of the LIN (Local Interconnect Network) Protocol Specification, Rev. 1.3. The IC furthermore can be used in ISO9141 systems.

Because of the very low current consumption of the NCV7380 in recessive state, it's suitable for ECU applications with low standby current requirements, whereby no sleep/wake−up control from the microprocessor is necessary.

Features

- Operating Voltage V_S = 6.0 to 18 V
- Low Current Consumption of Typ. 24 μA
- LIN−Bus Transceiver:
  - Slew Rate Control for Good EMC Behavior
  - Fully Integrated Receiver Filter
  - BUS Input Voltage −27 V to 40 V
  - Integrated Termination Resistor for LIN Slave Nodes (30 kΩ)
  - Baud Rate up to 20 kBaud
  - Compatible to LIN Specification 1.3
- Compatible to ISO9141 Functions
- High EMI Immunity
- Bus Terminals Protect Against Short−Circuits and Transients in the Automotive Environment
- Thermal Overload Protection
- High Signal Symmetry for use in RC–Based Slave Nodes up to 2% Clock Tolerance when Compared to the Master Node
- ±4.0 kV ESD Protection on all Pins
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control

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SO−8
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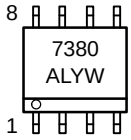
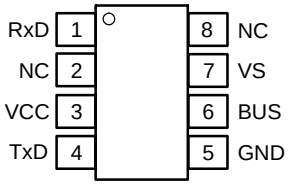
CASE 751

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



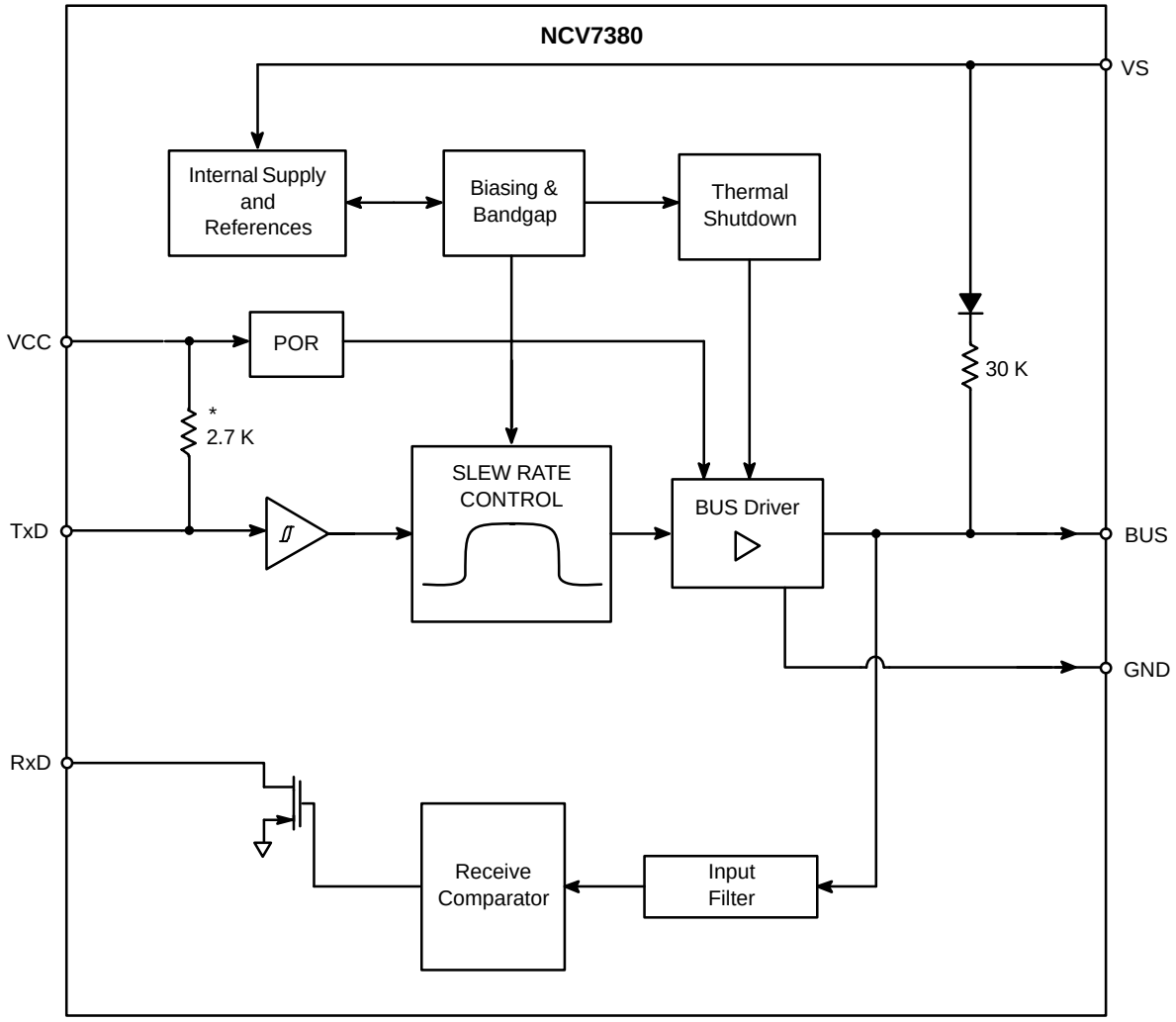
(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCV7380D	SO−8	95 Units/Rail
NCV7380DR2	SO−8	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



*Shown as a resistor for simplicity. Actual circuitry consists of a current source.

Figure 1. Block Diagram

PACKAGE PIN DESCRIPTION

Pin	Symbol	Description
1	RXD	Receive data from BUS to core, LOW in dominant state.
2	NC	No connection.
3	VCC	5.0 V supply input.
4	TXD	Transmit data from core to BUS, LOW in dominant state.
5	GND	Ground
6	BUS	LIN bus pin, LOW in dominant state.
7	VS	Battery input voltage.
8	NC	No connection.

Electrical Specification

All voltages are referenced to ground (GND). Positive currents flow into the IC.

The maximum ratings (in accordance with IEC 134) given in the table below are limiting values that do not lead to a permanent damage of the device but exceeding any of these limits may do so. Long term exposure to limiting values may effect the reliability of the device.

OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Battery Supply Voltage (Note 1)	V_S	6.0	18	V
Supply Voltage	V_{CC}	4.5	5.5	V
Operating Ambient Temperature	T_A	−40	+125	°C

MAXIMUM RATINGS

Rating	Symbol	Condition	Min	Max	Unit
Battery Supply Voltage	V_S	t < 1 min	−0.3	30	V
		Load Dump, t < 500 ms		40	
Supply Voltage	V_{CC}	−	−0.3	+7.0	V
Transient Supply Voltage	$V_{S.tr1}$	ISO 7637/1 Pulse 1 (Note 2)	−150	−	V
Transient Supply Voltage	$V_{S..tr2}$	ISO 7637/1 Pulses 2 (Note 2)	−	100	V
Transient Supply Voltage	$V_{S..tr3}$	ISO 7637/1 Pulses 3A, 3B	−150	150	V
BUS Voltage	V_{BUS}	t < 500 ms , Vs = 18 V	−27	40	V
		t < 500 ms ,Vs = 0 V	−40		
Transient Bus Voltage	$V_{BUS..tr1}$	ISO 7637/1 Pulse 1 (Note 3)	−150	−	V
Transient Bus Voltage	$V_{BUS.tr2}$	ISO 7637/1 Pulses 2 (Note 3)	−	100	V
Transient Bus Voltage	$V_{BUS.tr3}$	ISO 7637/1 Pulses 3A, 3B (Note 3)	−150	150	V
DC Voltage on Pins TxD, RxD	V_{DC}	−	−0.3	7.0	V
ESD Capability of Any Pin	ESD_{HB}	Human body model, equivalent to discharge 100 pF with 1.5 kΩ	−4.0	4.0	kV
Maximum Latch−Up Free Current at Any Pin	I_{LATCH}	−	−500	500	mA
Maximum Power Dissipation	P_{tot}	At T_A = 125°C	−	197	mW
Thermal Impedance	θ_{JA}	In Free Air	−	152	°C/W
Storage Temperature	T_{stg}	−	−55	+150	°C
Junction Temperature	T_J	−	−40	+150	°C
Lead Temperature Soldering Reflow: (SMD styles only)	T_{sld}	60 second maximum above 183°C −5°C/+0°C allowable conditions	−	240 peak	°C

1. V_S is the IC supply voltage including voltage drop of reverse battery protection diode, V_{DROP} = 0.4 to 1.0 V, V_{BAT_ECU} voltage range is 7.0 to 18 V.
2. ISO 7637 test pulses are applied to V_S via a reverse polarity diode and > 2.0 μF blocking capacitor.
3. ISO 7637 test pulses are applied to BUS via a coupling capacitance of 1.0 nF.

ELECTRICAL CHARACTERISTICS (V_S = 6.0 to 18 V, V_{CC} = 4.5 to 5.5 V and T_A = −40 to 125°C unless otherwise noted.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
GENERAL						
V_{CC} Undervoltage Lockout	V_{CC_UV}	EN = H, TxD = L	2.75	−	4.3	V
Supply Current, Dominant	I_{Sd}	V_S = 18 V, V_{CC} = 5.5 V, TxD = L	−	−	3.0	mA
Supply Current, Dominant	I_{CCd}	V_S = 18 V, V_{CC} = 5.5 V, TxD = L	−	−	1.0	mA
Supply Current, Recessive	I_{Sr}	V_S = 18 V, V_{CC} = 5.5 V, TxD = Open	−	10	20	μA
Supply Current, Recessive	I_{CCr}	V_S = 18 V, V_{CC} = 5.5 V, TxD = Open	−	14	30	μA
Supply Current, Recessive	$I_{Sr} + I_{CCr}$	V_S = 12 V, V_{CC} = 5.0 V, TxD = Open, T_A = 25°	−	24	−	μA
Thermal Shutdown	T_{sd} (Note 4)	−	155	−	180	°C
Thermal Recovery	T_{hys} (Note 4)	−	130	140	150	°C
BUS − Transmit						
Short Circuit Bus Current	I_{BUS_LIM}	$V_{BUS} = V_S$, Driver On	−	120	200	mA
Pull Up Current Bus	I_{BUS_PU}	V_{BUS} = 0, V_S = 12 V, Driver Off	−1.0	−	−	mA
Bus Reverse Current, Recessive	$I_{BUS\_PAS\_rec}$	$V_{BUS} > V_S$, 8.0 V < V_{BUS} < 18 V 8.0 V < V_S < 18 V, Driver Off	−	−	20	μA
Bus Reverse Current Loss of Battery	I_{BUS}	V_S = 0 V, 0 V < V_{BUS} < 18 V	−	−	100	μA
Bus Current During Loss of Ground	$I_{BUS\_NO\_GND}$	V_S = 12 V, 0 < V_{BUS} < 18 V	−1.0	−	1.0	mA
Transmitter Dominant Voltage	$V_{BUSdom\_DRV\_1}$	Load = 40 mA	−	−	1.2	V
Transmitter Dominant Voltage	$V_{BUSdom\_DRV\_2}$	V_S = 6.0 V, Load = 1000 Ω	0.6	−	−	V
Transmitter Dominant Voltage	$V_{BUSdom\_DRV\_3}$	V_S = 18 V, Load = 1000 Ω	0.8	−	−	V
BUS − Receive						
Receiver Dominant Voltage	V_{BUSdom}	−	0.4 *V_S	−	−	V
Receiver Recessive Voltage	V_{BUSrec}	−	−	−	0.6 *V_S	V
Center Point of Receiver Threshold	V_{BUS_CNT}	$V_{BUS\_CNT} = (V_{BUSdom} + V_{BUSrec})/2$	0.487 *V_S	0.5 *V_S	0.512 *V_S	V
Receiver Hysteresis	V_{HYS}	$V_{BUS\_CNTt} = (V_{BUSrec} - V_{BUSdom})$	−	0.175 *V_S	0.187 *V_S	V
TXD						
High Level Input Voltage	V_{ih}	Rising Edge	−	−	0.7*V_{CC}	V
Low Level Input Voltage	V_{il}	Falling Edge	0.3*V_{CC}	−	−	V
TxD Pull Up Current, High Level	I_{IH_TXD}	V_{TxD} = 4.0 V	−125	−50	−25	μA
TxD Pull Up Current, Low Level	I_{IL_TXD}	V_{TxD} = 1.0 V	−500	−250	−100	μA
RXD						
Low Level Output Voltage	V_{ol_rxd}	I_{RxD} = 2.0 mA	−	−	0.9	V
Leakage Current	V_{leak_rxd}	V_{RxD} = 5.5 V, Recessive	−1.0	−	1.0	μA

4. No production test, guaranteed by design and qualification.

ELECTRICAL CHARACTERISTICS (continued) (V_S = 6.0 to 18 V, V_{CC} = 4.5 to 5.5 V and T_A = −40 to 125°C unless otherwise noted.)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
AC CHARACTERISTICS						
Propagation Delay Transmitter (Notes 5 and 7)	t_{trans_pd}	Bus Loads: 1.0 KΩ/1.0 nF, 660 Ω/6.8 nF, 500 Ω/10 nF	−	−	5.0	μs
Propagation Delay Transmitter Symmetry (Note 7)	t_{trans_sym}	Calculate $t_{trans\_pdf} - t_{trans\_pdr}$	−2.0	−	2.0	μs
Propagation Delay Receiver (Notes 5 and 7)	t_{rec_pdf}	C_{RxD} = 20 pF	−	−	6.0	μs
Propagation Delay Receiver Symmetry (Note 7)	t_{rec_sym}	Calculate $t_{trans\_pdf} - t_{trans\_pdr}$	−1.5	−	1.5	μs
Slew Rate Falling Edge (Note 6)	t_{SRF}	Bus Load 1.0 KΩ/1.0 nF	−3.0	−2.0	−1.0	V/μs
Slew Rate Rising Edge (Note 6)	t_{SRR}	Bus Load 1.0 KΩ/1.0 nF	1.0	2.0	3.0	V/μs
Slope Time, Transition from Recessive to Dominant, Low Battery (Note 8)	t_{sdom_LB}	V_S = 6.0 V, Bus Loads: 1.0 KΩ/1.0 nF, 660 Ω/6.8 nF, 500 Ω/10 nF	−	−	5.4	μs
Slope Time, Transition from Dominant to Recessive, Low Battery (Note 8)	t_{srec_LB}	V_S = 6.0 V, Bus Load 500 Ω/10 nF	−	−	7.2	μs
Slope Symmetry, Low Battery	T_{ssym_LB}	Calculate $t_{sdom} - t_{srec}$	−7.0	−	+1.0	μs
Slope Time, Transition from Recessive to Dominant, High Battery (Note 8)	t_{sdom_HB}	V_S = 18 V, Bus Loads: 1.0 KΩ/1.0 nF, 660 Ω/6.8 nF, 500 Ω/10 nF	−	−	17.2	μs
Slope Time, Transition from Dominant to Recessive, High Battery (Note 8)	t_{srec_HB}	V_S = 18 V, Bus Loads: 1.0 KΩ/1.0 nF, 660 Ω/6.8 nF, 500 Ω/10 nF	−	−	17.2	μs
Slope Symmetry, High Battery	t_{ssym_HB}	Calculate $t_{sdom} - t_{srec}$	−5.0	−	+5.0	μs
Receiver Debounce Time (Notes 5 and 9)	t_{rec_deb}	BUS Rising and Falling Edge	1.5	−	4.0	μs

5. Propagation delays are not relevant for LIN protocol transmission, value only information parameter.
6. No production test, guaranteed by design and qualification.
7. See Figure 2 − Input/Output Timing.
8. See Figure 7 − Slope Time Calculation.
9. See Figure 3 − Receiver Debouncing.

TIMING DIAGRAMS

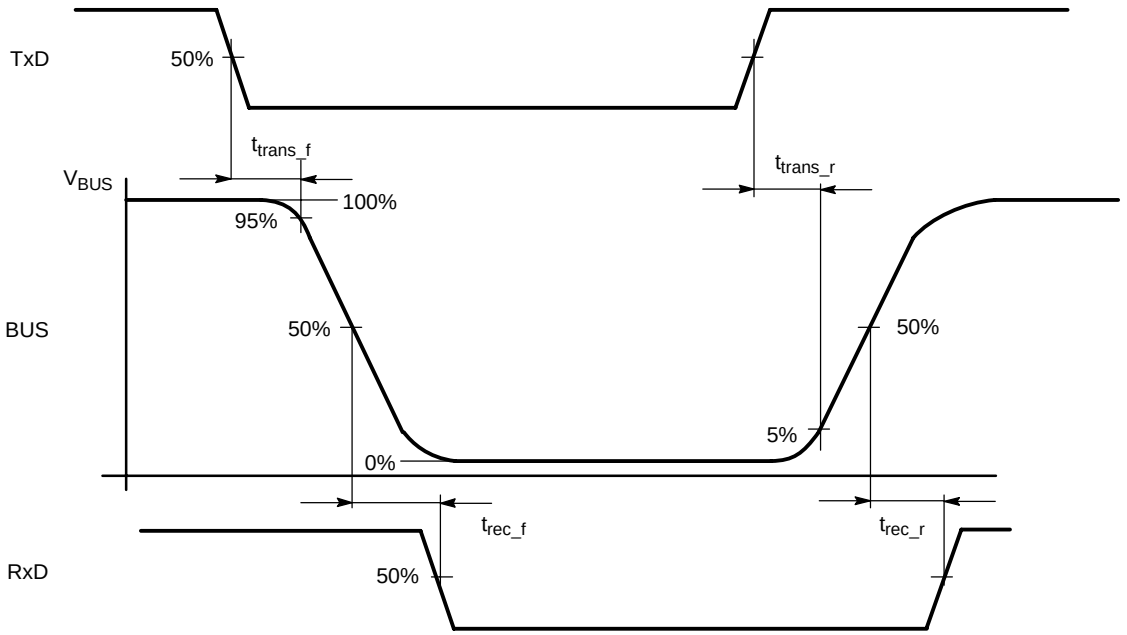


Figure 2. Input/Output Timing

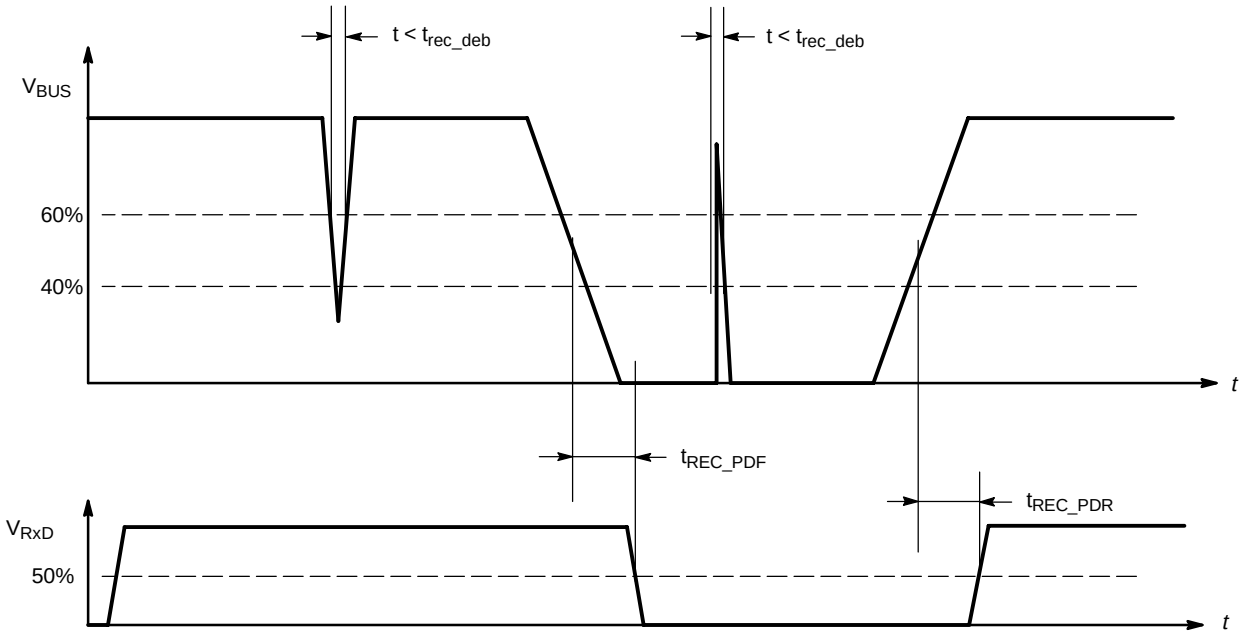


Figure 3. Receiver Debouncing

TEST CIRCUITS FOR DYNAMIC AND STATIC CHARACTERISTICS

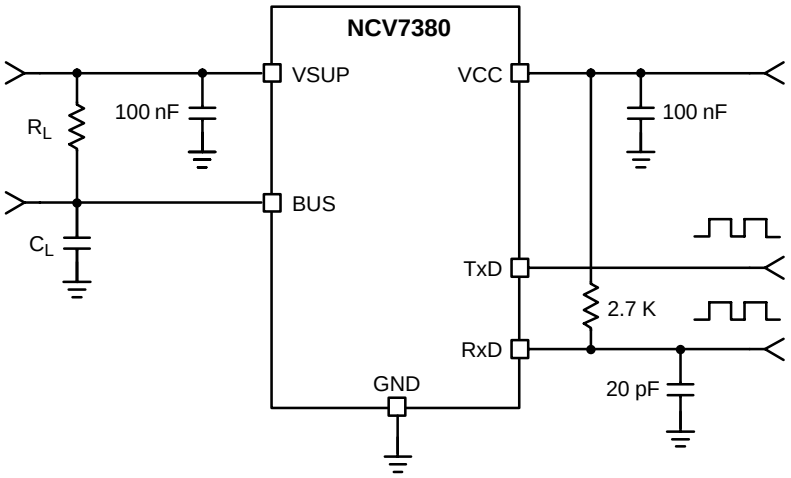


Figure 4. Test Circuit for Dynamic Characteristics

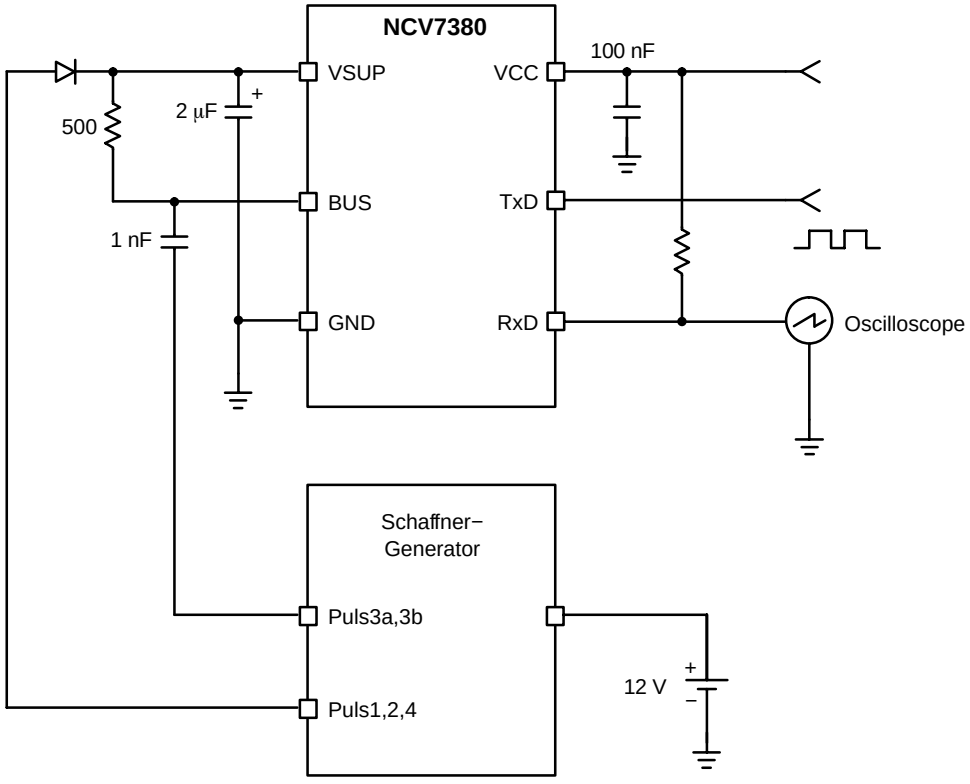


Figure 5. Test Circuit for Automotive Transients

Functional Description

Initialization

After *power on*, the chip automatically enters the recessive state (TxD = Open). Both V_{CC} and V_S must be present.

Operating Modes

All operation modes will be handled from the NCV7380 automatically.

Normal Mode

After power on, the IC switches automatically to normal mode. Bus communication is possible. If there is no communication on the bus line the power consumption of the IC is very low and does not require microprocessor control.

Thermal Shutdown Mode

If the junction temperature T_J is higher than 155°C, the NCV7380 could be switched into the thermal shutdown mode (bus driver will be switched off, receiver is on).

If T_J falls below the thermal shutdown temperature (typ. 140°C) the NCV7380 will be switched to the normal mode.

LIN BUS Transceiver

The transceiver consists of a bus−driver (1.2 V @ 40 mA) with slew rate control and current limit, and a receiver with a high voltage comparator with filter circuitry.

BUS Input/Output

The recessive BUS level is generated from the integrated 30 k pull up resistor in series with a diode. The diode prevents reverse current on V_{BUS} when $V_{BUS} > V_S$.

No additional termination resistor is necessary to use the NCV7380 on LIN slave nodes. If this IC is used for LIN master nodes, it is necessary to terminate the bus with an external 1.0 kΩ resistor in series with a diode to VBAT (Figure 8).

TxD Input

During transmission the signal on TxD will be transferred to the BUS driver for generating a BUS signal. To minimize the electromagnetic emission of the bus line, the BUS driver has integrated slew rate control and wave shaping.

Transmitting will be interrupted if thermal shutdown is active.

The CMOS compatible input TxD directly controls the BUS level:

TxD = low → BUS = low (dominant level)

TxD = high → BUS = high (recessive level)

The TxD pin has an internal pull up resistor connected to V_{CC}. This secures that an open TxD pin generates a recessive BUS level.

RxD Output

The signal on the BUS pin will be transferred continuously to the RxD pin. Short spikes on the bus signal are filtered with internal circuitry (Figure 3 and Figure 6).

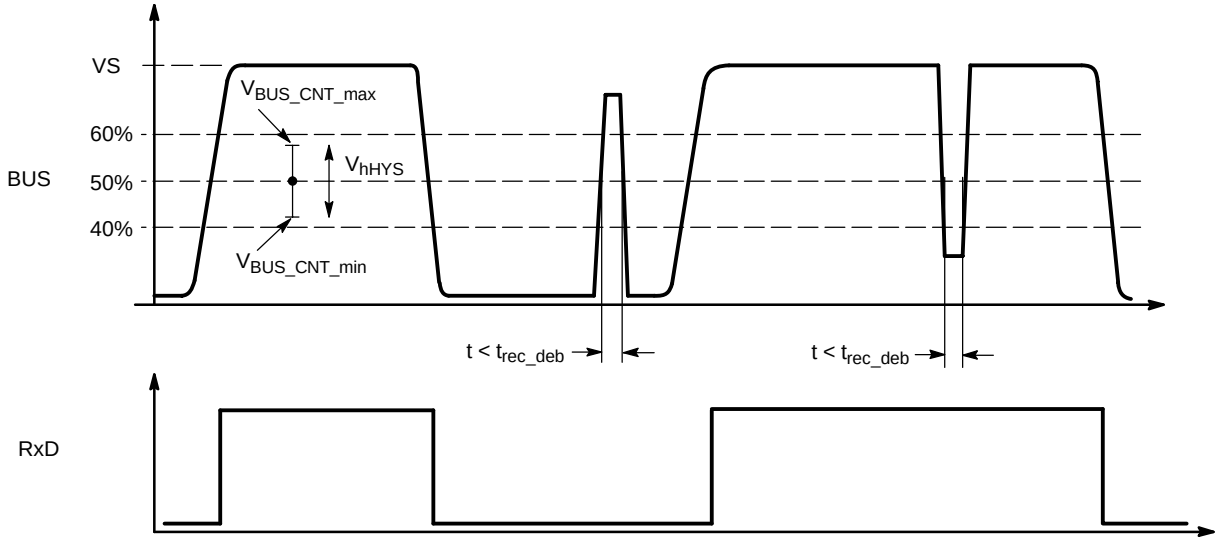


Figure 6. Receive Impulse Diagram

The receive threshold values $V_{BUS\_CNT\_max}$ and $V_{BUS\_CNT\_min}$ are symmetrical to $0.5*V_S$ with a hysteresis of $0.175*V_S$ (typ). The LIN specific receive threshold is between $0.4*V_S$ and $0.6*V_S$.

The received BUS signal will be output to the RxD pin:

$BUS < V_{BUS\_CNT} - 0.5 * V_{HYS}$
$\rightarrow$ RxD = low (BUS dominant)

$BUS > V_{BUS\_CNT} + 0.5 * V_{HYS}$
$\rightarrow$ RxD = high, floating (BUS recessive)

RxD is a buffered open drain output with a typical load of:

Resistance: 2.7 kΩ
Capacitance: < 25 pF

Data Rate

The NCV7380 is a *constant slew rate* transceiver. The bus driver operates with a fixed slew rate range of 1.0 V/μs $\leq \Delta V/\Delta T \leq$ 3.0 V/μs. This principle provides very good symmetry of the slope times between recessive to dominant and dominant to recessive slopes within the LIN bus load range (C_{BUS}, R_{term}).

The NCV7380 guarantees data rates up to 20 kbit within the complete bus load range under worst case conditions. The constant slew rate principle holds appropriate voltage levels and can operate within the LIN Protocol Specification for RC oscillator systems with a matching tolerance up to 2%.

Operating Under Disturbance

Loss of Battery

If V_S and V_{CC} are disconnected from the battery, the bus pin is in high impedance state. There is no impact to the bus traffic.

Loss of Ground

In case of an interrupted ground connection from V_S and V_{CC}, there is no influence to the bus line.

Short Circuit BUS to Battery

The transmitter output current is limited to 200 mA (max) in case of short circuit to battery.

Short Circuit BUS to Ground

Negative voltages on the bus pin are limited to current through the internal 30 k resistor and series diode from V_S.

Thermal Overload

The NCV7380 is protected against thermal overloads. If the chip temperature exceeds the thermal shutdown threshold, the transmitter is switched off until thermal recovery. The receiver continues to work during thermal shutdown.

Undervoltage V_{CC}

The V_{CC} undervoltage lockout feature disables the transmitter until it is above the undervoltage lockout threshold to prevent undesirable bus traffic.

Application Hints

LIN System Parameter

Bus Loading Requirements

Parameter	Symbol	Min	Typ	Max	Unit
Operating Voltage Range	V_{BAT}	8.0	−	18	V
Voltage Drop of Reverse Protection Diode	V_{Drop_rev}	0.4	0.7	1.0	V
Voltage Drop at the Series Diode in Pull Up Path	$V_{SerDiode}$	0.4	0.7	1.0	V
Battery Shift Voltage	V_{Shift_BAT}	0	−	0.1	V_{BAT}
Ground Shift Voltage	V_{Shift_GND}	0	−	0.1	V_{BAT}
Master Termination Resistor	R_{master}	900	1000	1100	Ω
Slave Termination Resistor	R_{slave}	20	30	60	kΩ
Number of System Nodes	N	2	−	16	−
Total Length of Bus Line	LEN_{BUS}	−	−	40	m
Line Capacitance	C_{LINE}	−	100	150	pF/m
Capacitance of Master Node	C_{Master}	−	220	−	pF
Capacitance of Slave Node	C_{Slave}	−	220	250	pF
Total Capacitance of the Bus including Slave and Master Capacitance	C_{BUS}	0.47	4.0	10	nF
Network Total Resistance	$R_{Network}$	500	−	862	Ω
Time Constant of Overall System	τ	1.0	−	5.0	μs

Recommendations for System Design

The goal of the LIN physical layer standard is to have a universal definition of the LIN system for plug and play solutions in LIN networks up to 20 kbd bus speeds.

In case of small and medium LIN networks, it's recommended to adjust the total network capacitance to at least 4.0 nF for good EMC and EMI behavior. This can be done by setting only the master node capacitance. The slave node capacitance should have a unit load of typically 220 pF for good EMC/EMI behavior.

In large networks with long bus lines and the maximum number of nodes, some system parameters can exceed the defined limits and the LIN system designer must intervene.

The whole capacitance of a slave node is not only the unit load capacitor itself. Additionally, there is the capacitance of wires and connectors, and the internal capacitance of the LIN transmitter. This internal capacitance is strongly dependent on the technology of the IC manufacturer and should be in the range of 30 pF to 150 pF. If the bus lines have a total length of nearly 40m, the total bus capacitance can exceed the LIN system limit of 10 nF.

A second parameter of concern is the integrated slave termination resistor tolerance. If most of the slave nodes have a slave termination resistance at the allowed maximum of 60 kΩ, the total network resistance is more than 700 Ω. Even if the total network capacitance is below or equal to the maximum specified value of 10 nF, the network time constant is higher than 7.0 μs.

This problem can be solved only by adjusting the master termination resistor to the required maximum network time constant of 5.0 μs (max).

The LIN bus output driver of the NCV7380 provides a higher drive capability than necessary (40 mA @ 1.2 V) within the LIN standard (33.6 mA @ 1.2 V). With this driver stage the system designer can increase the maximum LIN networks with a total network capacitance of more than 10 nF. The total network resistance can be decreased to:

$$R_{tl\_min} = (V_{Bat\_max} - V_{BUSdom})/I_{BUS\_max}$$
$$= (18\ V - 1.2\ V)/40\ mA = 420\ \Omega$$

NOTE: *The NCV7380 meets the requirements for implementation in RC−based slave nodes. The LIN Protocol Specification requires the deviation of the slave node clock to the master node clock after synchronization must not differ by more than ±2%.*

Setting the network time constant is necessary in large networks (primarily resistance) and also in small networks (primarily capacitance).

MIN/MAX SLOPE TIME CALCULATION

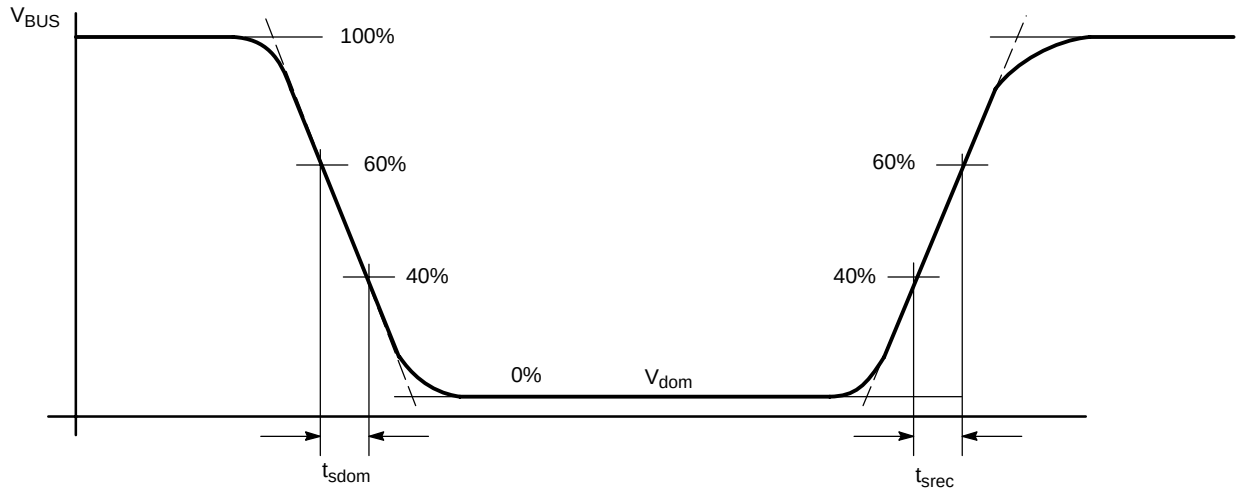


Figure 7. Slope Time Calculation

The slew rate of the bus voltage is measured between 40% and 60% of the output voltage swing (linear region). The output voltage swing is the difference between dominant and recessive bus voltage.

$$dV/dt = 0.2 * V_{swing}/(t_{40\%} - t_{60\%})$$

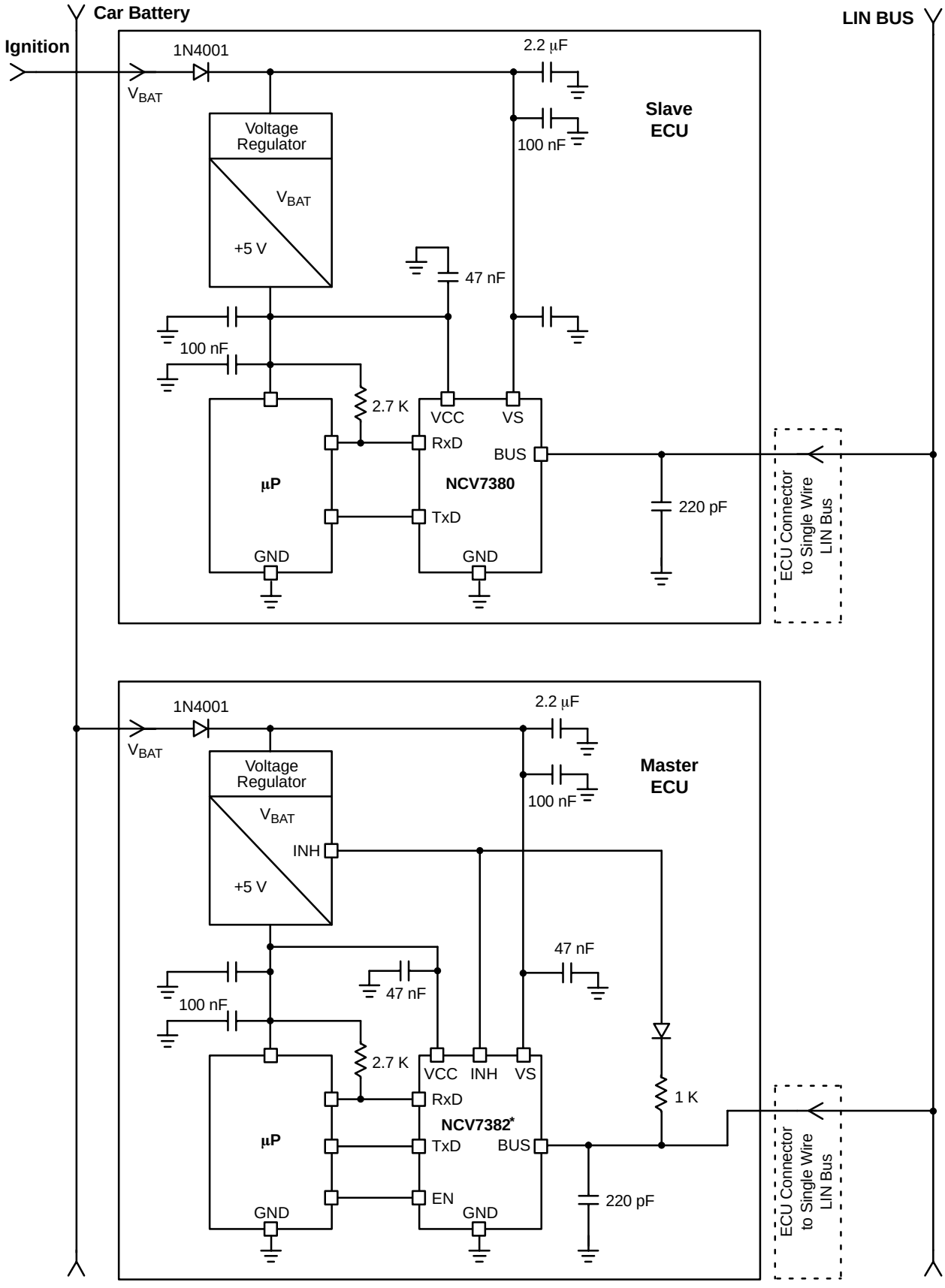
The slope time is the extension of the slew rate tangent until the upper and lower voltage swing limits:

$$t_{slope} = 5 * (t_{40\%} - t_{60\%})$$

The slope time of the recessive to dominant edge is directly determined by the slew rate control of the transmitter:

$$t_{slope} = V_{swing}/dV/dt$$

The dominant to recessive edge is influenced from the network time constant and the slew rate control, because it's a passive edge. In case of low battery voltages and high bus loads the rising edge is only determined by the network. If the rising edge slew rate exceeds the value of the dominant one, the slew rate control determines the rising edge.



*The NCV7382 is a pin compatible transceiver with INH control.

Figure 8. Application Circuitry

ESD/EMC Remarks

General Remarks

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

ESD Test

The NCV7380 is tested according to MIL883D (human body model).

EMC

The test on EMC impacts is done according to ISO 7637−1 for power supply pins and ISO 7637−3 for data and signal pins.

POWER SUPPLY PIN VS

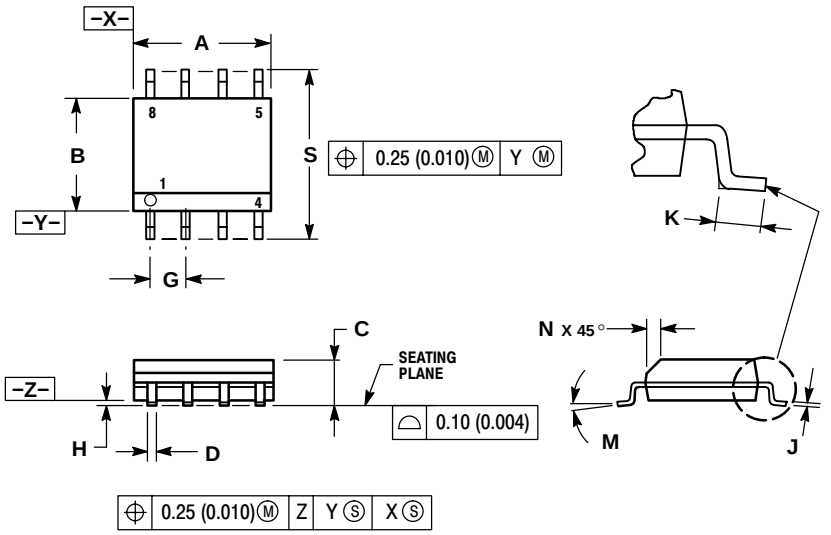
Test Pulse	Condition	Duration
1	t_1 = 5.0 s/U_S = −100 V/t_D = 2.0 ms	5000 Pulses
2	t_1 = 0.5 s/U_S = 100 V/t_D = 0.05 ms	5000 Pulses
3a/b	U_S = −150 V/U_S = 100 V Burst 100 ns/10 ms/90 ms Break	1 h
5	R_i = 0.5 Ω, t_D = 400 ms t_r = 0.1 ms/U_P + U_S = 40 V	10 Pulses Every 1 Min

DATA AND SIGNAL PINS BUS

Test Pulse	Condition	Duration
1	t_1 = 5.0 s/U_S = −100 V/t_D = 2.0 ms	1000 Pulses
2	t_1 = 0.5 s/U_S = 100 V/t_D = 0.05 ms	1000 Pulses
3a/b	U_S = −150 V/U_S = 100 V Burst 100 ns/10 ms/90 ms Break	1000 Burst

PACKAGE DIMENSIONS

SOIC−8 NB
D SUFFIX
CASE 751−07
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

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