Octal differential line receiver

NE5180/NE5181

DESCRIPTION

The NE5180 and NE5181 are octal line receivers designed to interface data terminal equipment with data communications equipment. These devices meet the requirements of EIA standards RS-232C, RS-423A, RS-422A, and CCITT V.10, V.11, V.28, X.26 and X.27. The NE5180 is intended for use where the data transmission rate is up to 200 kb/s. The NE5181 covers the entire range of data rates up to 10 Mb/s. The difference in data rates for the two devices results from the input filtering of the NE5180. These devices also provide a failsafe feature which protects against certain input fault conditions.

FEATURES

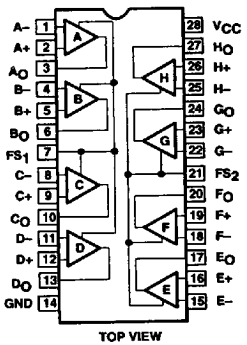
- Meets EIA RS-232C/423A/422A and CCITT V.10, V.11, V.28
- Single +5V supply—TTL compatible outputs
- Differential inputs withstand ±25V
- Failsafe feature
- Input noise filter (NE5180 only)
- Internal hysteresis
- Available in SMD PLCC

APPLICATIONS

- High-speed modems
- High-speed parallel communications
- Computer I/O ports
- Logic level translation

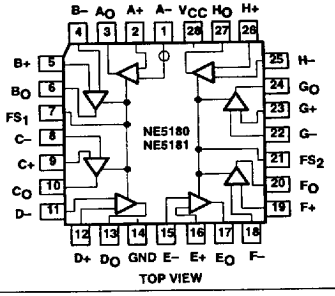
PIN CONFIGURATION

N Package



TOP VIEW

A Package



TOP VIEW

FUNCTION TABLE

INPUT	FAILSAFE INPUT	LOGIC OUTPUT
$V_{ID} > 200mV^1$	X	H
$V_{ID} < -200mV^1$	X	L
Both inputs open or grounded	0V	L
	V_{CC}	H

NOTE:
1. V_{ID} is defined as the non-inverting terminal input voltage minus the inverting terminal input voltage.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
28-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	NE5180N	0413B
28-Pin Plastic Dual In-Line (DIP) Package	0 to +70°C	NE5181N	0413B
28-Pin Plastic Lead Chip Carrier (PLCC) Package	0 to +70°C	NE5180A	0401F
28-Pin Plastic Lead Chip Carrier (PLCC) Package	0 to +70°C	NE5181A	0401F

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
P_D	Power dissipation	800	mW
V_{CC}	Supply voltage	7	V
V_{CM}	Common mode range	±15	V
V_{ID}	Differential input voltage	±25	V
I_{SINK}	Outputsink current	50	mV
V_{FS}	Failsafe voltage	−0.3 to V_{CC}	V
J_{OS}	Output short-circuit time	1	sec

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±5%, 0°C ≤ T_A ≤ +70°C, input common-mode range ±7V

SYMBOL	PARAMETER	TEST CONDITIONS		NE5180		NE5181		UNIT
				Min	Max	Min	Max	
R_{IN}	DC input resistance	3V ≤ |V_{IN}| ≤ 25V		3	7	3	7	kΩ
V_{OFS}	Failsafe output voltage	Inputs open or shorted to GND	0 ≤ I_{OUT} ≤ 8mA, $V_{failsafe}$ = 0V		0.45		0.45	V
			0 ≥ I_{OUT} ≥ −400µA, $V_{failsafe}$ = V_{CC}	2.7		2.7		
V_{th}	Differential input high[4] threshold	V_{OUT} ≥ 2.7V, I_{OUT} = −440µA	R_S = 0[1]		0.2		0.2	V
			R_S = 500[1]		0.4		0.4	
V_{tl}	Differential input low[4] threshold	V_{OUT} ≤ 0.45V, I_{OUT} = 8mA	R_S = 0[1]	−0.2		−0.2		V
			R_S = 500[1]	−0.4		−0.4		
V_H	Hysteresis[4]	FS = 0V or V_{CC} (See Figure 1)		50	140	50	140	mV
V_{IOC}	Open-circuit input voltage				2		2	V
C_I	Input capacitance				30		30	pF
V_{OH}	High level output voltage	V_{ID} = 1V, I_{OUT} = −440µA		2.7		2.7		V
V_{OL}	Low level output voltage	V_{ID} = −1V	I_{OUT} = 4mA[2]		0.4		0.4	V
			I_{OUT} = 8mA[2]		0.45		0.45	
I_{OS}	Short-circuit output current	V_{ID} = 1V [3]		20	100	20	100	mA
I_{CC}	Supply current	4.75V ≤ V_{CC} ≤ 5.25V, V_{ID} = −1V; FS = 0V			100		100	mA
I_{IN}	Input current	Other inputs grounded	V_{IN} = +10V		3.25		3.25	mA
			V_{IN} = −10V	−3.25		−3.25		

NOTES:
1. R_S is a resistor in series with each input.
2. Measured after 100ms warm-up (at 0°C).
3. Only 1 output may be shorted at a time and then only for a maximum of 1 second.
4. See Figure 1 for threshold and hysteresis definitions.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +5V ±5%, 0°C ≤ T_A ≤ +70°C

SYMBOL	PARAMETER	TEST CONDITIONS	NE5180		NE5181		UNIT
			Min	Max	Min	Max	
t_{PLH}	Propagation delay—low to high	C_L = 50pF, V_{ID} = ±1V		500		100	ns
t_{PHL}	Propagation delay—high to low	C_L = 50pF, V_{ID} = ±1V		500		100	ns
f_a	Acceptable input frequency	Unused input grounded, V_{ID} = ±200mV[1]		0.1		5.0	MHz
f_r	Rejectable input frequency	Unused input grounded, V_{ID} = ±500mV	5.5		NA		MHz

NOTE:
1. V_{ID} = ±1V for NE5181.

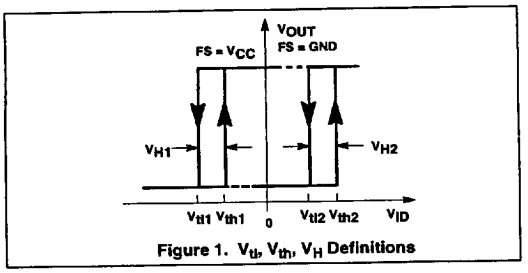
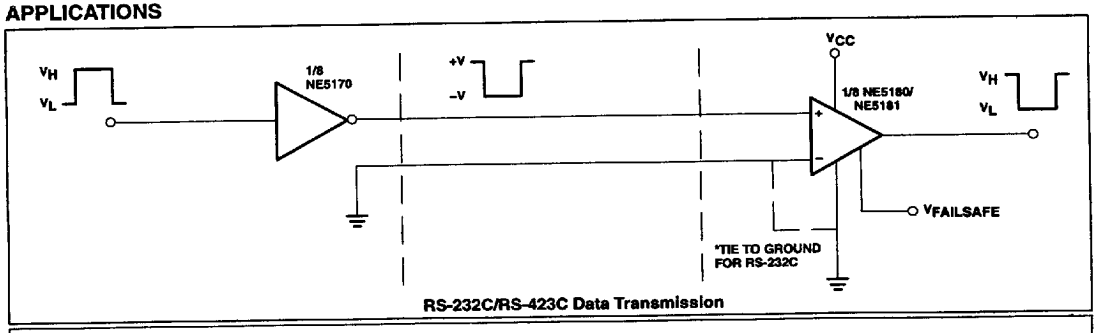


Figure 1. V_{th}, V_{th}, V_H Definitions

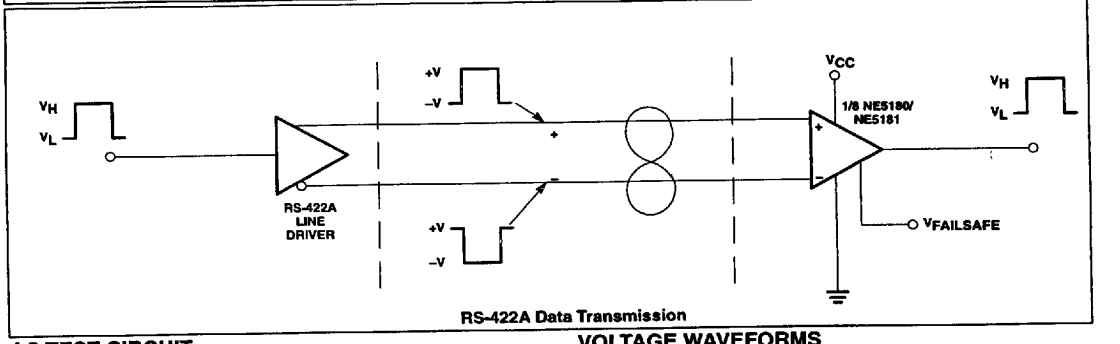
FAILSAFE OPERATION

These devices provide a failsafe operating mode to guard against input fault conditions as defined in RS-422A and RS-423A standards. These fault conditions are (1) driver in power-off condition, (2) receiver not interconnected with driver, (3) open-circuited interconnecting cable, and (4) short-circuited interconnecting cable. If one of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The receiver is programmed by connecting the failsafe input to V_{CC} or ground. A connection to

APPLICATIONS

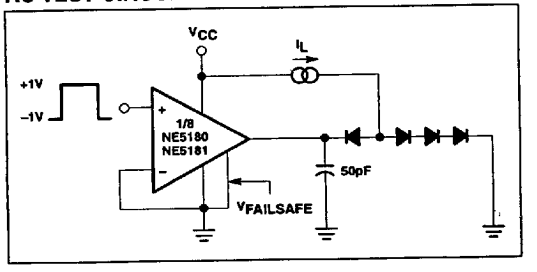


RS-232C/RS-423C Data Transmission

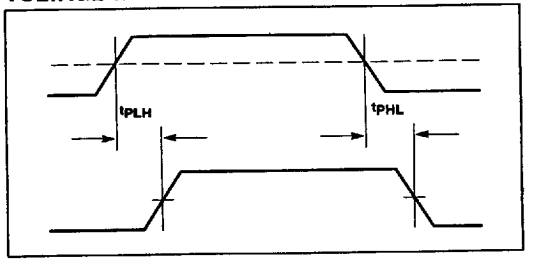


RS-422A Data Transmission

AC TEST CIRCUIT



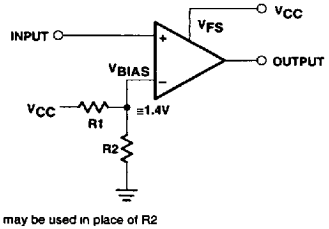
VOLTAGE WAVEFORMS



V_{CC} provides a logic "1" output under fault conditions, while a connection to ground provides a logic "0". There are two failsafe pins (F_{S1} and F_{S2}) on the NE5180 or NE5181 where each provides common failsafe control for four receivers.

RS-232 FAILSAFING

The internal failsafe circuitry works by providing a small input offset voltage which can be polarity-switched by using the failsafe control pins. This offset is kept small (approximately 80mV) to avoid degradation of the ±200mV input threshold for RS-423 or RS-422 operation. If the positive and negative inputs to any receiver are both shorted to ground or open circuited, the internal offset drives that output to the programmed failsafe state. If only one input open circuits (as may be the case for RS-232 operation), that input will rise to the "input open circuit voltage" (approximately 700mV). Since this is much greater than the 200mV threshold, the output will be driven to a state that is independent of the failsafe programming. Failsafe programming can be achieved for non-inverting single-ended applications by raising or lowering the unused input bias voltage as shown in Figure 2. For $V_{BIAS} \cong 1.4$, an open (or grounded) INPUT line will be approximately 700mV (0V) and the output will failsafe low. If the resistor divider is not used and V_{BIAS} is connected to ground, the output will failsafe high due to the internal failsafe offset for the INPUT grounded and the 700mV "open circuit input voltage" for the INPUT open circuited. Similar operation holds for an inverting configuration, with V_{BIAS} applied to the positive input and V_{FS} = ground.



NOTE:
Two silicon diodes may be used in place of R2

Figure 2. Single-Input Failsafe Programming

INPUT FILTERING (NE5180)

The NE5180 has input filtering for additional noise rejection. This filtering is a function of both signal level and frequency. For the specified input (5.5MHz at ±500mV) the input stage filter attenuates the signal such that the output stage threshold levels are not exceeded and no change of state occurs at the output. As the signal amplitude decreases (increases) the rejected frequency decreases (increases).

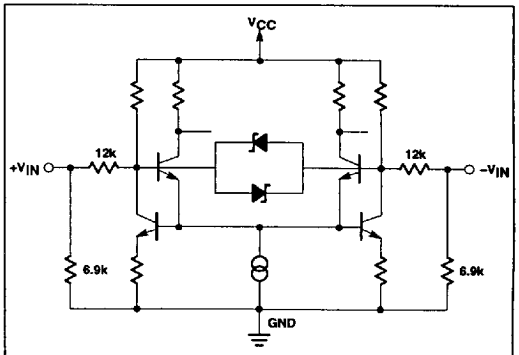


Figure 3. Differential Input Stage

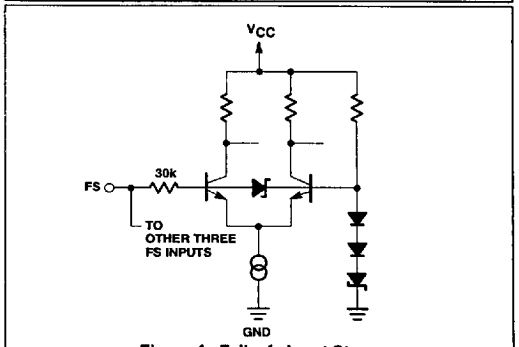


Figure 4. Failsafe Input Stage

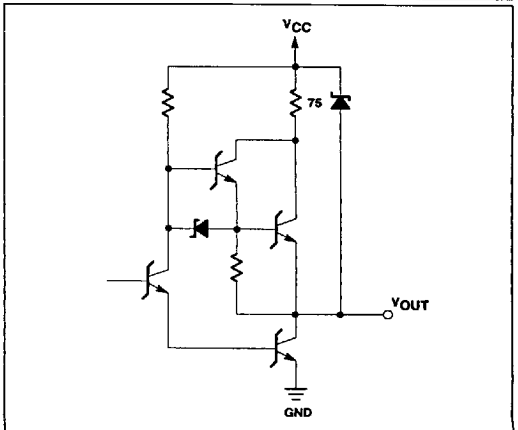


Figure 5. Output Stage

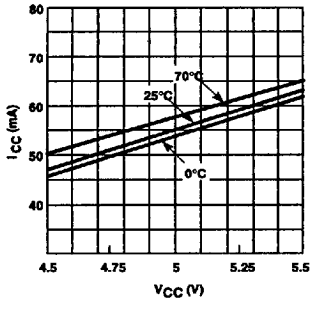


Figure 6. Typical Supply Current vs Supply Voltage

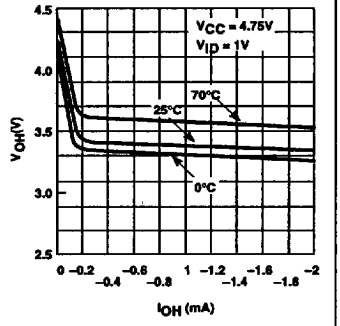


Figure 7. Typical High Level Output Voltage vs Output Current

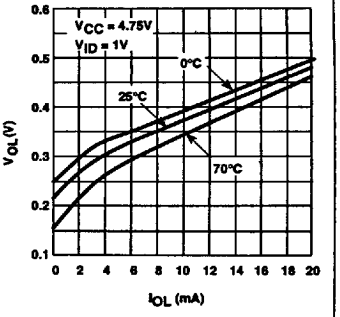
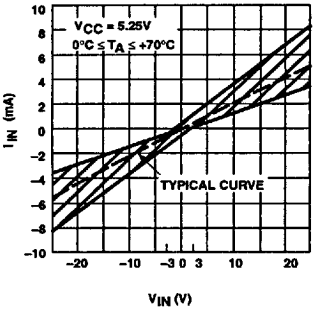


Figure 8. Typical Low Level Output Voltage vs Output Current



*This graph applies for all receiver inputs, provided that the opposite polarity input of the amplifier being measured is grounded.

Figure 9. Input Current vs Input Applied Voltage*

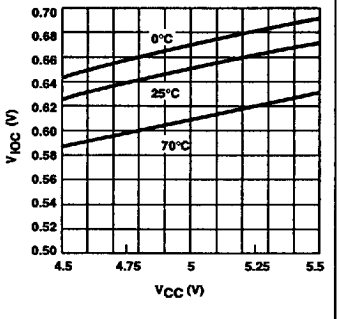


Figure 10. Typical V_{IOC} vs V_{CC}

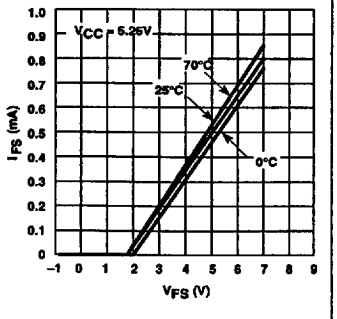


Figure 11. Typical FS Input Current vs FS Applied Voltage

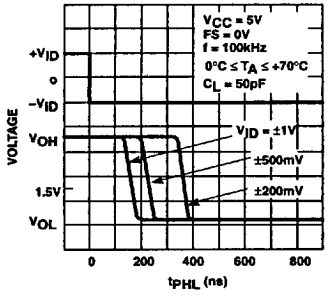


Figure 12. NE5180: Propagation Delay at Various Input Amplitudes

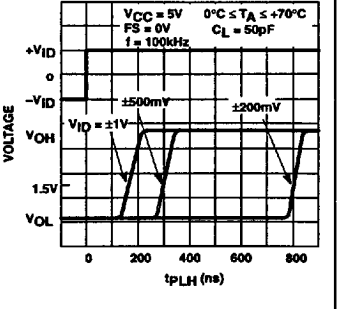


Figure 13. NE5180: Propagation Delay at Various Input Amplitude