

RF dual gain-stage

NE/SA5200

DESCRIPTION

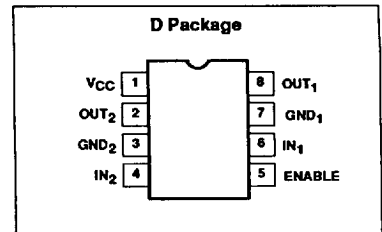
The NE/SA5200 is a dual amplifier with DC to 1200MHz response. Low noise ($NF = 3.6\text{dB}$) makes this part ideal for RF front-ends, and a simple power-down mode saves current for battery operated equipment. Inputs and outputs are matched to 50Ω .

The enable pin allows the designer the ability to turn the amplifiers on or off, allowing the part to act as an amplifier as well as an attenuator. This is very useful for front-end buffering in receiver applications.

FEATURES

- Dual amplifiers
- DC - 1200MHz operation
- Low DC power consumption (4.2mA per amplifier @ $V_{CC} = 5\text{V}$)
- Power-Down Mode ($I_{CC} = 95\mu\text{A}$ typical)
- 3.6dB noise figure at 900MHz
- Unconditionally stable
- Fully ESD protected
- Low cost
- Supply voltage 4-9V
- Gain $S_{21} = 7\text{dB}$ at $f = 1\text{GHz}$
- Input and output match S_{11} , S_{22} typically $< -14\text{dB}$

PIN CONFIGURATION



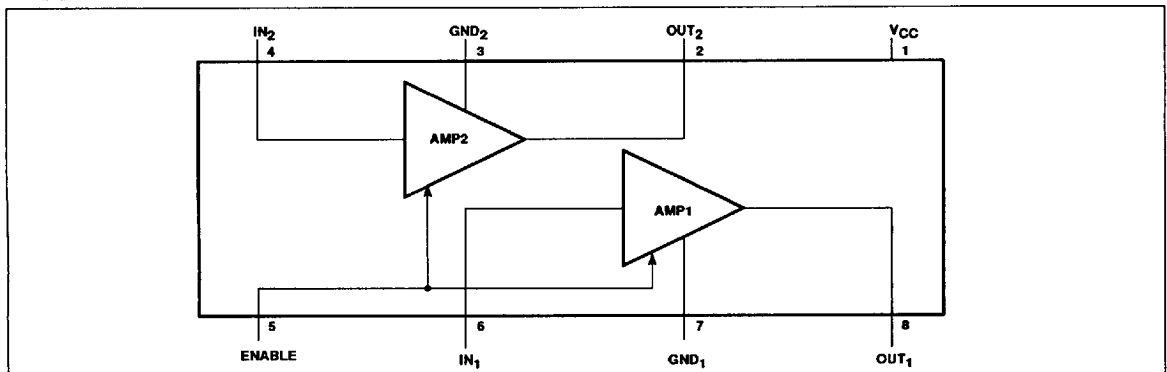
APPLICATIONS

- Cellular radios
- RF IF strips
- Portable equipment

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO (Surface-mount)	0-70°C	NE5200D
8-Pin Plastic SO (Surface-mount)	-40-+85°C	SA5200D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage ¹	-0.5 to +9	V
P_D	Power dissipation, $T_A = 25^\circ\text{C}$ (still air) ² 8-Pin Plastic SO	780	mW
T_{JMAX}	Maximum operating junction temperature	150	°C
P_{MAX}	Maximum power input/output	+20	dBm
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. Transients exceeding 10.5V on V_{CC} pin may damage product.
2. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA} :
8-Pin SO: $\theta_{JA} = 158^\circ\text{C/W}$

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.0 to 9.0	V
T_A	Operating ambient temperature range NE Grade SA Grade	0 to +70 -40 to +85	°C °C
T_J	Operating junction temperature NE Grade SA Grade	0 to +90 -40 to +105	°C °C

DC ELECTRICAL CHARACTERISTICS $V_{CC} = +5V$, $T_A = 25^\circ C$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4	5.0	9.0	V
I_{CC}	Total supply current	$V_{CC} = 5V$, ENABLE = High	6.4	8.4	10.4	mA
		$V_{CC} = 5V$, ENABLE = Low		95	255	µA
		$V_{CC} = 9V$, ENABLE = High		17.8	22.2	mA
		$V_{CC} = 9V$, ENABLE = Low		320	960	µA
V_T	TTL/CMOS logic threshold voltage ¹			1.25		V
V_{IH}	Logic 1 level	Power-up mode	2.0		V_{CC}	V
V_{IL}	Logic 0 level	Power-down mode	-0.3		0.8	V
I_{IL}	Enable input current	Enable = 0.4V	-1	0	1	µA
I_{IH}	Enable input current	Enable = 2.4V	-1	0	1	µA
$V_{IDC,ODC}$	Input and output DC levels		0.6	0.83	1.0	V

NOTE:

1. The ENABLE input must be connected to a valid logic level for proper operation of the NE/SA5200.

AC ELECTRICAL CHARACTERISTICS¹ $V_{CC} = +5V$, $T_A = 25^\circ C$, either amplifier, enable = 5V; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
S21	Insertion gain	$f = 100MHz$	9.2	11	13.2	dB
		$f = 900MHz$	5.2	7.5		dB
S22	Output return loss	$f = 900MHz$		-14.3		dB
S12	Reverse isolation	$f = 900MHz$		-17.9		dB
S11	Input return loss	$f = 900MHz$		-16.5		dB
P-1	Output 1dB compression point	$f = 900MHz$		-4.3		dBm
NF	Noise figure in 50Ω	$f = 900MHz$		3.6		dB
IP ₂	Input second-order intercept point	$f = 900MHz$		+4.3		dBm
IP ₃	Input third-order intercept point	$f = 900MHz$		-1.8		dBm
ISOL	Amplifier-to-amplifier isolation ²	$f = 900MHz$		-25		dB
P _{OUT}	Saturated output power	$f = 900MHz$		-1.7		dBm
S21	Insertion gain when disabled	$f = 100MHz$		-13		dB
		$f = 900MHz$		-13.5		dB

NOTE:

1. All measurements include the effects of the NE/SA5200 Evaluation Board (see Figure 2). Measurement system impedance is 50Ω.
2. Input applied to one amplifier, output taken at the other output. All ports terminated into 50Ω.

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APPLICATIONS

NE/SA5200 is a user-friendly, wide-band, unconditionally stable, low power dual gain amplifier circuit. There are several advantages to using the NE/SA5200 as a high frequency gain block instead of a discrete implementation. First is the simplicity of use. The NE/SA5200 does not need any external biasing components. Due to the higher level of integration and small footprint (SO8) package it occupies less space on the printed circuit board and reduces the manufacturing cost of the system. Also the higher level of integration improves the reliability of the amplifier over a discrete implementation with several components. The power down mode in the NE/SA5200 helps reduce power consumption in applications where the amplifiers can be disabled. And last but not the least is the impedance matching at inputs and outputs. Only those who have toiled through discrete transistor implementations for 50Ω input and output impedance matching can truly appreciate the elegance and simplicity of the NE/SA5200 input and output impedance matching to 50Ω.

A simplified equivalent schematic is shown in Figure 1. Each amplifier is composed of an NPN transistor with an Ft of 13GHz in a classical series-shunt feedback configuration. The two wideband amplifiers are biased from the same bias generator. In normal operation each amplifier consumes about 4mA of quiescent current (at VCC = 5V). In the disable mode the device consumes about 90μA of current, most of it is in the TTL enable buffer and the bias generator. The input impedance of the amplifiers is 50Ω. The amplifiers have typical gain of 11dB at 100MHz and 7dB of gain at 1.2GHz.

It can be seen from Figure 1 that any inductance between Pin 7, 3 and the ground plane will reduce the gain of the amplifiers at higher frequencies. Thus proper grounding of Pins 7 and 3 is essential for maximum gain and increased frequency response. Figure 2

shows the printed circuit board layout and the component placement for the NE/SA5200 evaluation board. The AC coupling capacitors should be selected such that at they are shorts at the desired frequency of operation. Since most low-cost large value surface mount capacitors cease to be simply capacitors in the UHF range and exhibit an inductive behavior, it is recommended that high frequency chip capacitors be utilized in the circuit. A good power supply bypass is also essential for the performance of the amplifier and should be as close to the device as practical.

Figure 3 shows the typical frequency response of the two channels of NE/SA5200. The low frequency gain is about 11dB at 100MHz and slowly drops off to 10dB at 500MHz. The gain is about 8dB at 900MHz and 7dB at 1.2 GHz which is typical of NE/SA5200 with a good printed circuit board layout. It can also be seen that both channels have a very well matched frequency response and matched gain to within 0.1dB at 100MHz and 0.2dB at 900MHz.

NE/SA5200 finds applications in many areas of RF communications. It is an ideal gain block for high performance, low cost, low power RF communications transceivers. A typical radio transceiver front-end is shown in Figure 4. This could be the front-end of a cellular phone, a VHF/ UHF hand-held transceiver, UHF cordless telephone or a spread spectrum system. The NE/SA5200 can be used in the receiver path of most systems as an LNA and pre-amplifier. The bandpass filter between the two amplifiers also minimize the noise into the first mixer. In the transmitter path, NE/SA5200 can be used as a buffer to the VCO and isolate the VCO from any load variations due to the power level changes in the power amplifier. This improves the stability of the VCOs. The NE/SA5200 can also be used as a pre-driver to the power amplifier modules.

The two amplifiers in NE/SA5200 can be easily cascaded to have a 13dB gain block at

900MHz. At 100MHz the gain will be 22dB and a noise figure of about 5.5dB. The NE/SA5200 can be operated at a higher voltage up to 9V for much improved 1dB output compression point and higher 3rd order intercept point.

Several stages of NE/SA5200 can also be cascaded and be used as an IF amplifier strip for DBS/TV/GPS receivers. Figure 5 shows a 60dB gain IF strip at 180MHz. The noise figure for the cascaded amplifier chain is given by equation 1.

$$NF \text{ (total)} = NF1 + NF2/G1 + NF3/G1 \cdot G2 + NF4/G1 \cdot G2 \cdot G3 + \dots \text{ (Equation 1)}$$

NOTE: The noise figure and gain should not be in dB in the above equation.

Since the noise figure for each stage is about 3.6dB and the gain is about 11dB, the noise figure for the 60dB gain IF strip will be about 6.4dB.

In applications where a single amplifier is required with a 7.5dB gain at 900MHz and current consumption is of paramount importance (battery powered receivers), the amplifier A1 can be used and amplifier A2 can be disabled by leaving GND2 (Pin 3) unconnected. This will reduce the total current consumption for the IC to a meager 4mA.

The ENABLE pin is useful for Time-Division-Duplex systems where the receiver can be disabled for a period of time. In this case the overall system supply current will be decreased by 8mA.

The ENABLE pin can also be used to improve the system dynamic range. For input levels that are extremely high, the NE/SA5200 can be disabled. In this case the input signal is attenuated by 13dB. This prevents the system from being overloaded as well as improves the system's overall dynamic range. In the disabled condition the NE/SA5200 IP3 increases to nearly +20dBm.

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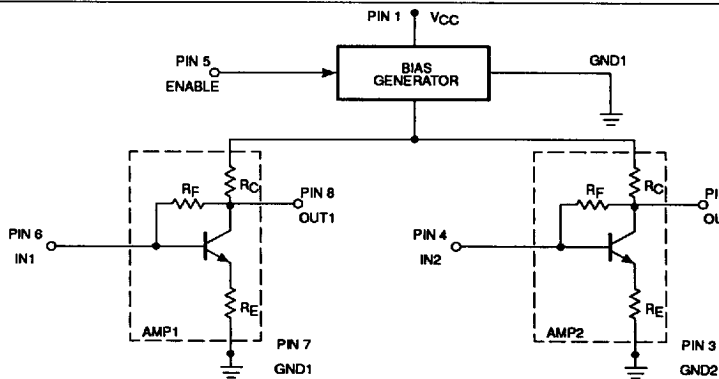
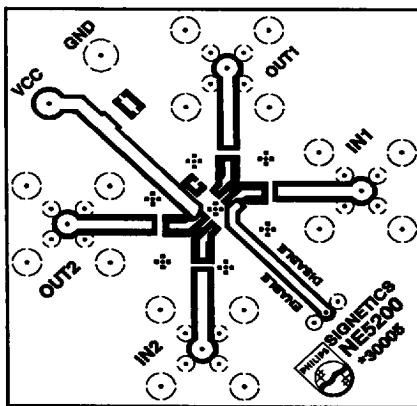
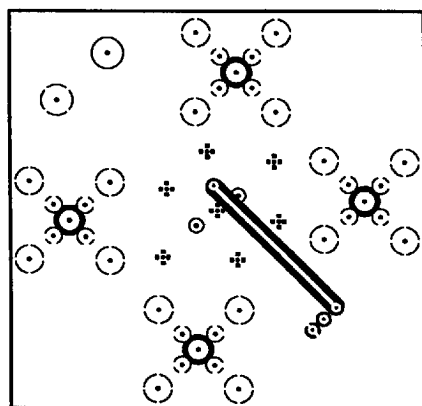


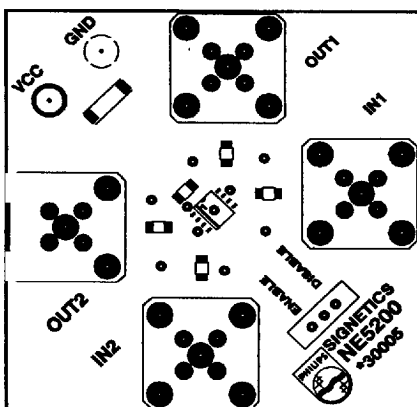
Figure 1. Simplified Equivalent Schematic of NE/SA5200



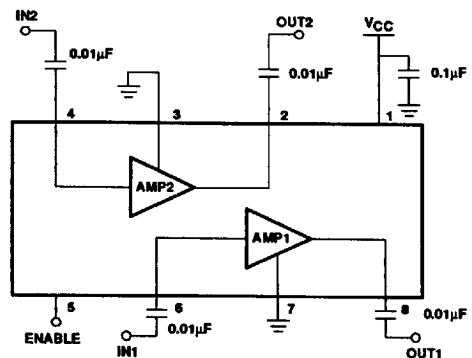
a. Top Side



b. Bottom Side



c. Top Silk Screen



d. NE/SA5200 Evaluation Board Schematic

Figure 2. Printed Circuit Board Layout of the NE/SA5200 Evaluation Board

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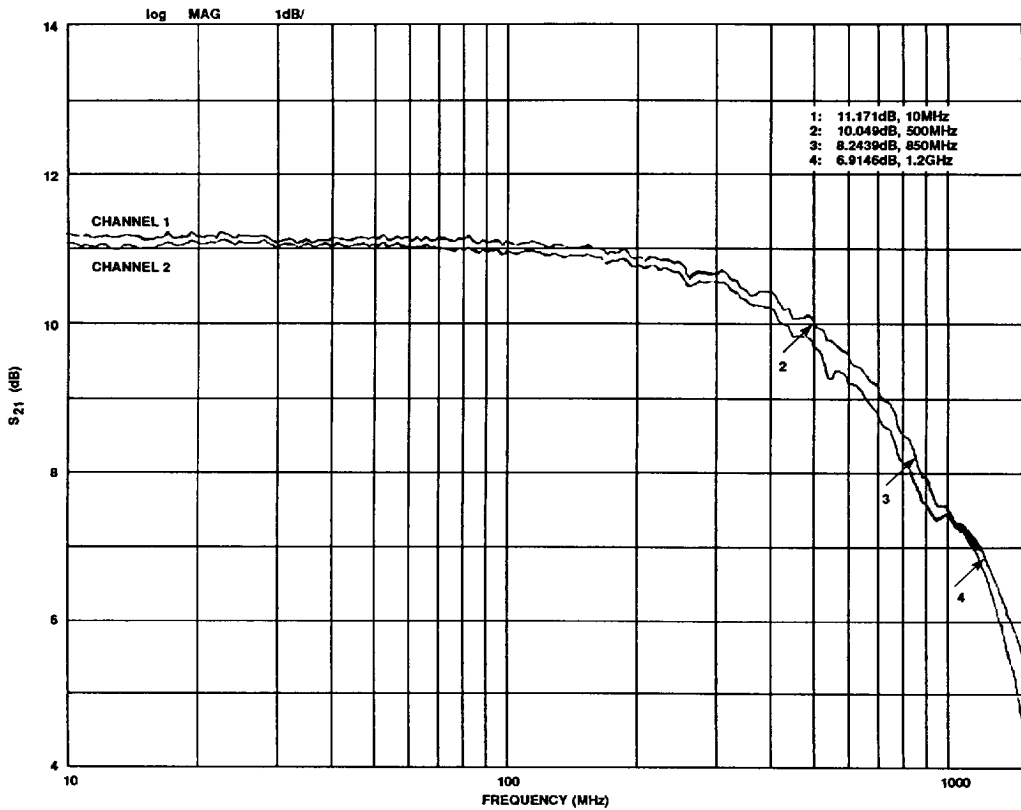


Figure 3. Typical Frequency Response of NE/SA5200 in a 50Ω System

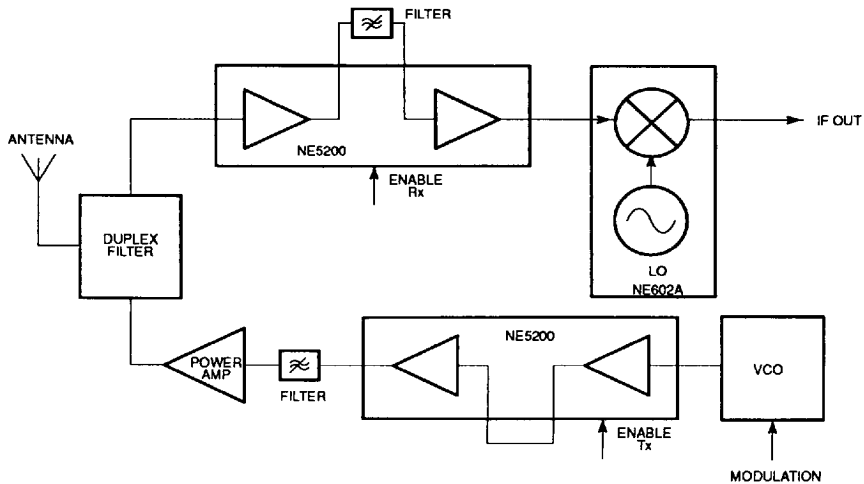
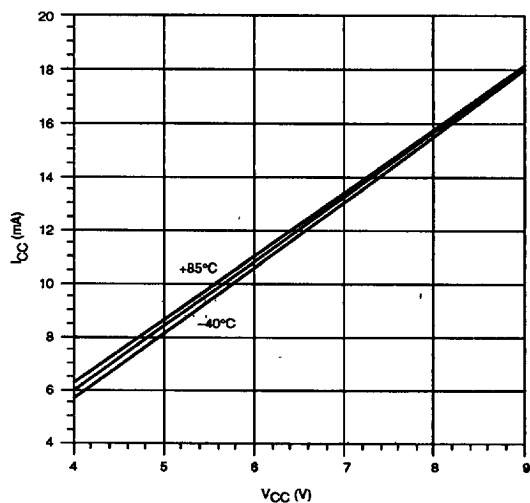
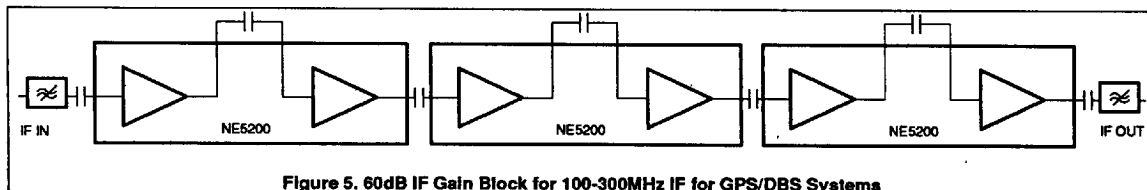


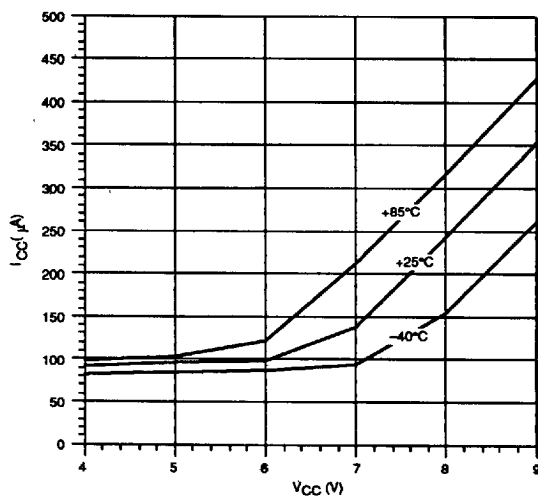
Figure 4. Typical Radio Transceiver Front-End

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**Figure 6. Supply Current
vs Supply Voltage and Temperature**



**Figure 7. Disabled Supply Current
vs V_{CC} and Temperature**

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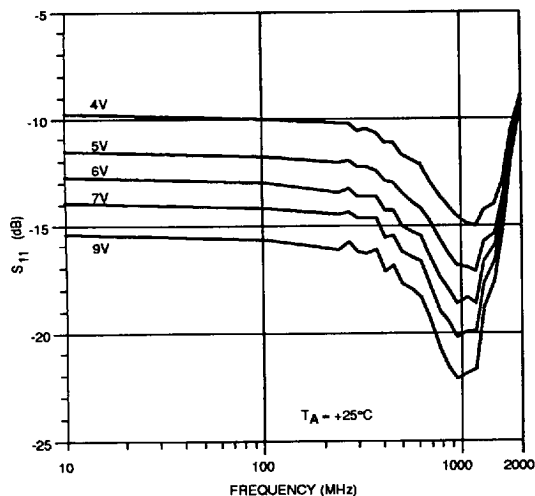


Figure 8. Input Match vs
Frequency and V_{CC}

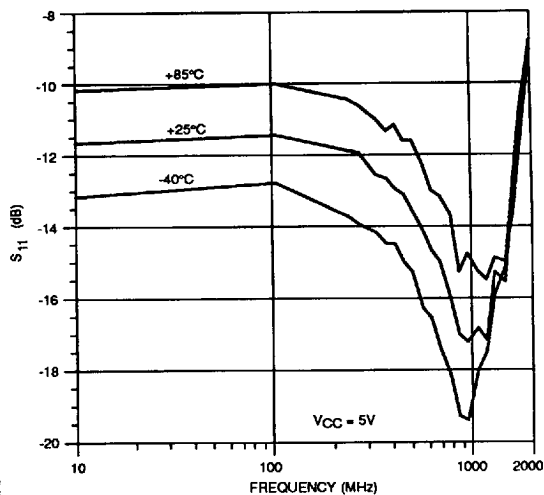


Figure 9. Input Match vs
Frequency and Temperature

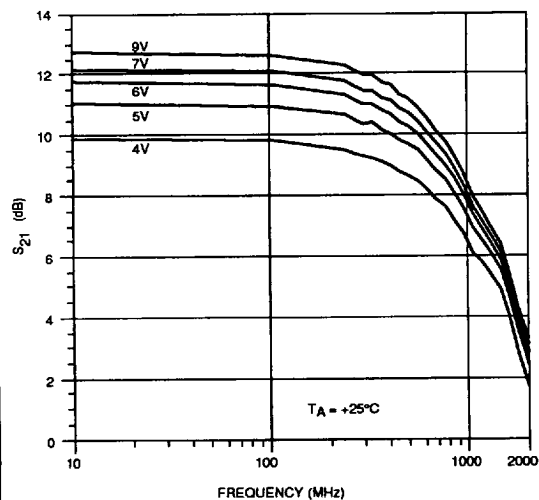


Figure 10. Insertion Gain vs
Frequency and V_{CC}

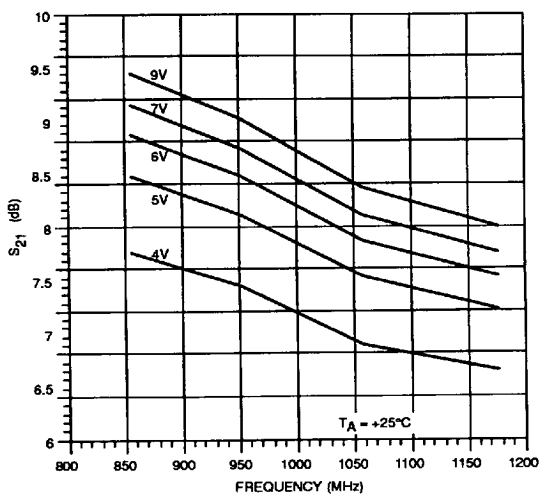


Figure 11. Insertion Gain vs
Frequency and V_{CC}
— Expanded Detail —

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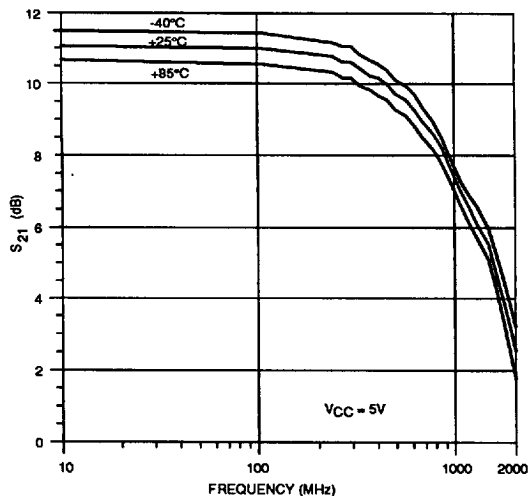


Figure 12. Insertion Gain vs
Frequency and Temperature

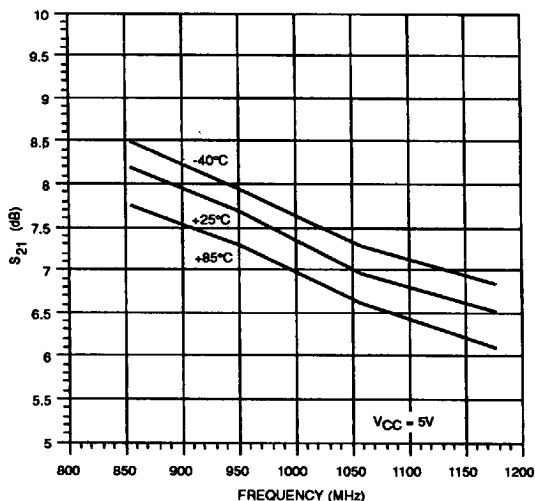


Figure 13. Insertion Gain vs
Frequency and Temperature
– Expanded Detail –

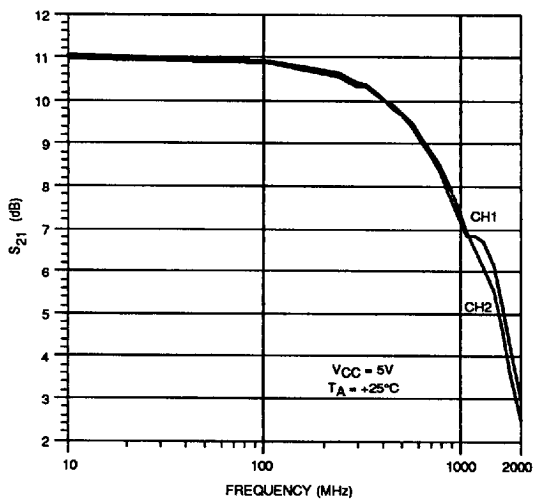


Figure 14. Insertion Gain Matching
(CH1 vs CH2) vs Frequency

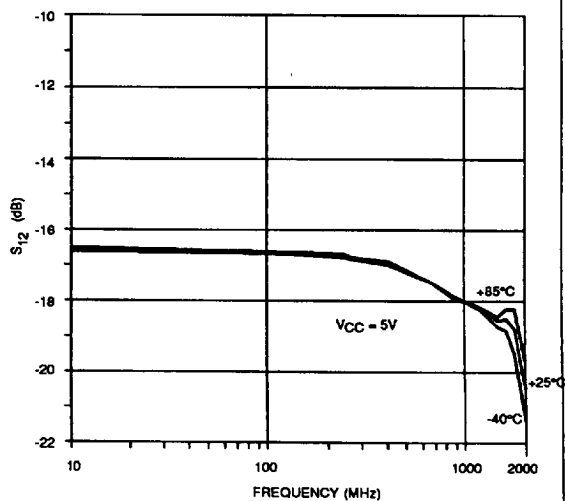


Figure 15. Reverse Insertion Gain vs
Frequency and Temperature

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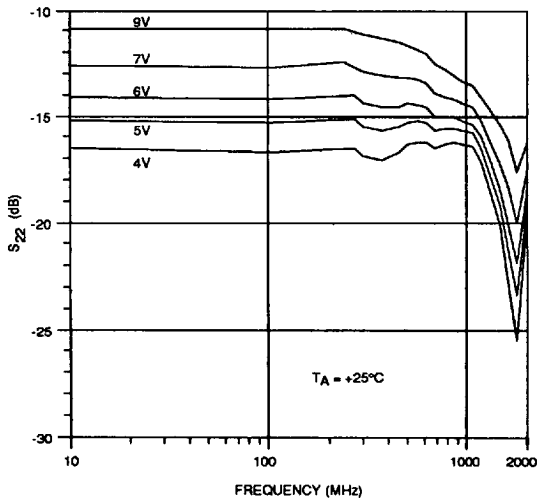


Figure 16. Output Match vs
Frequency and V_{CC}

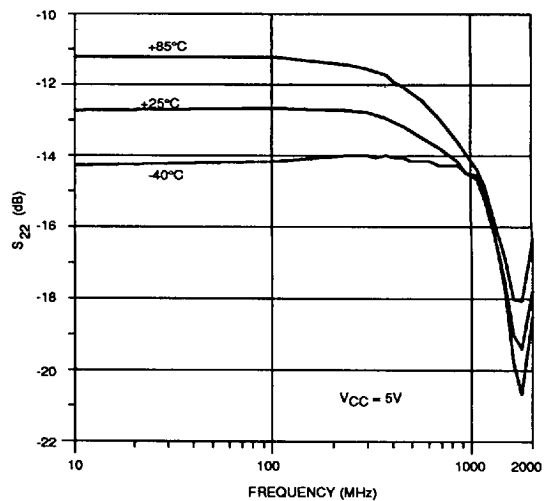


Figure 17. Output Match vs
Frequency and Temperature

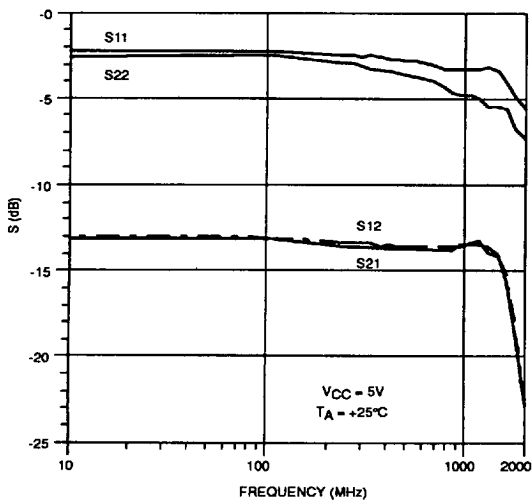


Figure 18. S-parameters vs
Frequency for Disabled Amplifier

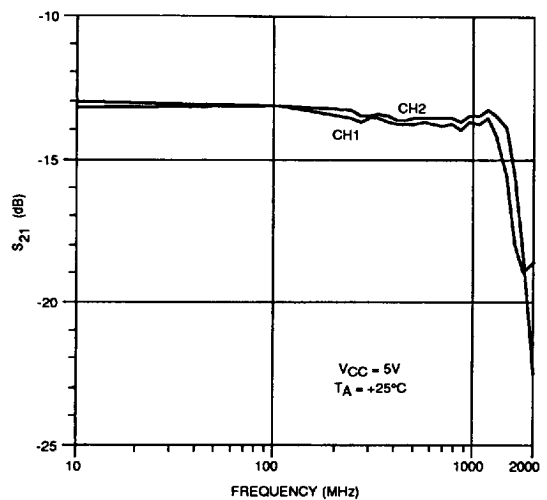


Figure 19. Insertion Gain Matching
Disabled (CH1 vs CH2) vs Frequency

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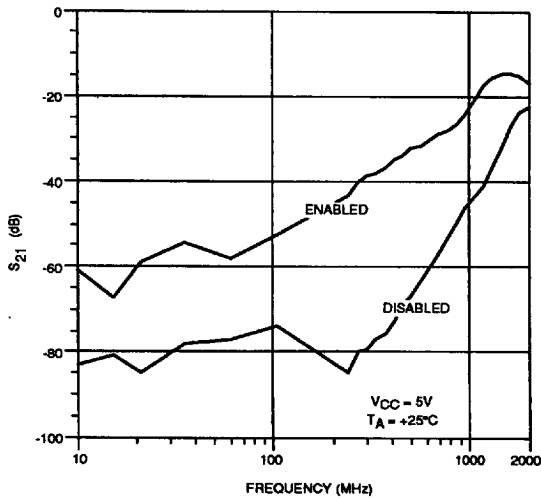


Figure 20. CH1 Input to CH2 Output Isolation vs. Frequency

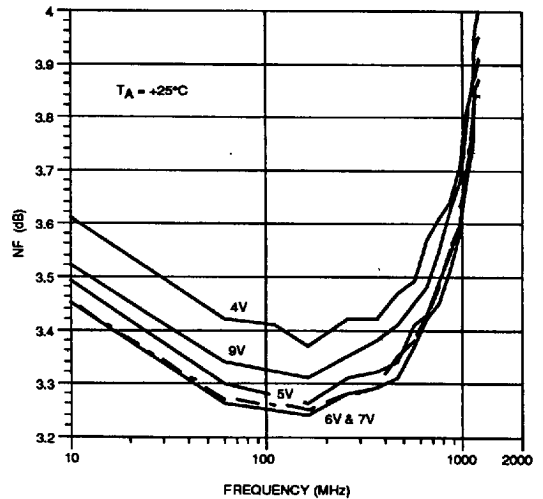


Figure 21. Noise Figure vs Frequency and V_{CC} in a 50Ω System

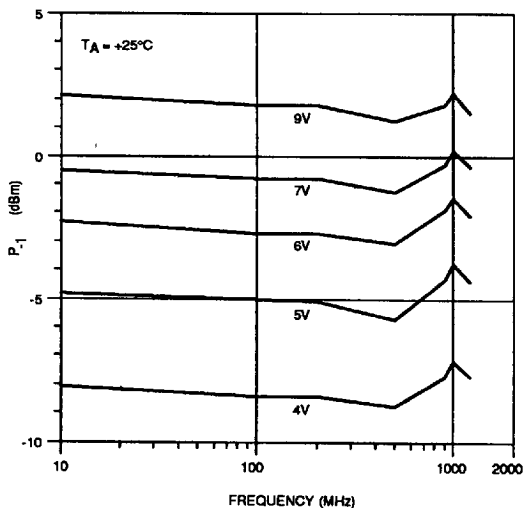


Figure 22. 1dB Output Compression Point vs Frequency and V_{CC}

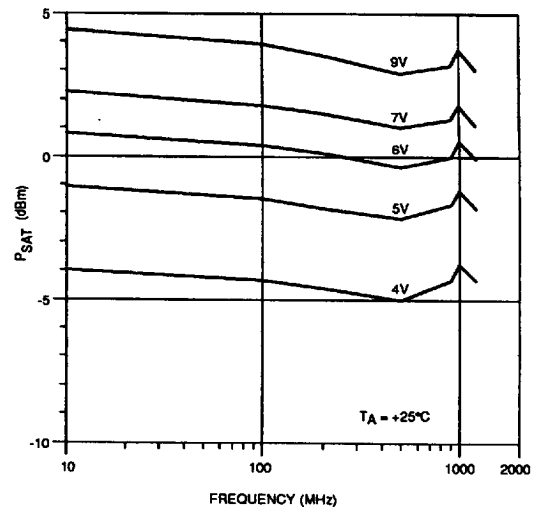


Figure 23. Saturated Output Power vs Frequency and V_{CC}

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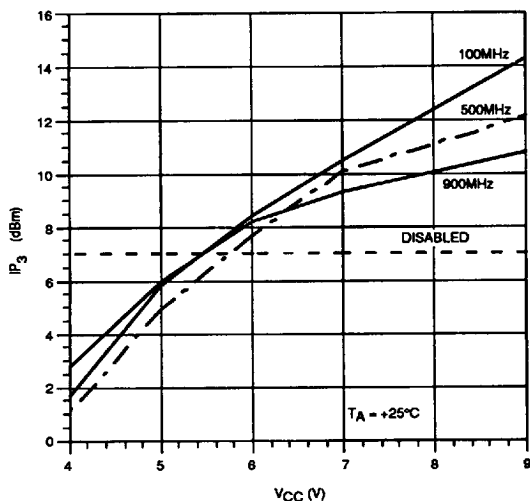


Figure 24. Third-Order Output Intercept
vs Frequency and V_{CC}

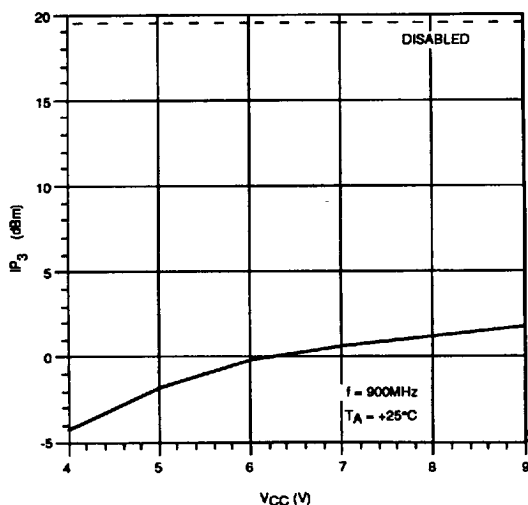


Figure 25. Third-Order Input Intercept
vs Frequency and V_{CC}

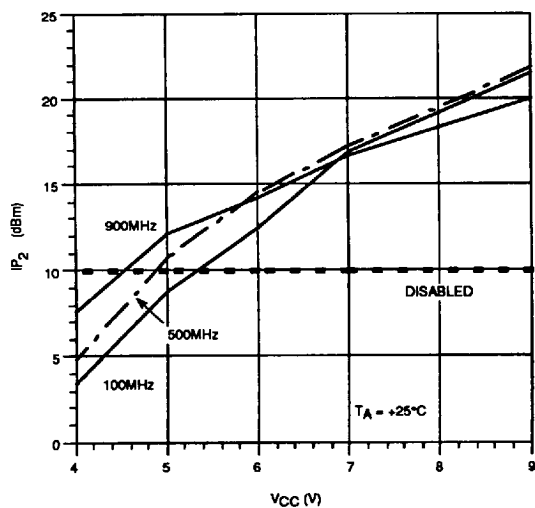


Figure 26. Second-Order Output Intercept
vs Frequency and V_{CC}

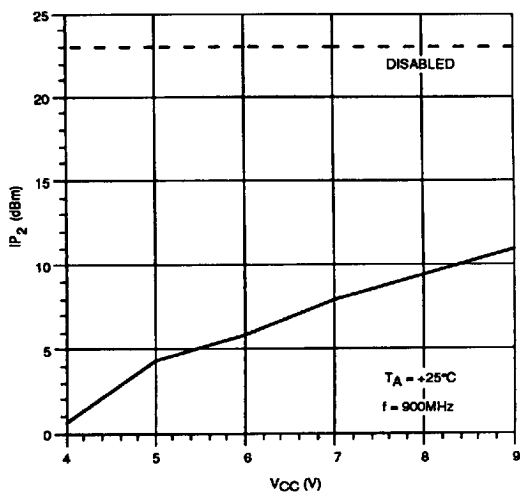


Figure 27. Second-Order Input Intercept
vs Frequency and V_{CC}

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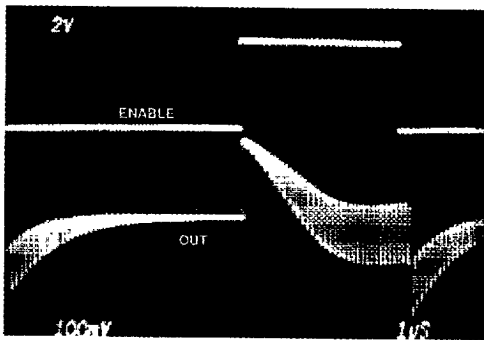


Figure 28. Switching Speed; $f_{IN} = 10\text{MHz}$ at -26dBm , $V_{DD} = 5\text{V}$, Coupling Capacitors Set to $0.01\mu\text{F}$

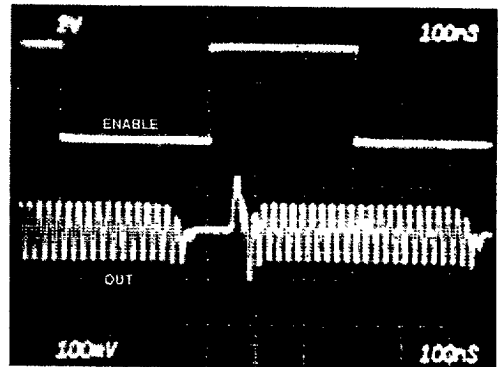


Figure 29. Switching Speed; $f_{IN} = 50\text{MHz}$ at -26dBm , $V_{DD} = 5\text{V}$, Coupling Capacitors Set to 100pF