DATA SHEET

NE/SA5217
Postamplifier with link status indicator

Product specification

1995 Apr 26

IC19

PHILIPS

Postamplifier with link status indicator NE/SA5217

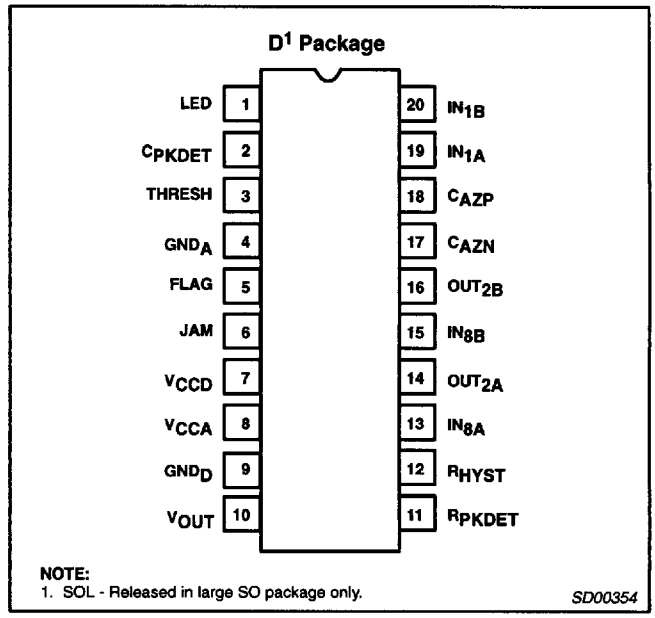
DESCRIPTION

The NE/SA5217 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The NE5217 can be DC coupled with the previous transimpedance stage using NE5210, NE5211 or NE5212A transimpedance amplifiers. The main difference between the NE5217 and the NE5214 is that the NE5217 does not make the output of A1 and input of A2 accessible; instead, it brings out the output of A2 and the input of A8 thus activating the on-chip Schmitt trigger function by connecting two external capacitors. The result is that a much longer string of 1s and 0s, in the bit stream, can be tolerated. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide adjustable input threshold and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, thereby insuring a low Bit Error Rate (BER). An auto-zero loop can be used to replace two input coupling capacitors with a single Auto Zero (AZ) capacitor. A signal absent flag indicates when signals are below threshold. The low signal condition forces the TTL output to the last logic state. User interaction with this "jamming" system is available. The NE/SA5217 is packaged in a standard 20-pin surface-mount package and typically consumes 40mA from a standard 5V supply. The NE/SA5217 is designed as a companion to the NE/SA5211/5212A and NE5210 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the postamplifier inputs. The NE5210/5217, NE/SA5211/5217 or NE/SA5212A/5217 combinations convert nanoamps of photodetector current into standard digital TTL levels.

APPLICATIONS

- Fiber optics
- Communication links in Industrial and/or Telecom environment with high EMI/RFI
- Local Area Networks (LAN)
- Synchronous Optical Networks (SONET) STS-1
- RF limiter
- Good for 2^{23} -1 pseudo random bit stream

PIN CONFIGURATION



NOTE:
1. SOL - Released in large SO package only.

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FEATURES

- Postamp for the NE/SA5211/5212A. NE5210 preamplifier family
- Wideband operation: typical 75MHz (150MBaud NRZ)
- Interstage filtering/equalization possible
- Single 5V supply
- Low signal flag
- Output disable
- Link status threshold and hysteresis programmable
- LED driver (normally ON with above threshold signal)
- Fully differential for excellent PSRR
- Auto-zero loop for DC offset cancellation
- 2kV ElectroStatic Discharge (ESD) protection

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) Package	0 to +70°C	NE5217D	SOT163-1
20-Pin Plastic Small Outline Large (SOL) Package	-40 to +85°C	SA5217D	SOT163-1

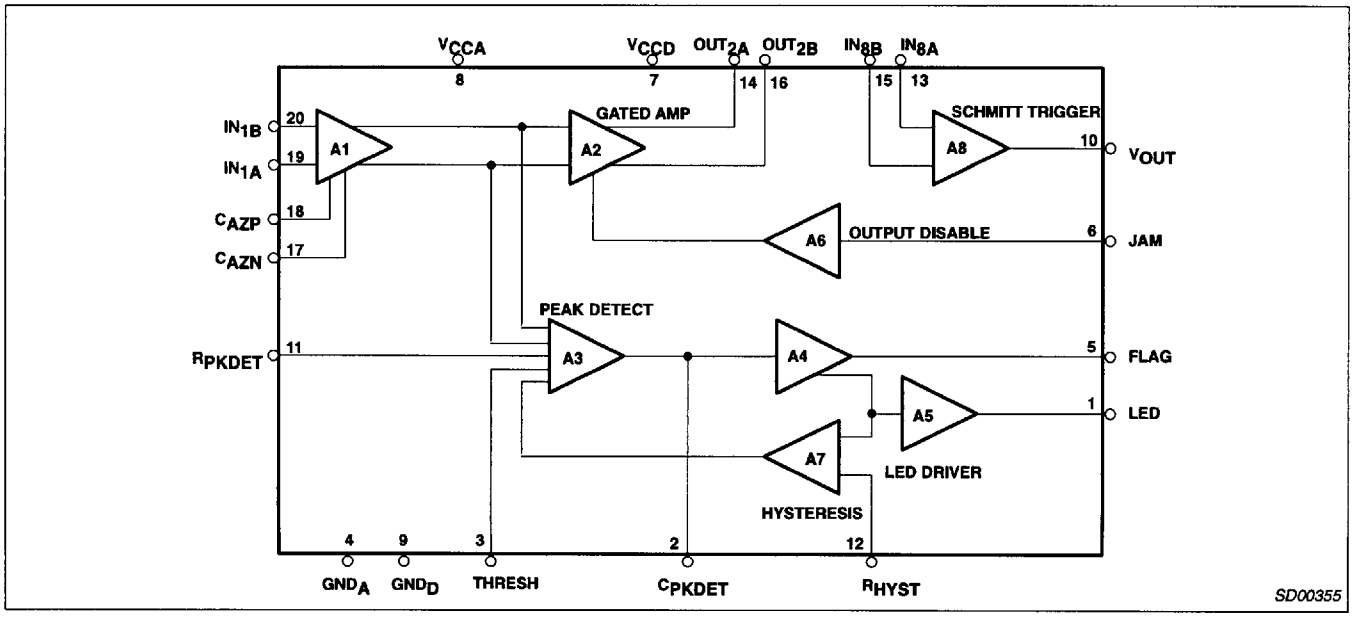
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Power supply	+6	+6	V
V_{CCD}	Power supply	+6	+6	V
T_A	Operating ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	-55 to +150	-55 to +150	°C
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C
P_D	Power dissipation	1.4	1.4	W
V_{IJ}	Jam input voltage	-0.5 to 5.5	-0.5 to 5.5	V

PIN DESCRIPTIONS

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver. Open collector output transistor with 125Ω series limiting resistor. An above threshold signal turns this transistor ON.
2	C_{PKDET}	Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor.
3	THRESH	Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector.
4	GND_A	Device analog ground pin.
5	FLAG	Peak detector digital output. When this output is LOW, there is data present above the threshold. This pin is normally connected to the JAM pin and has a TTL fanout of two.
6	JAM	Input to inhibit data flow. Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, LOW. This pin is normally connected to the FLAG pin and is TTL-compatible.
7	V_{CCD}	Power supply pin for the digital portion of the chip.
8	V_{CCA}	Power supply pin for the analog portion of the chip.
9	GND_D	Device digital ground pin.
10	V_{OUT}	TTL output pin with a fanout of five.
11	R_{PKDET}	Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}.
12	R_{HYST}	Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector.
13	IN_{8A}	Non-inverting input to amplifier A8.
14	OUT_{2A}	Non-inverting output of amplifier A2.
15	IN_{8B}	Inverting input to amplifier A8.
16	OUT_{2B}	Inverting output of amplifier A2.
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
19	IN_{1A}	Non-inverting input of the preamp A1.
20	IN_{1B}	Inverting input of the preamp A1.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING		UNIT
		NE5217	SA5217	
V_{CCA}	Power supply	4.5 to 5.5	4.5 to 5.5	V
V_{CCD}	Power supply	4.5 to 5.5	4.5 to 5.5	V
T_A	Ambient temperature range	0 to +70	-40 to +85	°C
T_J	Operating junction temperature range	0 to +95	-40 to +110	°C
P_D	Power dissipation	300	300	mW

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5217			SA5217			
			Min	Typ	Max	Min	Typ	Max	
I_{CCA}	Analog supply current			30	40		30	41.2	mA
I_{CCD}	Digital supply current (TTL, Flag, LED)			10	13.3		10	13.5	mA
V_{I1}	A1 input bias voltage (A,B inputs)		3.11	3.4	3.68	3.08	3.4	3.70	V
V_{O2}	A1 output bias voltage (A,B outputs)		3.17	3.8	4.45	3.10	3.8	4.50	V
V_{I8L}	A8 input bias voltage Low (A,B inputs)		3.40	3.55	3.68	3.40	3.55	3.68	V
V_{I8H}	A8 input bias voltage High (A,B inputs)		3.70	3.91	4.10	3.68	3.91	4.12	V
V_{OH}	High-level TTL output voltage	I_{OH}=-200µA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level TTL output voltage	I_{OL}=8mA		0.3	0.4		0.3	0.4	V
I_{OH}	High-level TTL output current	V_{OUT}=2.4V		-40	-26		-40	-24.4	mA
I_{OL}	Low-level TTL output current	V_{OUT}=0.4V	8.0	30		7.0	30		mA
I_{OS}	Short-circuit TTL output current	V_{OUT}=0.0V		-95			-95		mA
V_{THRESH}	Threshold bias voltage	Pin 3 Open		0.75			0.75		V
V_{RPKDET}	RPKDET	Pin 11 Open		0.72			0.72		V
V_{RHYST}	RHYST bias voltage	Pin 12 Open		0.72			0.72		V
V_{IHJ}	High-level jam input voltage		2.0			2.0			V
V_{ILJ}	Low-level jam input voltage				0.8			0.8	V
I_{IHJ}	High-level jam input current	V_{IJ}=2.7V			20			30	µA
I_{ILJ}	Low-level jam input current	V_{IJ}=0.4V	-450	-240		-485	-240		µA
V_{OHF}	High-level flag output voltage	I_{OH}=-80µA	2.4	3.8		2.4	3.8		V
V_{OLF}	Low-level flag output voltage	I_{OL}=3.2mA		0.33	0.4		0.33	0.4	V
I_{OHF}	High-level flag output current	V_{OUT}=2.4V		-18	-5.3		-18	-5	mA
I_{OLF}	Low-level flag output current	V_{OUT}=0.4V	3.6	10		3.25	10		mA
I_{SCF}	Short-circuit flag output current	V_{OUT}=0.0V	-60	-40	-25	-61	-40	-26	mA
I_{LEDH}	LED ON maximum sink current	V_{LED}=3.0V	13	22	80	8	22	80	mA

AC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5217			SA5217			
			Min	Typ	Max	Min	Typ	Max	
f_{OP}	Maximum operating frequency	Test circuit	60	75		60	75		MHz
V_{INH}	Maximum Functional A1 input signal (single ended)	Test Circuit		1.6			1.6		V_{P-P}
V_{INL}	Minimum Functional A1 input signal (single-ended)	Test CIrcuit		6			6		mV_{P-P}
	Minimum Functional A1 input signal (differential)			3			3		
	Minimum input sensitivity for output BER $\leq 10^{-9}$ (single-ended)	PRBS = $2^{23}-1$		9			9		mV_{P-P}
	Minimum input sensitivity for output BER $\leq 10^{-9}$ (differential)			4.5			4.5		
R_{IN1}	Input resistance (differential at IN_1)	PRBS = $2^{23}-1$		1200			1200		Ω
C_{IN1}	Input capacitance (differential at IN_1)			2			2		pF
R_{IN8}	Input resistance (differential at IN_2)			2000			2000		Ω
C_{IN2}	Input capacitance (differential at IN_2)			2			2		pF
R_{OUT2}	Output resistance (differential at OUT_2)			25			25		Ω
C_{OUT2}	Output capacitance (differential at OUT_2)			2			2		pF
V_{HYS}	Hysteresis voltage range (single-ended)	Test circuit, $T_A = 25°C$ R_{RHYST}=5k R_{THRESH}=33k		10			10		mV_{P-P}
	Hysteresis voltage range (differential)			5			5		
V_{THR}	Threshold voltage (single-ended)	(FLAG Low) Test circuit, @ 50MHz		19			19		mV_{P-P}
	Threshold voltage (differential)	R_{RHYST}=4k R_{THRESH}=33k		9.5			9.5		
t_{TLH}	TTL Output Rise Time 20% to 80%	Test Circuit		1.3			1.3		ns
t_{THL}	TTL Output Fall Time 80% to 20%	Test Circuit		1.2			1.2		ns
t_{RFD}	t_{TLH}/t_{THL} mismatch			0.1			0.1		ns
t_{PWD}	Pulse width distortion of output	50mV_{P-P}, 1010. . .input Distortion = $\frac{T_H - T_L}{T_H + T_L} 10^2$		TBD			TBD		%

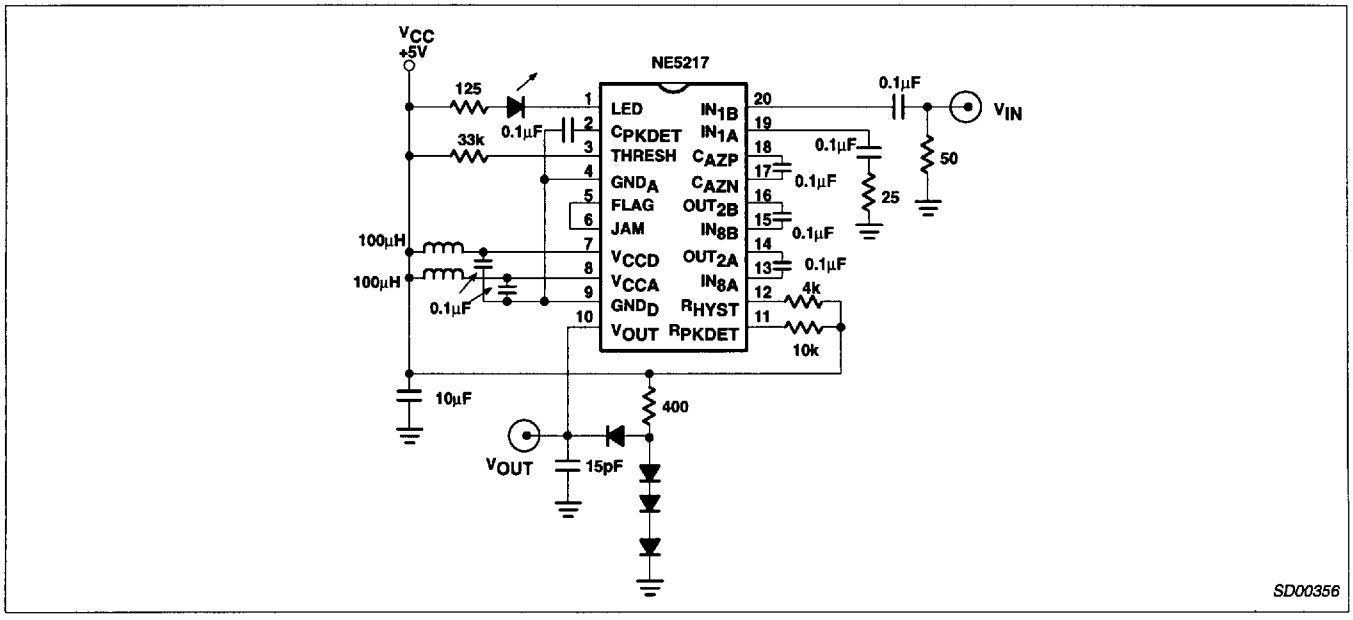
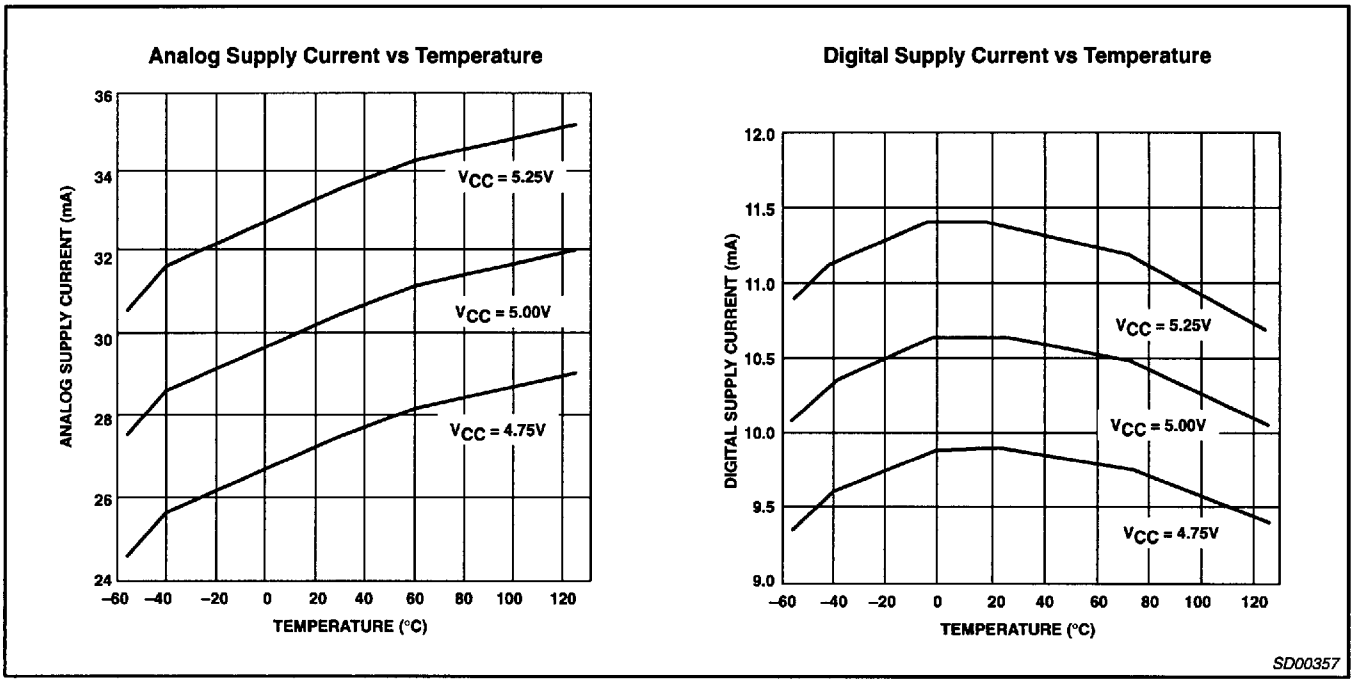
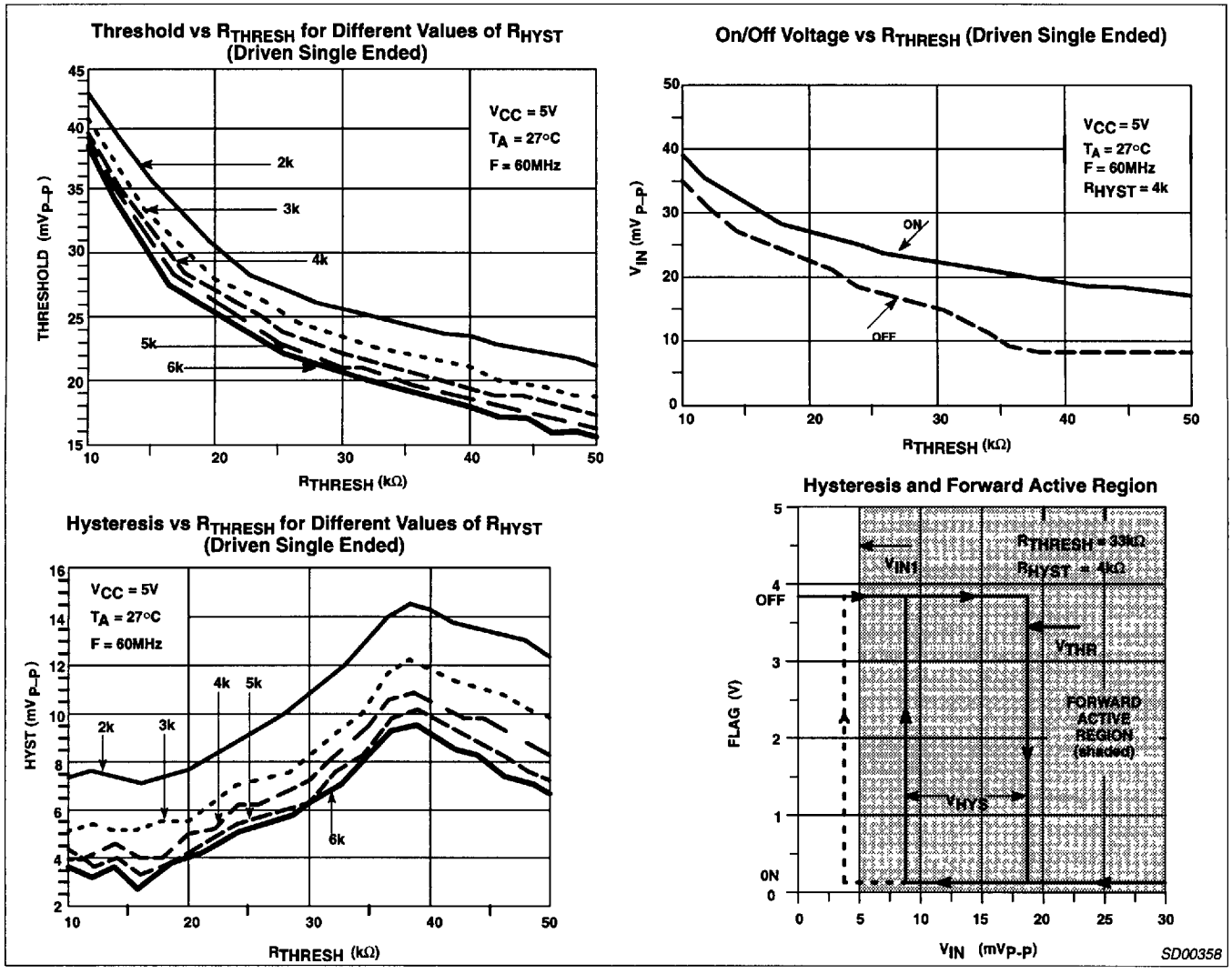


Figure 1. AC Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (continued)



THEORY OF OPERATION AND APPLICATION

The NE5217 postamplifier is a highly integrated chip that provides up to 60dB of gain at 60MHz, to bring mV level signals up to TTL levels.

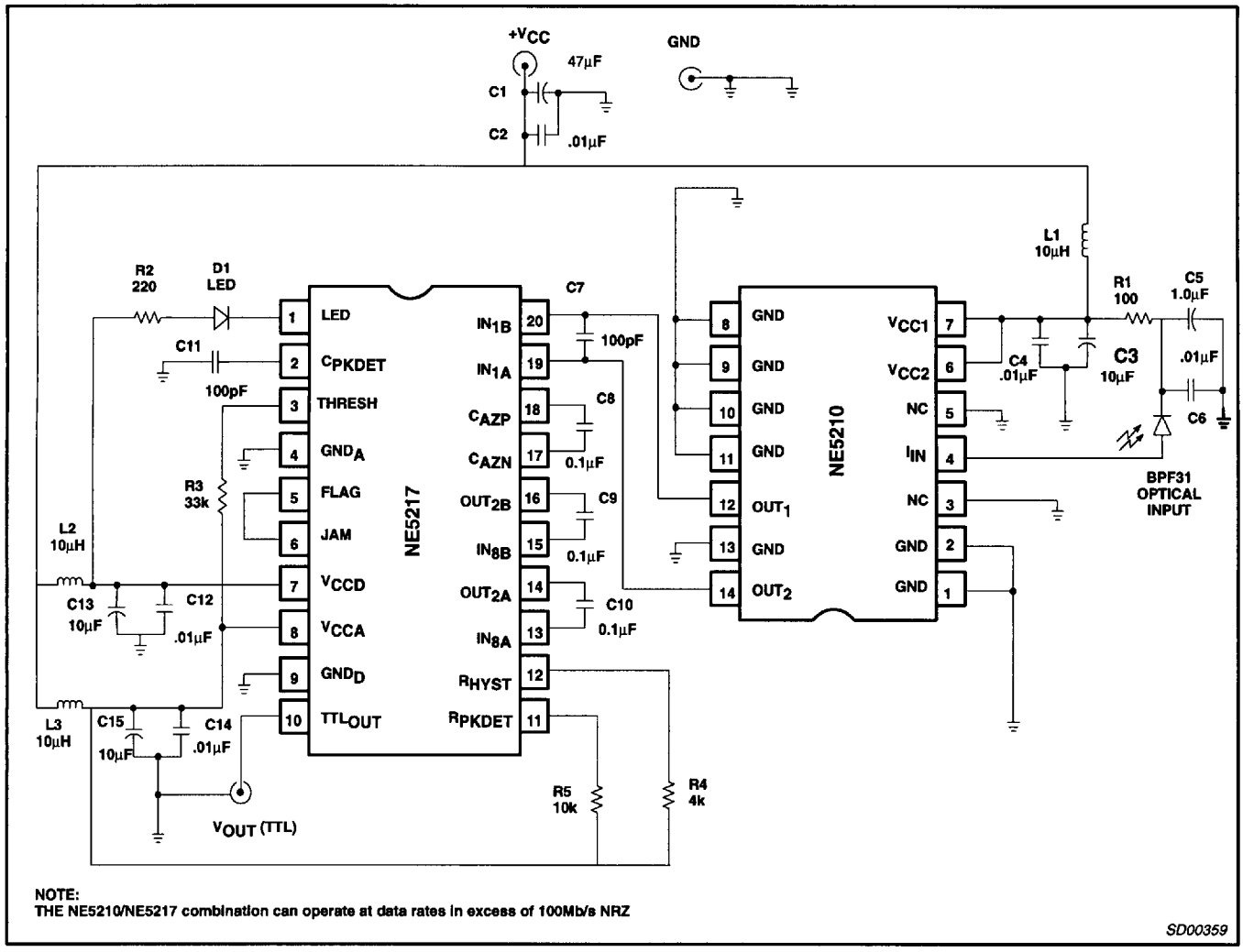
The NE5217 contains eight amplifier blocks (see Block Diagram). The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3-A4-A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times. It outputs a TTL High on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on-chip LED driver turns the external LED to the On state when the input signal is above the threshold. In a typical application the "FLAG" output is tied back tot he "JAM" input; forcing the "JAM" input to TTL High will latch the TTL Data Out at the last logical state.

Threshold voltage and hysteresis voltage range are adjustable with resistors R_{THRESH} and R_{HYST}. The typical values given in the data sheet will result in performance shown in the graph "Hysteresis and Forward Active Region". A minority of parts may be sensitive enough that FLAG High (Off) occurs below the minimum functional input signal level, V_{IN1}. This condition is shown by the dotted line in the graph. Such parts may require adjustment of R_{THRESH} if it is important to guarantee that an output signal is present for the full hysteresis range. If this is not important, R_{THRESH} may be adjusted to give a FLAG Low for lower level input signals.

An auto-zero loop allows the NE5217 to be directly connected to a transimpedance amplifier such as the NE5210, NE5211, or NE5212A without coupling capacitors. This auto-zero loop cancels the transimpedance amplifier's DC offset, the NE5217 A1 offset, and the data-dependent offset in the PIN diode/transimpedance amplifier combination.

A typical application of the NE5217 postamplifier is depicted in Figure 2. The system uses the NE5211 transimpedance amplifier which has a 28k differential transimpedance gain and a -3dB bandwidth of 140MHz. this typical application is optimized for a 50Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.



NOTE:
THE NE5210/NE5217 combination can operate at data rates in excess of 100Mb/s NRZ

SD00359

Figure 2. A 50Mb/s Fiber Optic Receiver

For more information on this application, please refer to Application Brief AB1432.

Die Sales Disclaimer

Due to the limitations in testing high frequency and other parameters at the die level, and the fact that die electrical characteristics may shift after packaging, die electrical parameters are not specified and die are not guaranteed to meet electrical characteristics (including temperature range) as noted in this data sheet which is intended only to specify electrical characteristics for a packaged device.

All die are 100% functional with various parametrics tested at the wafer level, at room temperature only (25°C), and are guaranteed to be 100% functional as a result of electrical testing to the point of wafer sawing only. Although the most modern processes are utilized for wafer sawing and die pick and place into waffle pack carriers, it is impossible to guarantee 100% functionality through this process. There is no post waffle pack testing performed on individual die.

Since Philips Semiconductors has no control of third party procedures in the handling or packaging of die, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems on any die sales.

Although Philips Semiconductors typically realizes a yield of 85% after assembling die into their respective packages, with care customers should achieve a similar yield. However, for the reasons stated above, Philips Semiconductors cannot guarantee this or any other yield on any die sales.

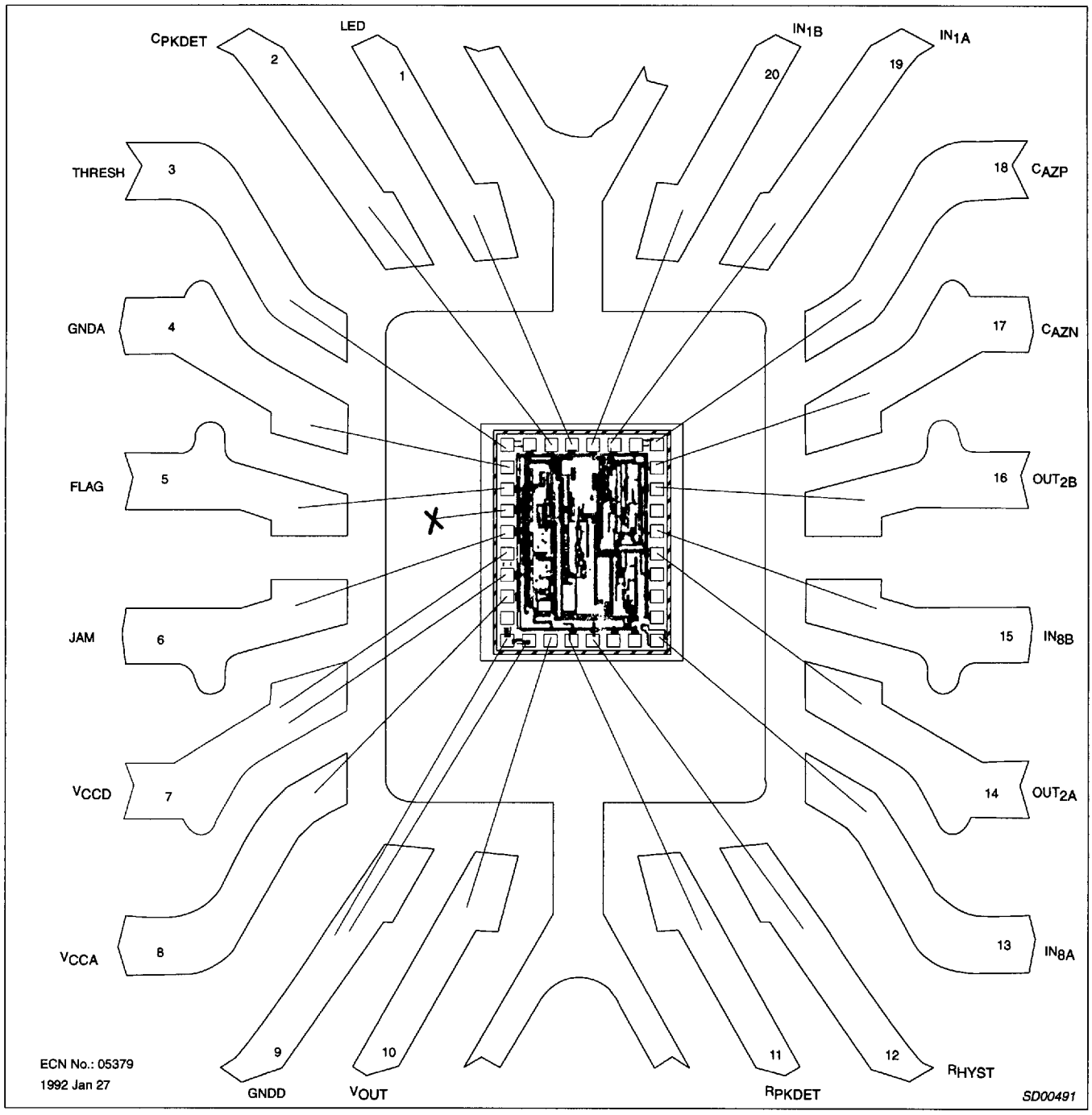
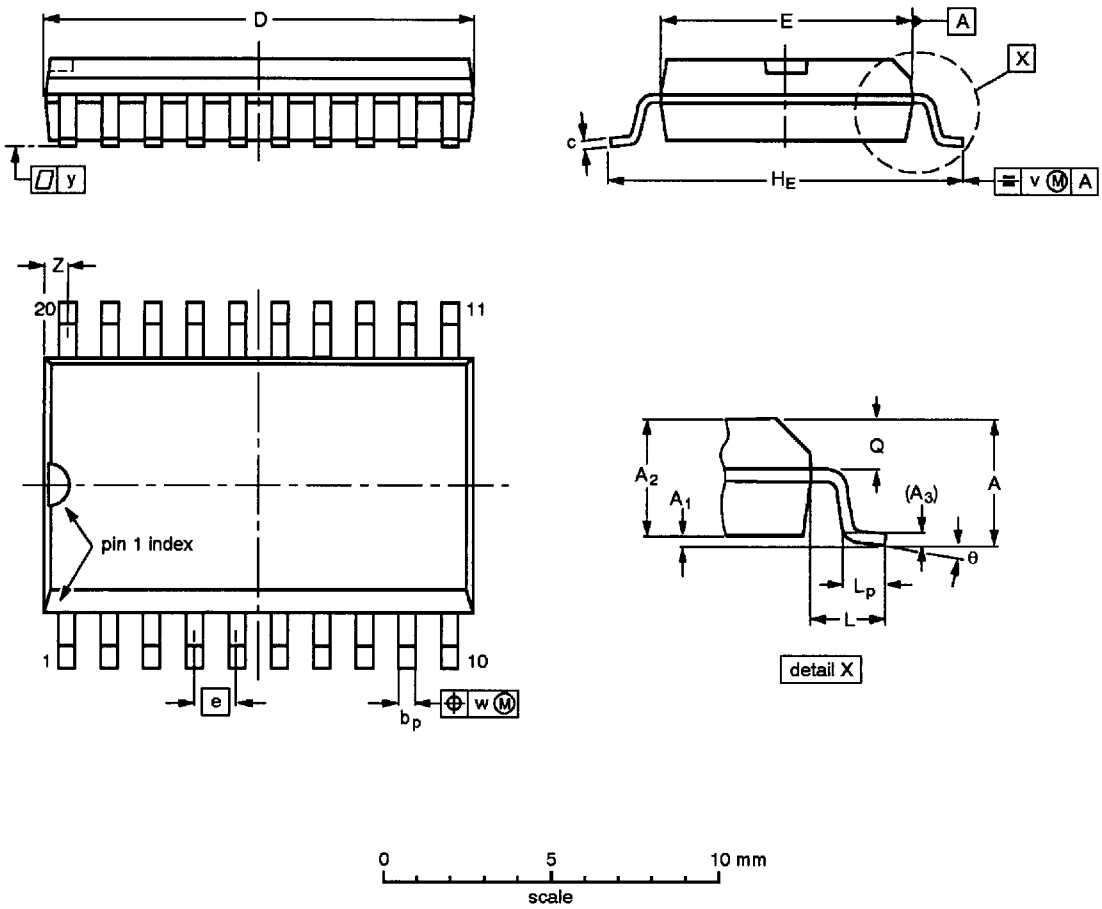


Figure 3. NE/SA5217 Bonding Diagram

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24