DATA SHEET

NE/SA5224
FDDI fiber optic postamplifier

Product specification

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Philips Semiconductors

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FDDI fiber optic postamplifier | NE/SA5224

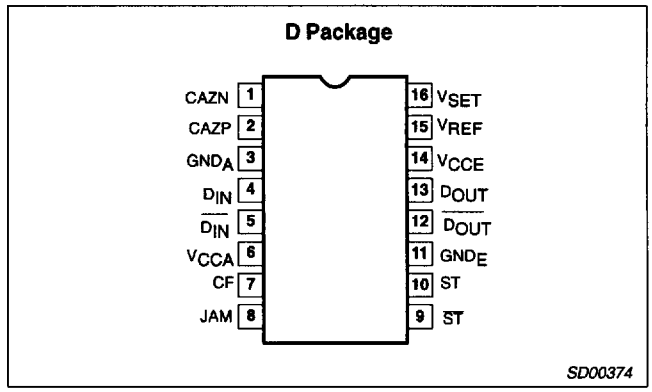
DESCRIPTION

The NE/SA5224 is a high-gain limiting amplifier that is designed to process signals from fiber optic preamplifiers. Capable of operating at 125Mb/s, the chip is FDDI compatible and has input signal level-detection with a user-adjustable threshold. The DATA and LEVEL-DETECT outputs are differential for optimum noise margin and ease of use. Also available is the NE/SA5225 which is an ECL 10K version of the NE/SA5224.

FEATURES

- Wideband operation: 1.0kHz to 120MHz typical
- Applicable in 155Mb/s OC3/SONET receivers
- Operation with single +5V or –5.2V supply
- Differential 100k ECL outputs
- Programmable input signal level-detection
- Fully differential for excellent PSRR to 1GHz

PIN DESCRIPTION



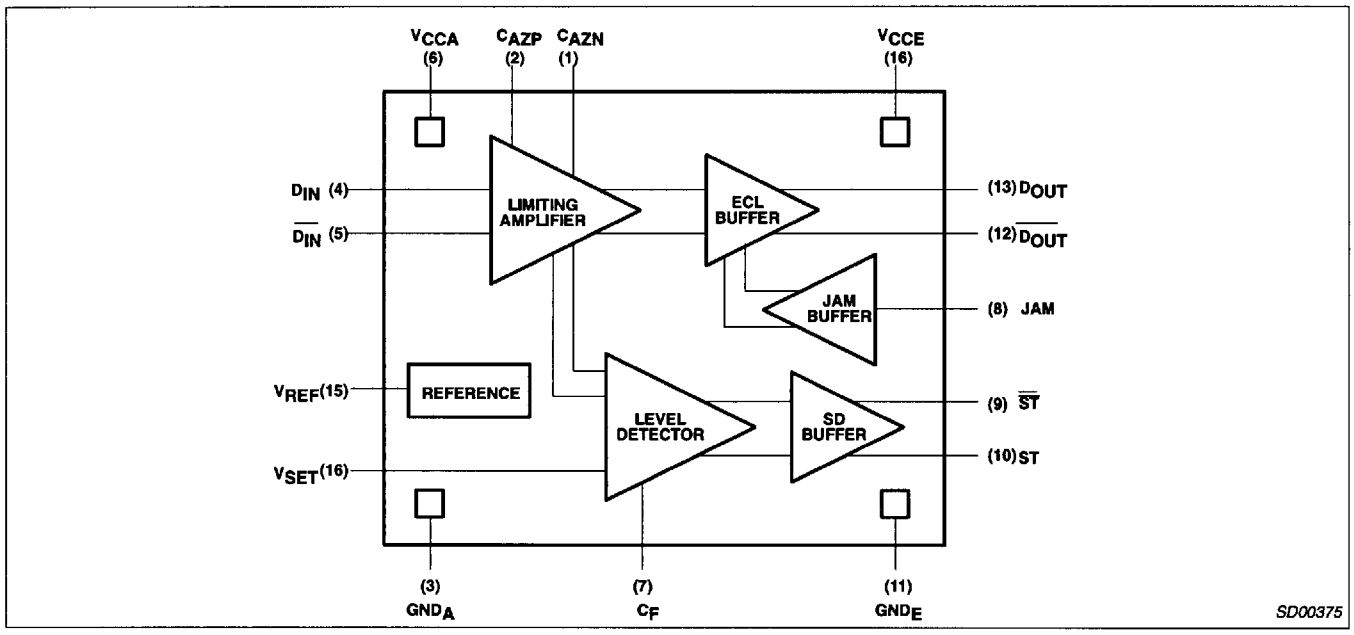
APPLICATIONS

- FDDI
- Data communication in noisy industrial environments
- LANs

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) package	0 to +70°C	NE5224D	SOT109-1
16-Pin Plastic Small Outline (SO) package	–40 to +85°C	SA5224D	SOT109-1

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NO.	NAME	FUNCTION
1	C_{AZN}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZP} will cancel the offset voltage of the limiting amplifier.
2	C_{AZP}	Auto-zero capacitor pin. Connecting a capacitor between this pin and C_{AZN} will cancel the offset voltage of the limiting amplifier.
3	GND_A	Analog GND pin. Connect to ground for +5V upshifted ECL operation. Connect to –5.2V for standard ECL operation. Must be at same potential as GND_E (Pin 11).
4	D_{IN}	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to $\overline{D_{IN}}$ (Pin 5).
5	$\overline{D_{IN}}$	Differential input. DC bias level is set internally at approximately 2.9V. Complimentary to D_{IN} (Pin 4).
6	V_{CCA}	Analog power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground for standard ECL operation. Must be at same potential as V_{CCE} (Pin 14).
7	C_F	Filter capacitor for level detector. Capacitor should be connected between this pin and V_{CCA}.
8	JAM	This ECL-compatible input controls the output buffers $\overline{D_{OUT}}$ and D_{OUT} (Pins 12 and 13). When an ECL LOW signal is applied, the outputs will follow the input signal. When an ECL HIGH signal is applied, the D_{OUT} and $\overline{D_{OUT}}$ pins will latch into LOW and HIGH states, respectively. When left unconnected, this pin is actively pulled-low (JAM OFF).
9	$\overline{ST}$	Input signal level-detect $\overline{STATUS}$. This ECL output is high when the input signal is below the user programmable threshold level.
10	ST	ECL compliment of $\overline{ST}$ (Pin 9).
11	GND_E	Digital GND pin. Connect to ground for +5V upshifted ECL operation. Connect to a negative supply for normal ECL operation. Must be at the same potential as GND_A (Pin 3).
12	$\overline{D_{OUT}}$	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL HIGH condition. Complimentary to D_{OUT} (Pin 13).
13	D_{OUT}	ECL-compatible output. Nominal level is V_{CCE}–1.3V. When JAM is HIGH, this pin will be forced into an ECL LOW condition. Complimentary to $\overline{D_{OUT}}$ (Pin 12).
14	V_{CCE}	Digital power supply pin. Connect to a +5V supply for upshifted ECL operation. Connect to ground during normal ECL operation. Must be at the same potential as V_{CCA} (Pin 6).
15	V_{REF}	Reference voltage for threshold level voltage divider. Nominal value is approximately 2.64V.
16	V_{SET}	Input threshold level setting circuit. This input can come from a voltage divider between V_{REF} and GND_A.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNITS
		NE	SA	
V_{CC}	Power supply (V_{CC} - GND)	6	6	V
T_A	Operating ambient	0 to +70	–45 to +85	°C
T_J	Operating junction	–55 to +150	–55 to +150	°C
T_{STG}	Storage	–65 to +150	–65 to +150	°C
P_D	Power dissipation, T_A = 25°C (still air)[1] 16-pin Plastic SO	1100	1100	mW

NOTE:
1. Maximum dissipation is determined by the ambient temperature and the thermal resistance, θ_{JA}: 16-pin SO: θ_{JA} = 110°C/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature ranges NE grade SA grade	 0 to +70 –40 to +85	 °C °C
T_J	Junction temperature ranges NE grade SA grade	 0 to +95 –40 to +110	 °C °C

DC ELECTRICAL CHARACTERISTICS

Min and Max limits apply over operating temperature at V_{CC} = 5V ±10%, unless otherwise specified. Typical data apply at T_A = 25°C and V_{CC} = +5V.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA5224			UNIT
			Min	Typ	Max	
V_{IN}	Input signal voltage single-ended differential		 .002 .004		 1.5 3.0	V_{P-P}
V_{OS}	Input offset voltage[2]				50	µV
V_N	Input RMS noise[2]				60	µV
V_{TH}	Input level-detect programmability single-ended	V_{IN} = 200kHz square wave	2		12	mV_{P-P}
V_{HYS}	Level-detect hysteresis		4	5	6	dB
I_{CC}	V_{CCA} + V_{CCE} supply current	No ECL loading		27	35	mA
I_{INL}	JAM input current	Pin 8 = 0V	–10		10	µA
V_{OHMAX}	Maximum logic high[1]				–0.880	V_{DC}
V_{OHMIN}	Minimum logic high[1]		–1.055			V_{DC}
V_{OLMAX}	Maximum logic low[1]				–1.620	V_{DC}
V_{OLMIN}	Minimum logic low[1]		–1.870			V_{DC}
V_{IH}	Minimum input for JAM = high[1]		–1.165			V_{DC}
V_{IL}	Maximum input for JAM = low[1]				–1.490	V_{DC}

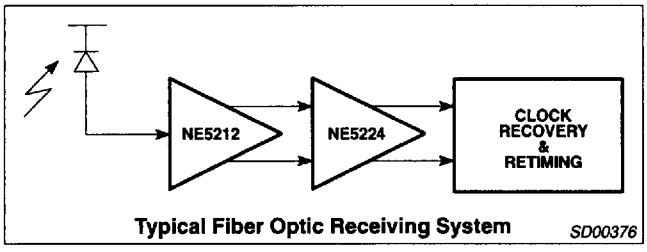
NOTES:
1. These ECL specifications are referenced to the V_{CCE} rail and apply for T_A = 0°C to 85°C.
2. Guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

Typical data apply at T_A = 25°C and V_{CC} = +5V. Min and Max limits apply for 4.5 ≤ V_{CC} ≤ 5.5V and specified NE or SA temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA5224			UNIT
			Min	Typ	Max	
BW_1	Lower –3dB bandwidth	C_{AZ} = 0.1µF	0.5	1.0	1.5	kHz
BW_2	Upper –3dB bandwidth		90	120	150	MHz
R_{IN}	Input resistance	Pin 4 or 5	2.9	4.5	7.6	kΩ
C_{IN}	Input capacitance	Pin 4 or 5			2.5	pF
t_r, t_f	ECL output[3] risetime, falltime	R_L = 50Ω To V_{CCE} - 2V 20-80%	1.2		2.2	ns
t_{PWD}	Pulsewidth distortion				0.3	ns_{P-P}
R_{AZ}	Auto zero output resistance	Pin 1 or 2	155	250	423	kΩ
R_F	Level-detect filter resistance	Pin 7	14	24	41	kΩ
t_{LD}	Level-detect time constant	C_F = 0	0.5	1.0	2.0	µs

NOTES:
1. Both outputs should be terminated identically to minimize differential feedback to the device inputs on a PC board or substrate.



Typical Fiber Optic Receiving System

INPUT BIASING

The DATA INPUT pins (4 and 5) are DC biased at approximately 2.9V by an internal reference generator. The NE5224 can be DC coupled, but the driving source must operate within the allowable 1.4V to 4.4V input signal range (for V_{CC} = 5V). If AC coupling is used to remove any DC compatibility requirement, the coupling capacitors C1 and C2 must be large enough to pass the lowest input frequency of interest. For example, .001µF coupling capacitors react with the internal 4.5k input bias resistors to yield a lower –3dB frequency of 35kHz. This then sets a limit on the maximum number of consecutive "1"s or "0"s that can be sensed accurately at the system data rate. Capacitor tolerance and resistor variation (2.9k to 7.6k) must be included for an accurate calculation.

AUTO-ZERO CIRCUIT

Figure 1 also shows the essential details of the auto-zero circuit. A feedback amplifier (A4) is used to cancel the offset voltage of the forward signal path, so the input to the internal ECL comparator (A6) is at its toggle point in the absence of any input signal. The time constant of the cancelling circuitry is set by an external capacitor (C_{AZ}) connected between Pins 1 and 2. The formula for the lower –3dB frequency is:

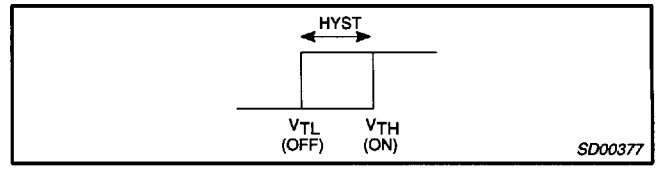
$$f_{-3dB} = \frac{150}{2\pi \cdot R_{AZ} \cdot C_{AZ}}$$

where R_{AZ} is the internal driving impedance which can vary from 155k to 423k over temperature and device fabrication limits. The input coupling time constant must also be considered in determining the lower frequency response of the NE5224.

INPUT SIGNAL LEVEL-DETECTION

The NE5224 allows for user programmable input signal level-detection and can automatically disable the switching of its ECL data outputs if the input is below a set threshold. This prevents the outputs from reacting to noise in the absence of a valid input signal, and insures that data will only be transmitted when the input signal-to-noise ratio is sufficient for low bit-error-rate system operation. Complimentary ECL flags (ST and STB) indicate whether the input signal is above or below the desired threshold level.

Figure 2 shows a simplified block diagram of the NE5224 level-detect system. The input signal is amplified and rectified before being compared to a programmable reference. A filter is included to prevent noise spikes from triggering the level-detector. This filter has a nominal 1µs time constant, and additional filtering can be achieved by using an external capacitor (CF) from Pin 7 to V_{CCA} (the internal driving impedance is nominally 24k). The resultant signal is then compared to a programmable level, V_{SET}, which is set by an internal voltage reference (2.64V) and an external resistor divider (R1 and R2). The value of R1 + R2 should be maintained at approximately 5k.



The circuit is designed to operate accurately over a differential 2-12mV_{P-P} square-wave input level detect range. This level, $V_{SET}/100$, is the average of V_{TH} and V_{TL}.

Nominal hysteresis of 5dB is provided by the complimentary ECL output comparator yielding $V_{TL} = \frac{V_{SET}}{139}$ and $V_{TH} = \frac{V_{SET}}{78}$. For example, with V_{SET} = 1.2V, a 15.4mV_{P-P} square-wave differential input will drive the ST pin high, and an input level below 8.6mV_{P-P} will drive the ST pin low.

Since a "JAM" function is provided (Pin 8) and can force the data outputs to a predetermined state (D_{OUT} = LOW, $\overline{D_{OUT}}$ = HIGH), the $\overline{ST}$ and JAM pins can be connected together to automatically disable signal transmission when the chip senses that the input signal is below the desired threshold. JAM (Pin 8) low enables the Data Outputs. $\overline{ST}$ will be in a high ECL state for input signals below threshold.

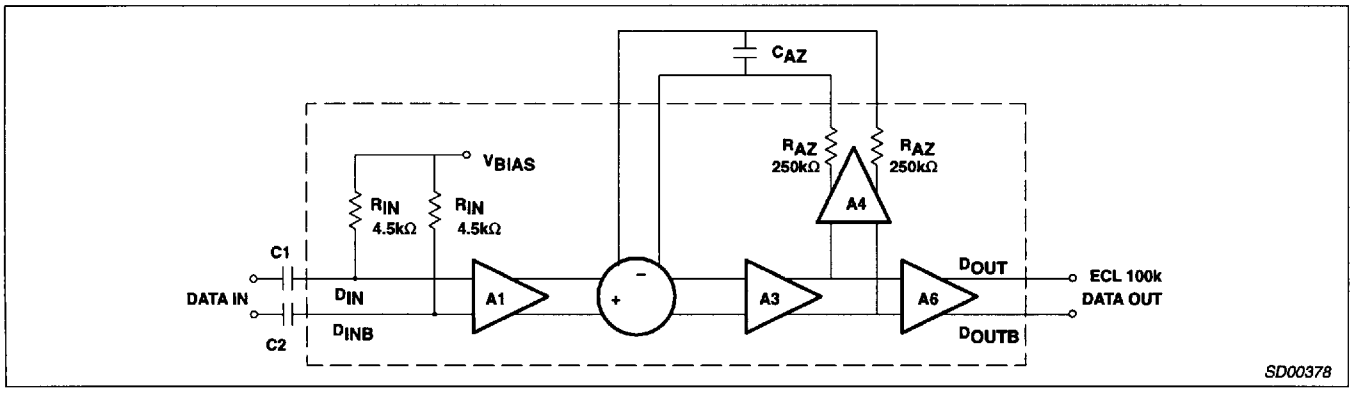


Figure 1. NE5224 Forward Gain Path Including Auto-Zero

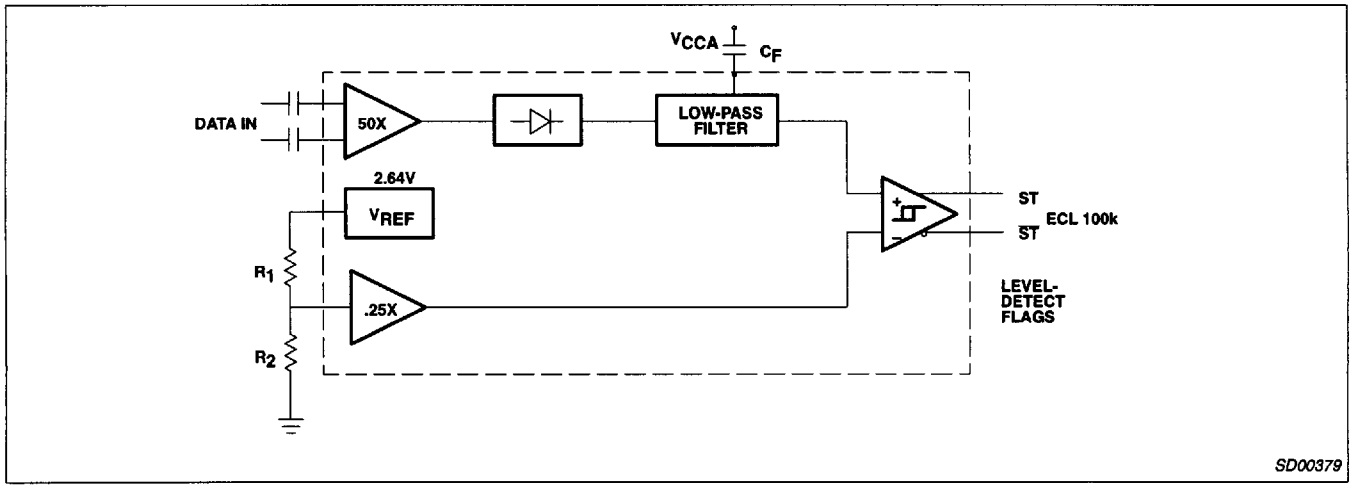


Figure 2. NE5224 Input Signal Level-Detect System

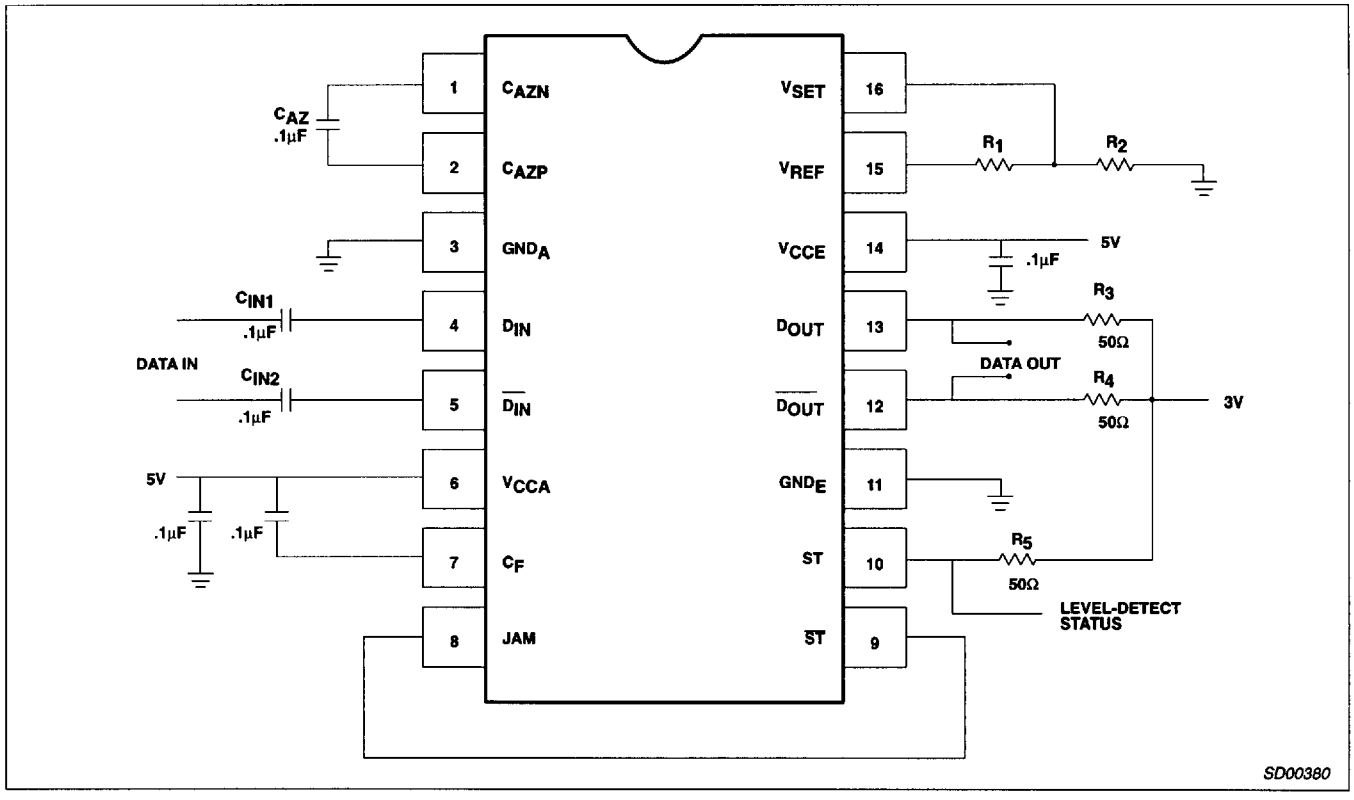


Figure 3. Application with V_{CC} = 5.0V

NOTE: A 50Ω resistor is required from Pin 9 to 3V only if the $\overline{ST}$ pin is required to meet 100k ECL specifications.

Die Sales Disclaimer

Due to the limitations in testing high frequency and other parameters at the die level, and the fact that die electrical characteristics may shift after packaging, die electrical parameters are not specified and die are not guaranteed to meet electrical characteristics (including temperature range) as noted in this data sheet which is intended only to specify electrical characteristics for a packaged device.

All die are 100% functional with various parametrics tested at the wafer level, at room temperature only (25°C), and are guaranteed to be 100% functional as a result of electrical testing to the point of wafer sawing only. Although the most modern processes are utilized for wafer sawing and die pick and place into waffle pack carriers, it is impossible to guarantee 100% functionality through this process. There is no post waffle pack testing performed on individual die.

Since Philips Semiconductors has no control of third party procedures in the handling or packaging of die, Philips Semiconductors assumes no liability for device functionality or performance of the die or systems on any die sales.

Although Philips Semiconductors typically realizes a yield of 85% after assembling die into their respective packages, with care customers should achieve a similar yield. However, for the reasons stated above, Philips Semiconductors cannot guarantee this or any other yield on any die sales.

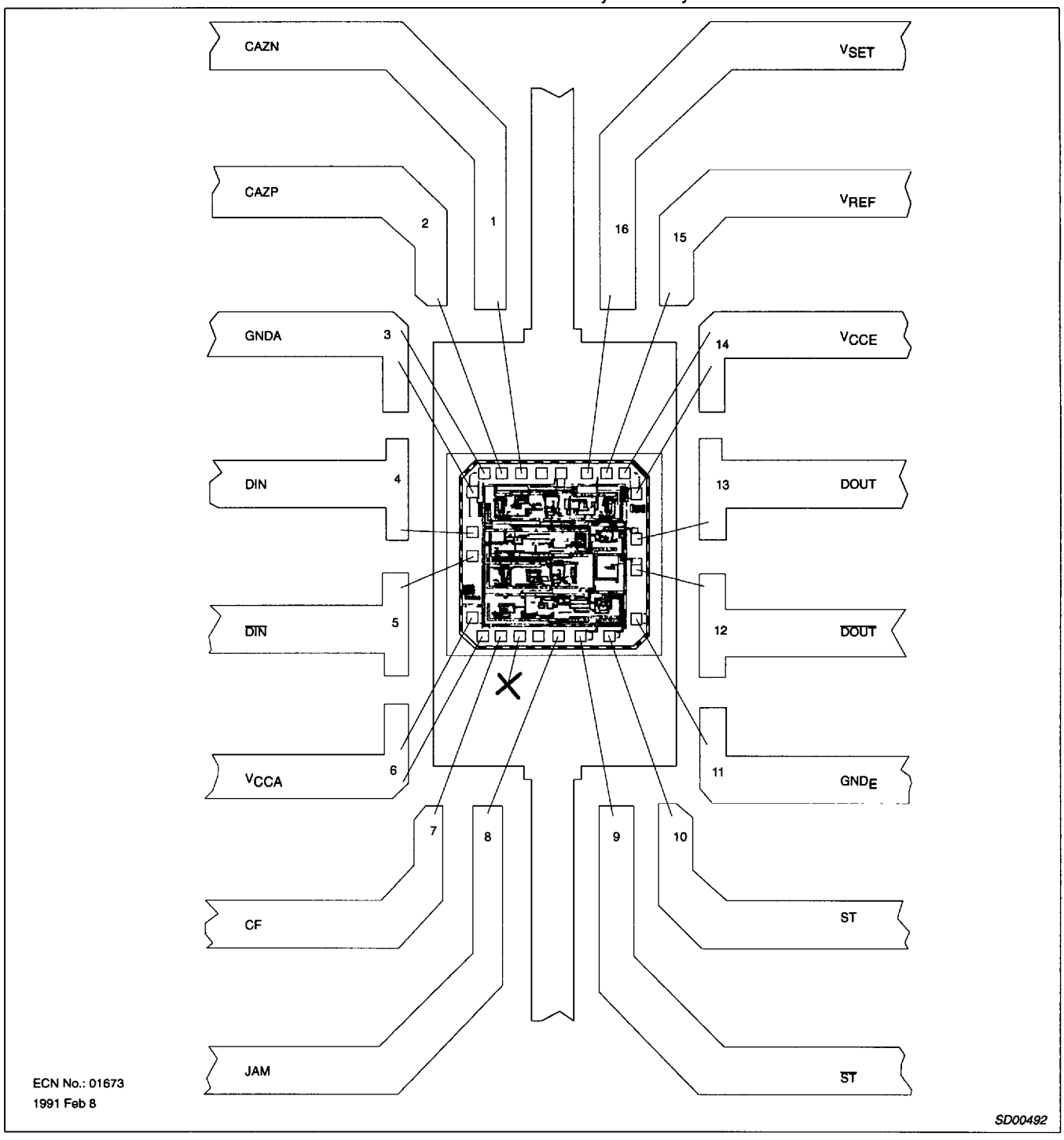
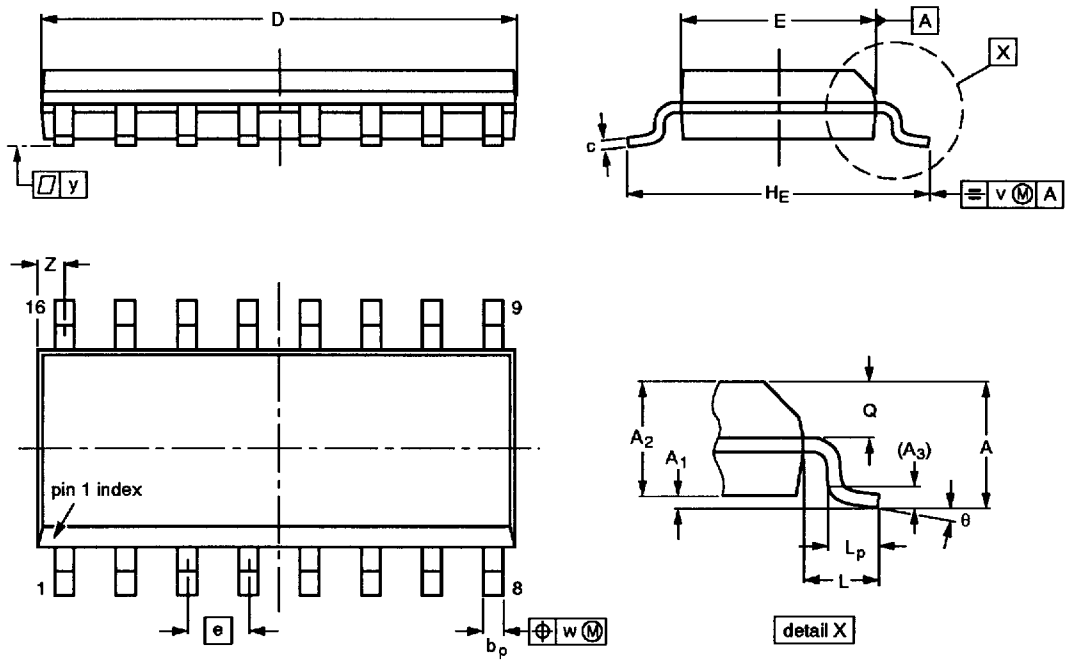
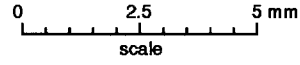


Figure 4. NE/SA5224 Bonding Diagram

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23