

Single pole double throw (SPDT) switch

NE/SA630

DESCRIPTION

The NE630 is a wideband RF switch fabricated in BiCMOS technology and incorporating on-chip CMOS/TTL compatible drivers. Its primary function is to switch signals in the frequency range DC - 1GHz from one 50Ω channel to another. The switch is activated by a CMOS/TTL compatible signal applied to the enable channel 1 pin (ENCH1).

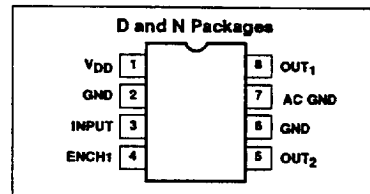
The extremely low current consumption makes the NE/SA630 ideal for portable applications. The excellent isolation and low loss makes this a suitable replacement for PIN diodes.

The NE/SA630 is available in an 8-pin dual in-line plastic package and an 8-pin SO (surface mounted miniature) package.

FEATURES

- Wideband (DC - 1GHz)
- Low through loss (1dB typical at 200MHz)
- Unused input is terminated internally in 50Ω
- Excellent overload capability (1dB gain compression point +18dBm at 300MHz)
- Low DC power (170μA from 5V supply)
- Fast switching (20ns typical)
- Good isolation (off channel isolation 60dB at 100MHz)
- Low distortion (IP₃ intercept +33dBm)
- Good 50Ω match (return loss 18dB at 400MHz)
- Full ESD protection
- Bidirectional operation

PIN CONFIGURATION



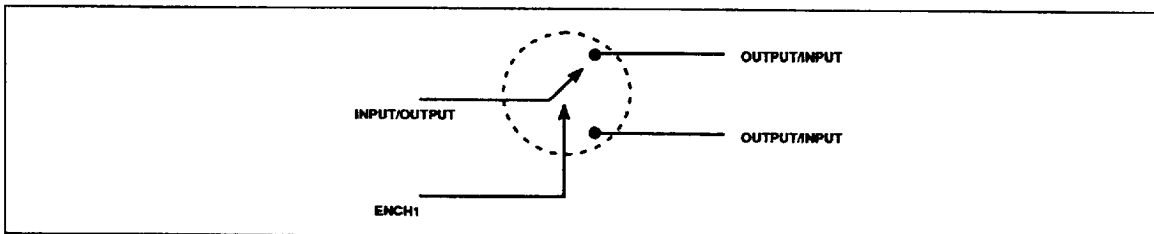
APPLICATIONS

- Digital transceiver front-end switch
- Antenna switch
- Filter selection
- Video switch
- FSK transmitter

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to 70°C	NE630N
8-Pin Plastic SO (Surface-mount)	0 to 70°C	NE630D
8-Pin Plastic DIP	-40 to +85°C	SA630N
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA630D

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V _{DD}	Supply voltage	-0.5 to +5.5	V
P _D	Power dissipation, T _A = 25°C (still air) ¹ 8-Pin Plastic DIP 8-Pin Plastic SO	1160 780	mW mW
T _{JMAX}	Maximum operating junction temperature	150	°C
P _{MAX}	Maximum power input/output	+20	dBm
T _{STG}	Storage temperature range	-65 to +150	°C

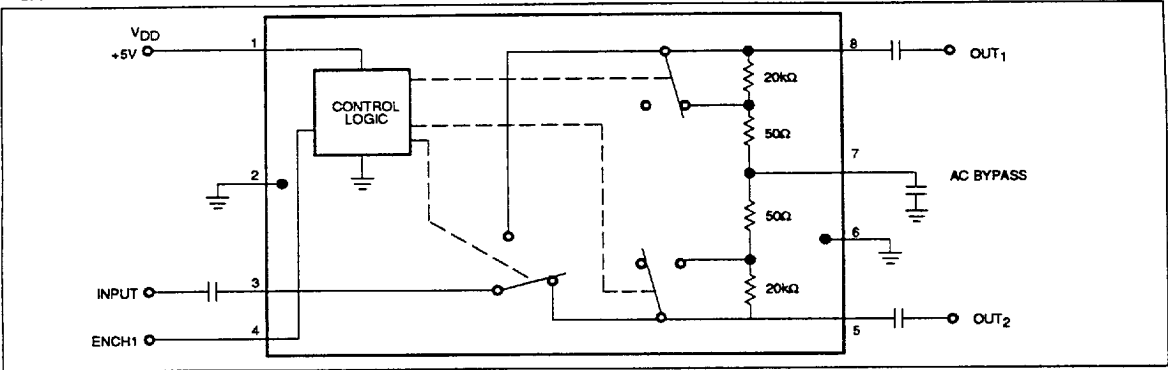
NOTES:

- Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, θ_{JA}:
8-Pin DIP: θ_{JA} = 108°C/W
8-Pin SO: θ_{JA} = 158°C/W

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EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNITS
V _{DD}	Supply voltage	3.0 to 5.5V	V
T _A	Operating ambient temperature range NE Grade SA Grade	0 to +70 -40 to +85	°C °C
T _J	Operating junction temperature range NE Grade SA Grade	0 to +90 -40 to +105	°C °C

DC ELECTRICAL CHARACTERISTICS

V_{DD} = +5V, T_A = 25°C; unless otherwise stated

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA630			
			MIN	TYP	MAX	
I _{DD}	Supply current		40	170	300	μA
V _T	TTL/CMOS logic threshold voltage ¹		1.1	1.25	1.4	V
V _{IH}	Logic 1 level	Enable channel 1	2.0		V _{DD}	V
V _{IL}	Logic 0 level	Enable channel 2	-0.3		0.8	V
I _{IL}	ENCH1 input current	ENCH1 = 0.4V	-1	0	1	μA
I _{IH}	ENCH1 input current	ENCH1 = 2.4V	-1	0	1	μA

NOTE:

1. The ENCH1 input must be connected to a valid Logic Level for proper operation of the NE/SA630.

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AC ELECTRICAL CHARACTERISTICS¹ - D PACKAGE $V_{DD} = +5V$, $T_A = 25^\circ C$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA630			
			MIN	TYP	MAX	
S ₂₁ , S ₁₂	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2	2.8	dB
S ₂₁ , S ₁₂	Isolation (OFF channel) ²	10MHz 100MHz 500MHz 900MHz	70 24	80 60 50 30		dB
S ₁₁ , S ₂₂	Return loss (ON channel)	DC - 400MHz 900MHz		20 12		dB
S ₁₁ , S ₂₂	Return loss (OFF channel)	DC - 400MHz 900MHz		17 13		dB
t _D	Switching speed (on-off delay)	50% TTL to 90/10% RF		20		ns
t _r , t _f	Switching speeds (on-off rise/fall time)	90%/10% to 10%/90% RF		5		ns
	Switching transients			165		mV _{P-P}
P _{-1dB}	1dB gain compression	DC - 1GHz		+18		dBm
IP ₃	Third-order intermodulation intercept	100MHz		+33		dBm
IP ₂	Second-order intermodulation intercept	100MHz		+52		dBm
NF	Noise figure (Z _O = 50Ω)	100MHz 900MHz		1.0 2.0		dB

NOTE:

1. All measurements include the effects of the D package NE/SA630 Evaluation Board (see Figure 1B). Measurement system impedance is 50 Ω .
2. The placement of the AC bypass capacitor is critical to achieve these specifications. See the applications section for more details.

AC ELECTRICAL CHARACTERISTICS¹ - N PACKAGE $V_{DD} = +5V$, $T_A = 25^\circ C$; all other characteristics similar to the D-Package, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA630			
			MIN	TYP	MAX	
S_{21} , S_{12}	Insertion loss (ON channel)	DC - 100MHz 500MHz 900MHz		1 1.4 2.5		dB
S_{21} , S_{12}	Isolation (OFF channel)	10MHz 100MHz 500MHz 900MHz	58	68 50 37 15		dB
NF	Noise figure ($Z_0 = 50\Omega$)	100MHz 900MHz		1.0 2.5		dB

NOTE:

1. All measurements include the effects of the N package NE/SA630 Evaluation Board (see Figure 1C). Measurement system impedance is 50 Ω .

APPLICATIONS

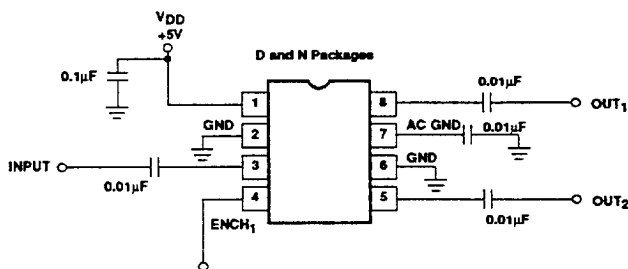
The typical applications schematic and printed circuit board layout of the NE/SA630 evaluation board is shown in Figure 1. The layout of the board is simple, but a few cautions need to be observed. The input and output traces should be 50 Ω . The placement of the AC bypass capacitor is *extremely*

critical if a symmetric isolation between the two channels is desired. The trace from Pin 7 should be drawn back towards the package and then be routed downwards. The capacitor should be placed straight down as close to the device as practical. For better isolation between the two channels at higher frequencies, it is also advisable to run the two

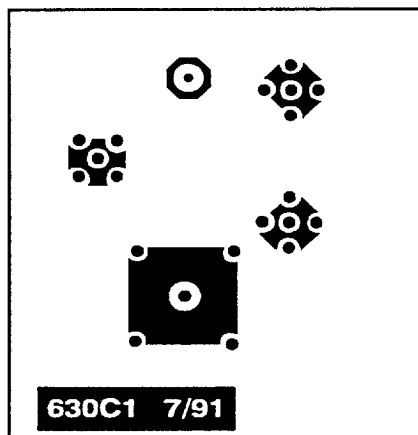
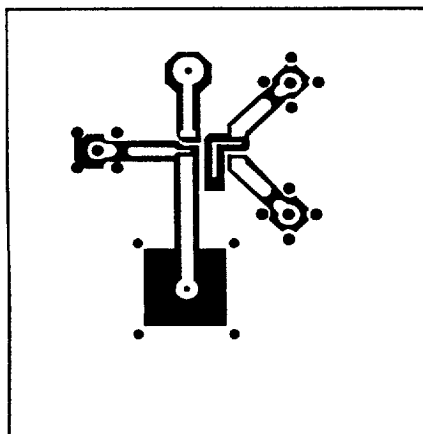
output/input traces at an angle. This also minimizes any inductive coupling between the two traces. The power supply bypass capacitor should be placed close to the device. Figure 7 shows the frequency response of the NE/SA630. The loss matching between the two channels is excellent to 1.2GHz as shown in

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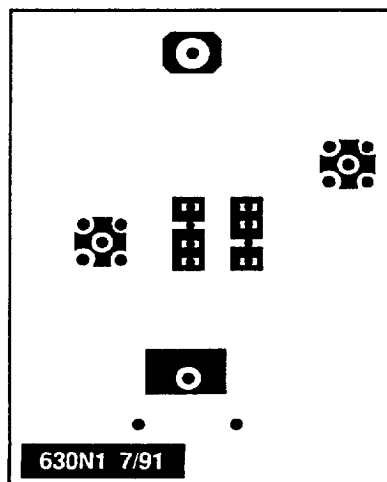
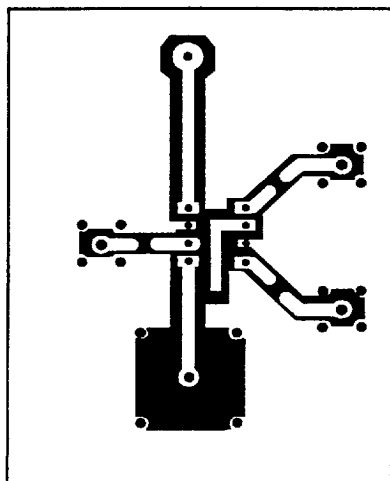
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a. NE/SA Evaluation Board Schematic



b. NE/SA630 D-Package Board Layout



c. NE/SA630 N-Package Board Layout

Figure 1

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Figure 10. The isolation and matching of the two channels over frequency is shown in Figure 12 and Figure 14, respectively.

The NE630 is a very versatile part and can be used in many applications. Figure 2 shows a block diagram of a typical Digital RF transceiver front-end. In this application the NE630 replaces the duplexer which is typically very bulky and lossy. Due to the low power consumption of the device, it is ideally suited for handheld applications such as in CT2 cordless telephones. The NE630 can also be used to generate Amplitude Shift Keying (ASK) or On-Off Keying (OOK) and Frequency Shift Keying (FSK) signals for digital RF communications systems. Block diagrams for these applications are shown in Figure 3 and Figure 4, respectively.

For applications that require a higher isolation at 1GHz than obtained from a single NE630, several NE630s can be cascaded as shown in Figure 5. The cascaded configuration will have a higher loss but greater than 35dB of isolation at 1GHz and greater than 65dB @ 500MHz can be obtained from this configuration. By modifying the enable control, an RF multiplexer/ de-multiplexer or antenna selector can be constructed. The simplicity of NE630 coupled with its ease of use and high performance lends itself to many innovative applications.

The NE/SA630 switch terminates the OFF channel in 50Ω. The 50Ω resistor is internal and is in series with the external AC bypass capacitor. Matching to impedances other than 50Ω can be achieved by adding a resistor in series with the AC bypass capacitor (e.g., 25Ω additional to match to a 75Ω environment).

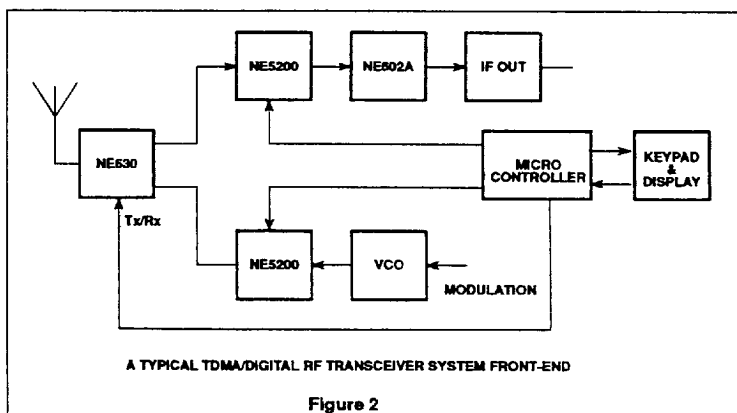


Figure 2

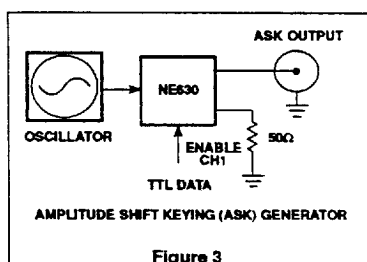


Figure 3

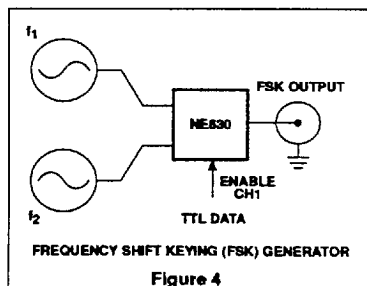


Figure 4

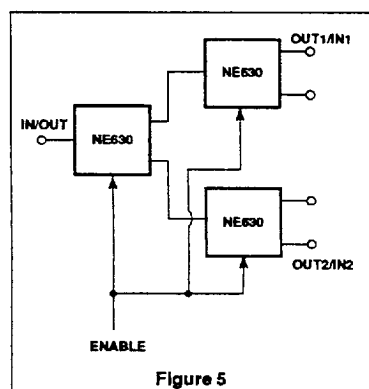


Figure 5

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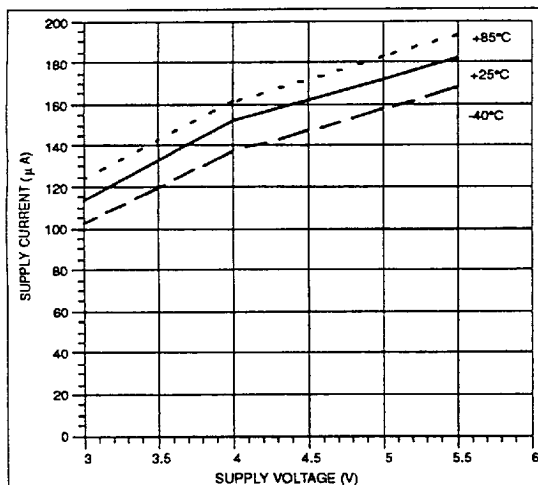
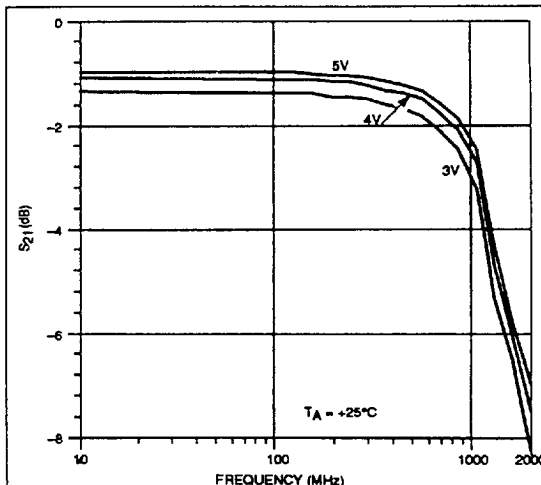
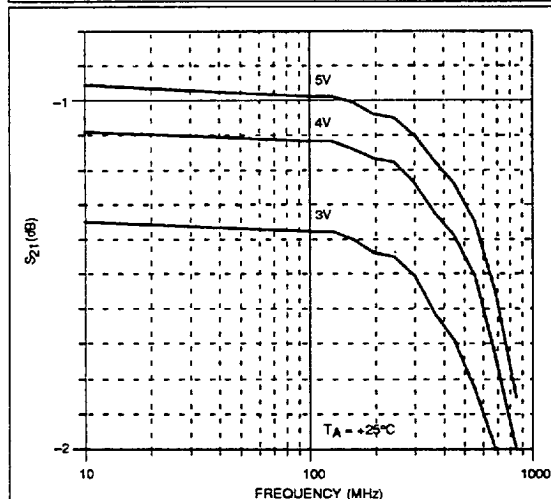
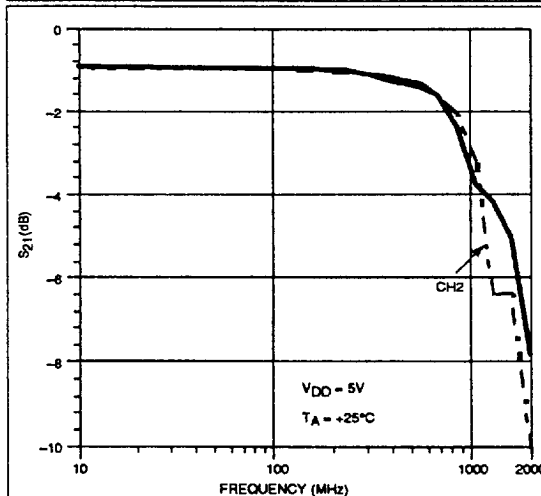
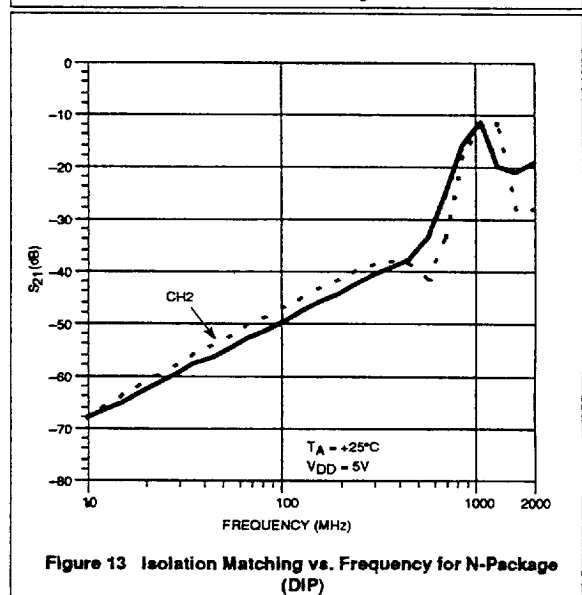
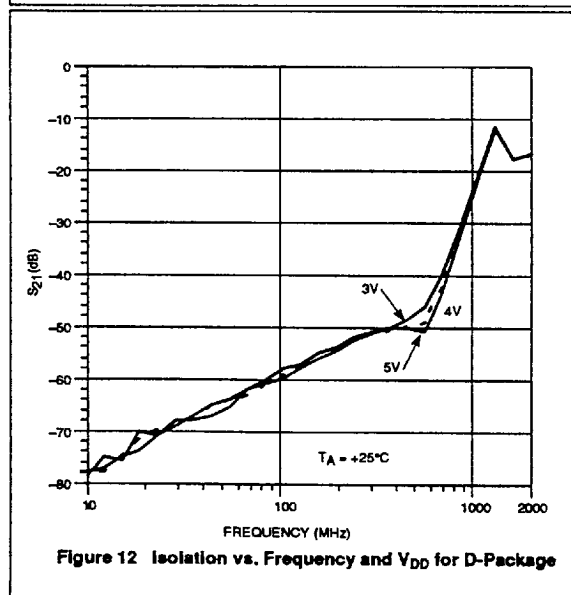
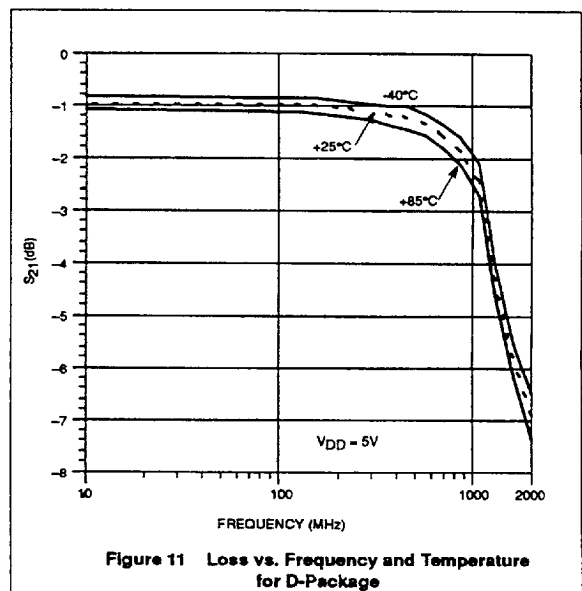
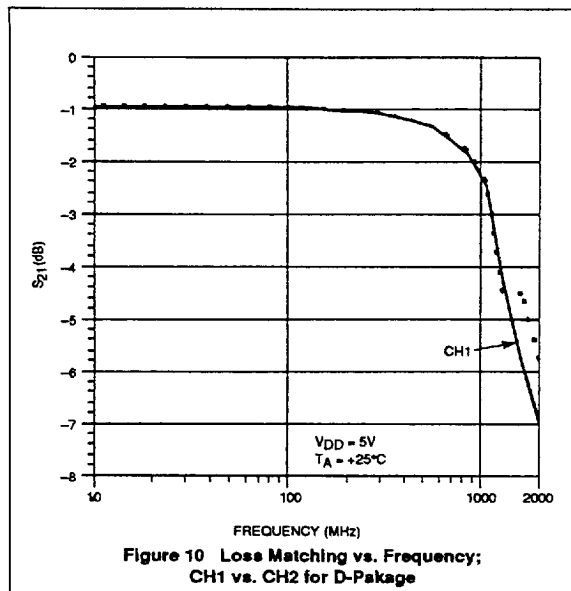
Figure 6 Supply Current vs. V_{DD} and TemperatureFigure 7 Loss vs. Frequency and V_{DD} for D-PackageFigure 8 Loss vs. Frequency and V_{DD} for D-Package
-Expanded Detail-

Figure 9 Loss Matching vs. Frequency for N-Package (DIP)

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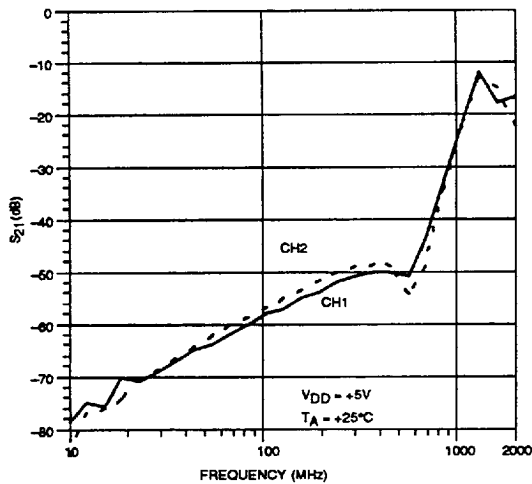


Figure 14 Isolation Matching vs. Frequency; CH1 vs. CH2 for D-Package

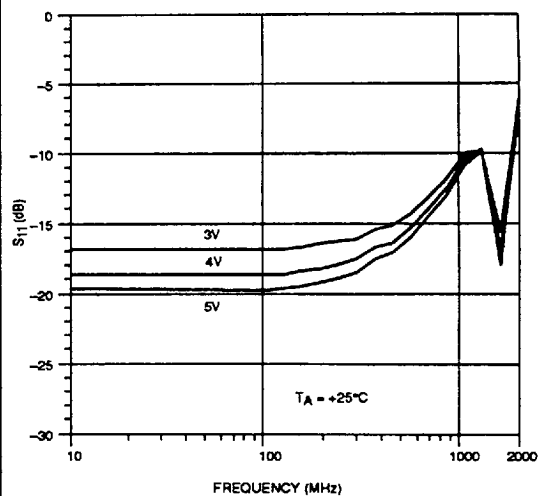


Figure 15 Input Match On-Channel vs. Frequency and V_{DD}

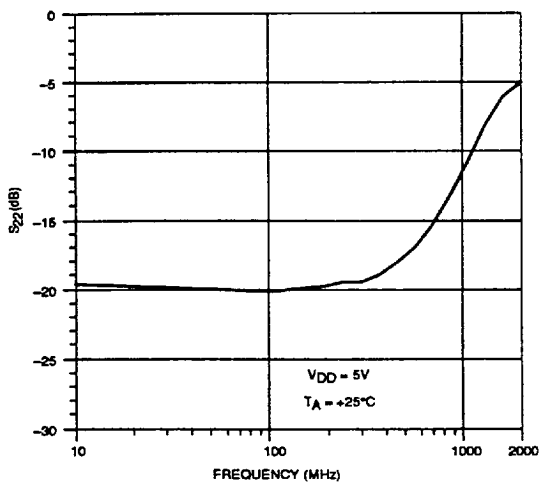


Figure 16 Output Match On-Channel vs. Frequency

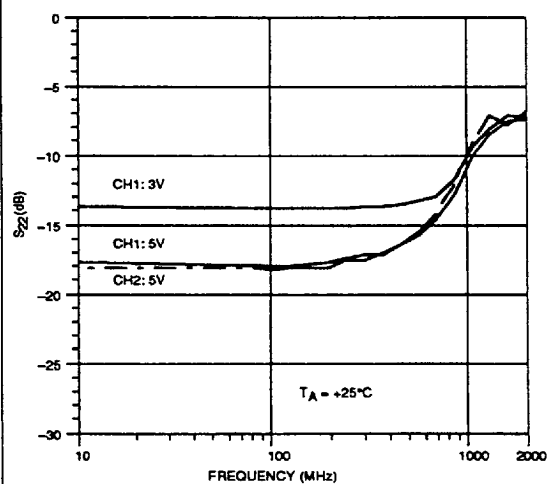


Figure 17 OFF-Channel Match vs. Frequency and V_{DD}

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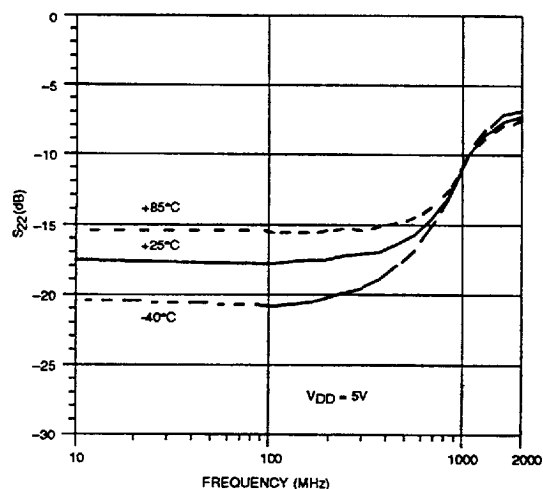
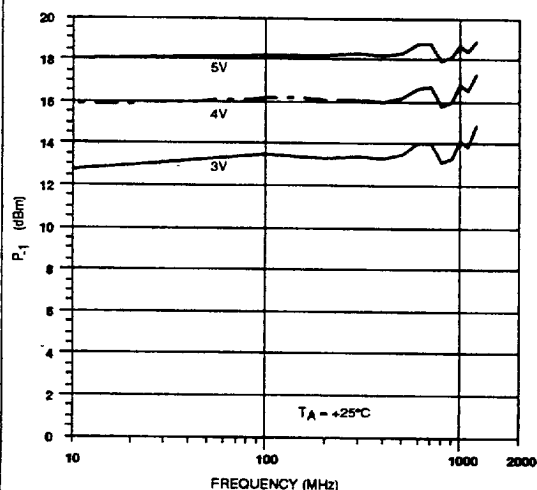
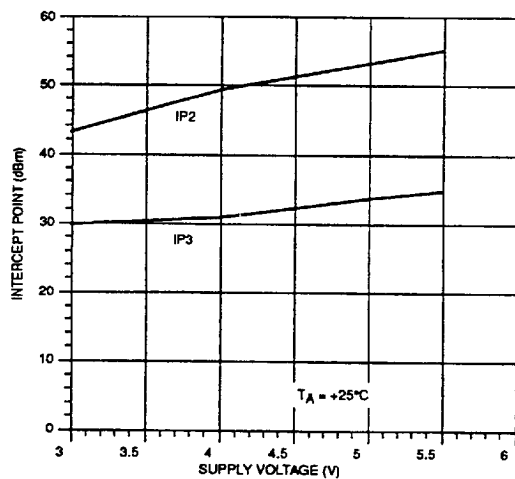
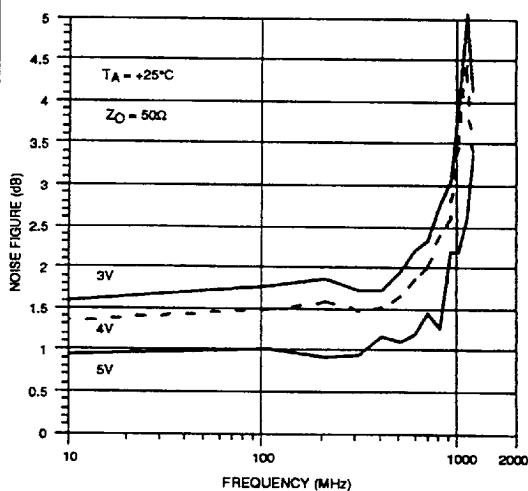
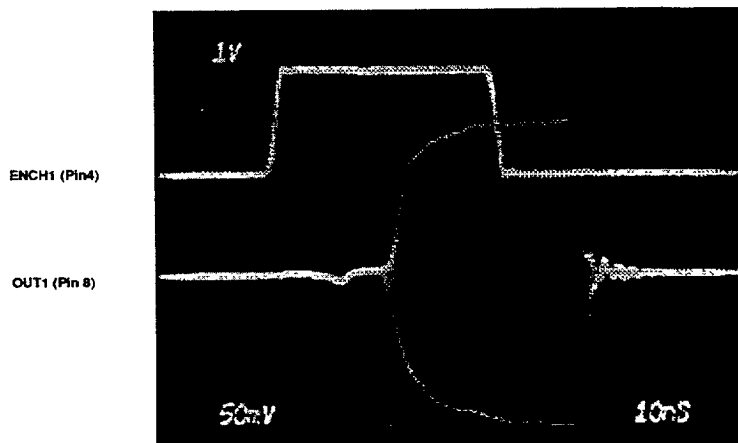


Figure 18 OFF Channel Match vs. Frequency and Temperature

Figure 19 P-1 dB vs. Frequency and V_{DD} Figure 20 Intercept Points vs. V_{DD} Figure 21 Noise Figure vs. Frequency and V_{DD}
for D-Package

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Figure 22 Switching Speed; $f_M = 100\text{MHz}$ at -6dBm , $V_{DD} = 5\text{V}$