



GAL22V10 Family

GAL18V10

GAL22V10

GAL26CV12

High-Performance E²CMOS®

FEATURES

- **HIGH PERFORMANCE E²CMOS[®] TECHNOLOGY**
 - 15 ns Maximum Propagation Delay
 - F_{max} = 50 MHz
 - TTL Compatible 8 - 16 mA Outputs
 - UltraMOS[®] III Advanced CMOS Technology
 - Internal Pull-Up Resistor on all Pins
- **50% REDUCTION IN POWER**
 - 75 - 90mA Typ I_{cc}
- **E² CELL TECHNOLOGY**
 - Reconfigurable Logic
 - Reprogrammable Cells
 - 100% Tested/Guaranteed 100% Yields
 - High Speed Electrical Erasure (<50ms)
 - 20 Year Data Retention
- **OUTPUT LOGIC MACROCELLS**
 - Maximum Flexibility for Complex Logic Designs
 - Uses the Standard 22V10 OLMC Architecture
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
 - 100% Functional Testability
- **APPLICATIONS INCLUDE:**
 - DMA Control
 - State Machine Control
 - High Speed Graphics Processing
 - Standard Logic Speed Upgrade
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

DESCRIPTION

T-46-13-27

The GAL22V10 Family of devices are high-speed, E²CMOS[®] PLDs built using the familiar 22V10 architecture. Three devices are offered in the GAL22V10 Family. They are the GAL18V10 (20-pin), GAL22V10 (24-pin), and the GAL26CV12 (28-pin). Each of these devices uses the industry standard 22V10 universal architecture which provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The devices differ in the number of I/Os, Pins, and Product Terms offered.

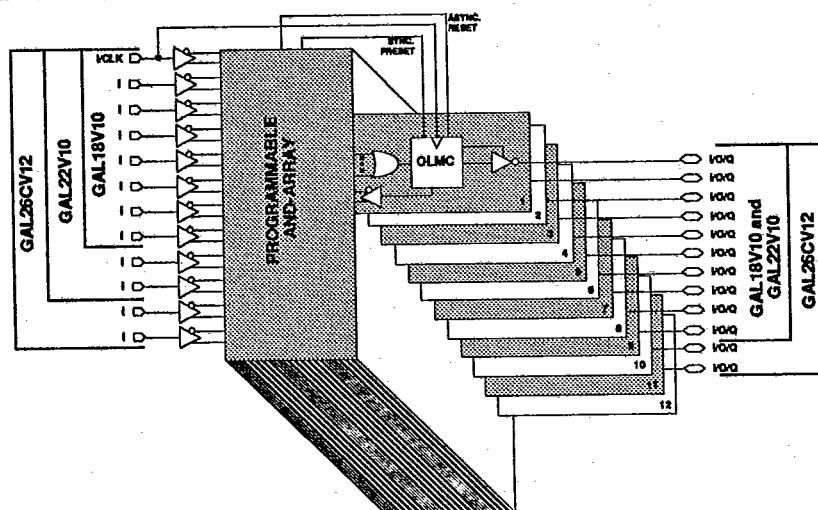
The GAL22V10 is a 24-pin device which contains twelve (12) dedicated input pins and ten (10) input/output pins. The device has a variable number of product terms per OLMC, ranging from eight (8) to sixteen (16) per output.

The GAL18V10 is a 20-pin version of the popular 22V10 device. The GAL18V10 provides design engineers with a smaller footprint and lower cost alternative to the 24-pin 22V10 device. The GAL18V10 contains eight (8) dedicated input pins and ten (10) input/output pins.

The GAL26CV12 is a 28-pin version of the 22V10 device. The GAL26CV12 features more inputs and outputs in order to provide greater functionality and increased I/O. The GAL26CV12 contains fourteen (14) dedicated input pins and twelve (12) input/output pins.

Electrically reprogrammable CMOS technology allows complete AC, DC, and functional testing of every GAL device. Therefore, LATTICE guarantees 100% field programmability and functionality of all GAL products. LATTICE also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

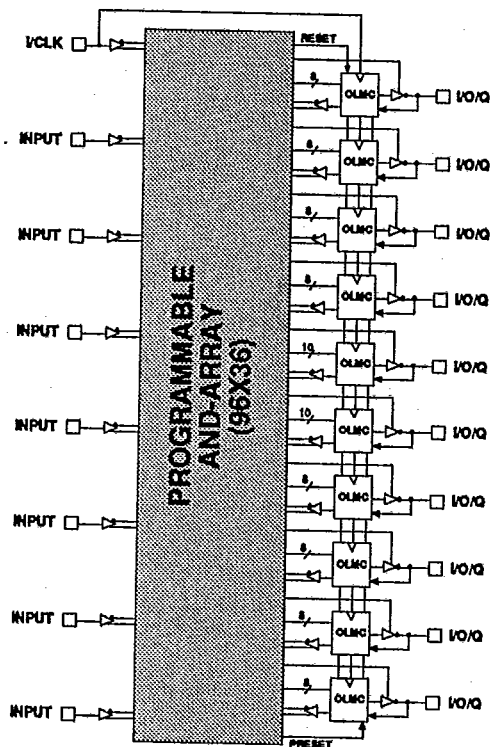
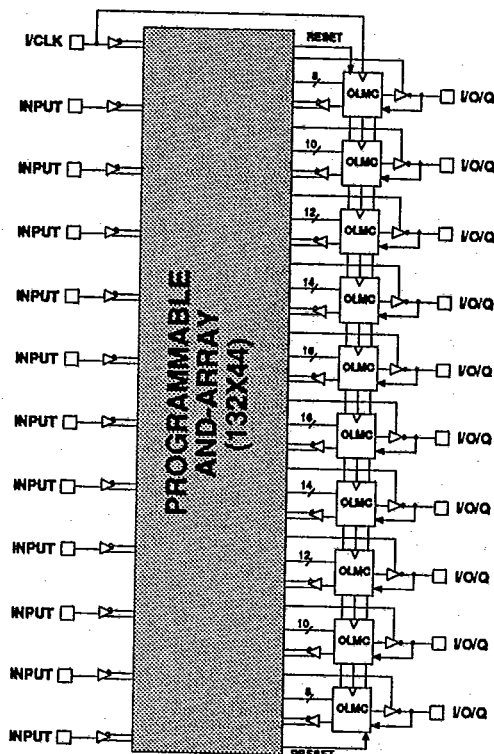
BLOCK DIAGRAM: GAL18V10, 22V10, and 26CV12



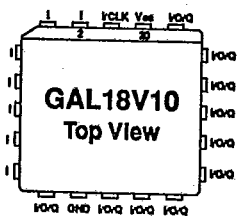
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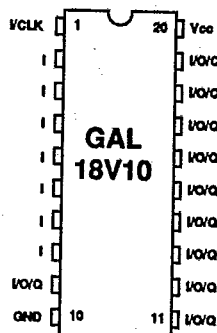
March 1990

Specifications **GAL22V10 Family****GAL18V10 BLOCK DIAGRAM****GAL22V10 BLOCK DIAGRAM****GAL18V10 PIN DIAGRAMS**

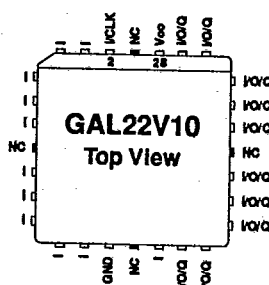
Chip Carrier



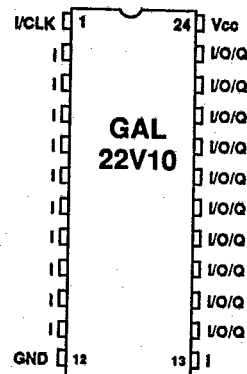
Skinny Dip

**GAL22V10 PIN DIAGRAMS**

Chip Carrier



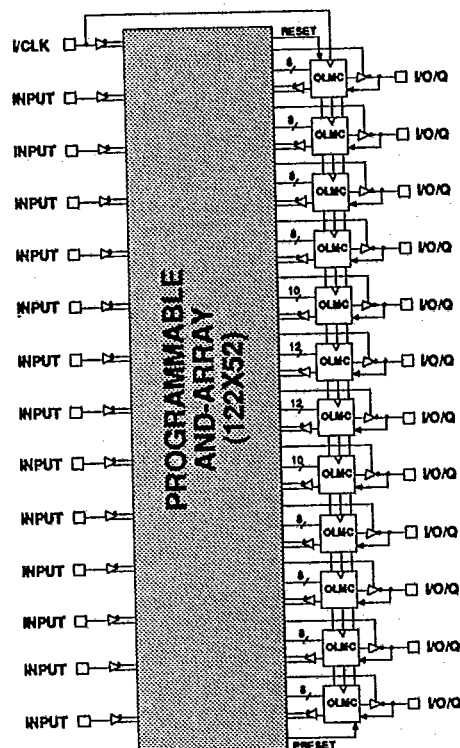
Skinny Dip





Specifications GAL22V10 Family

GAL26CV12 BLOCK DIAGRAM

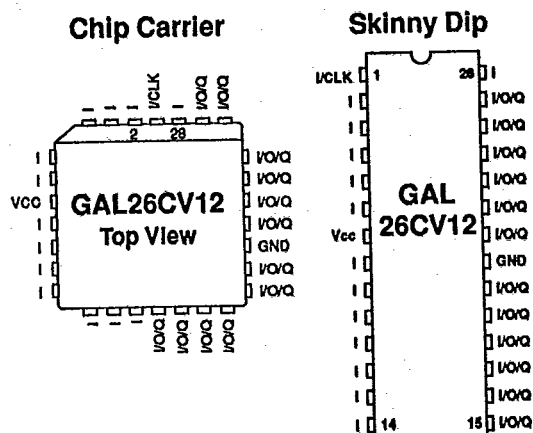


PRODUCT SELECTOR GUIDE

	COMMERCIAL TEMP.		
	GAL18V10	GAL22V10	GAL26CV12
Pins	20	24	28
Tpd (Max.)	15ns	15ns	15ns
Icc (Typ.)	75mA	90mA	90mA
Dedicated Inputs	8	12	14
Inputs/Outputs	10	10	12
Product Terms per macrocell	8-12	8-16	8-10
Technology	E ² CMOS	E ² CMOS	E ² CMOS

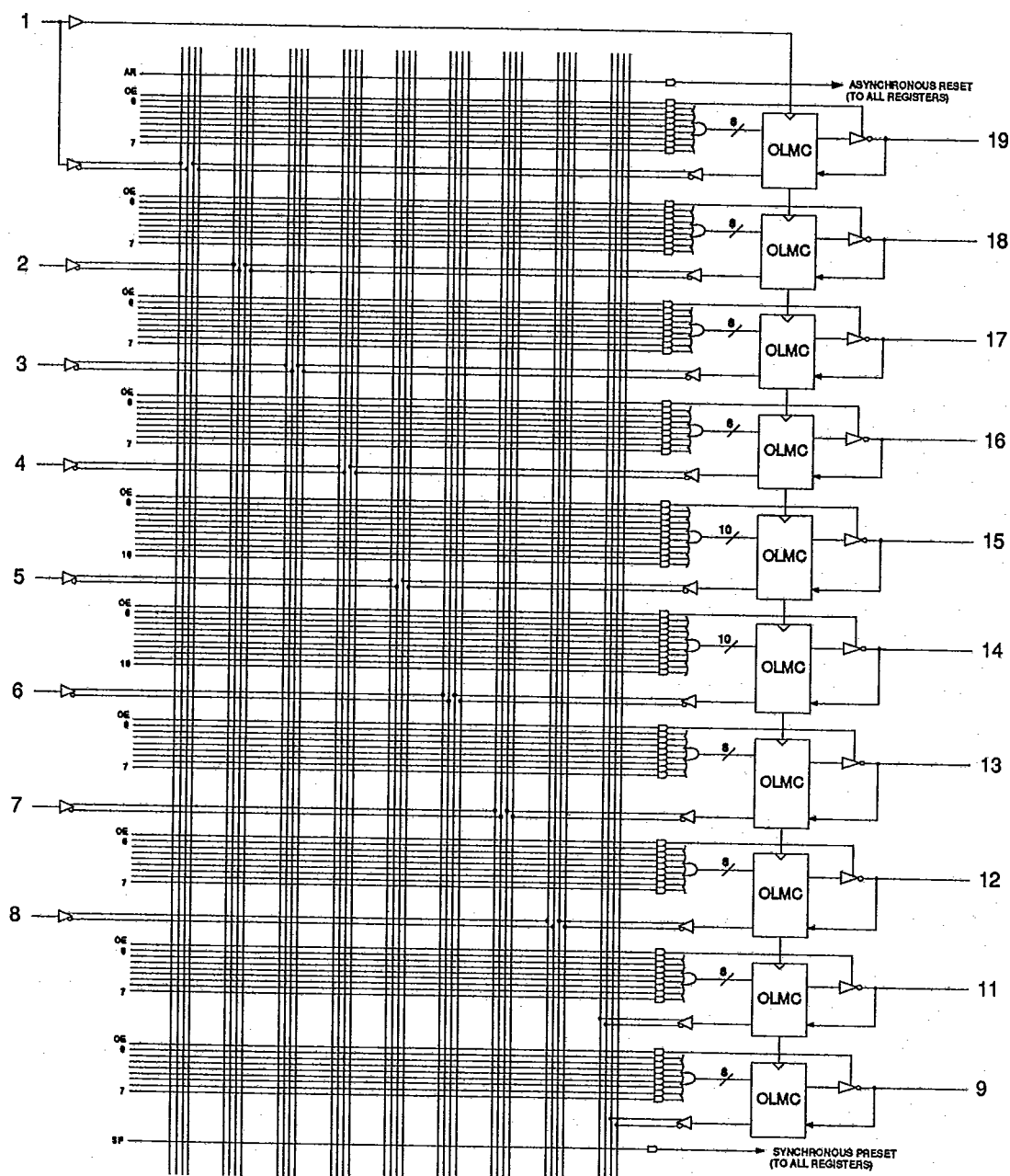
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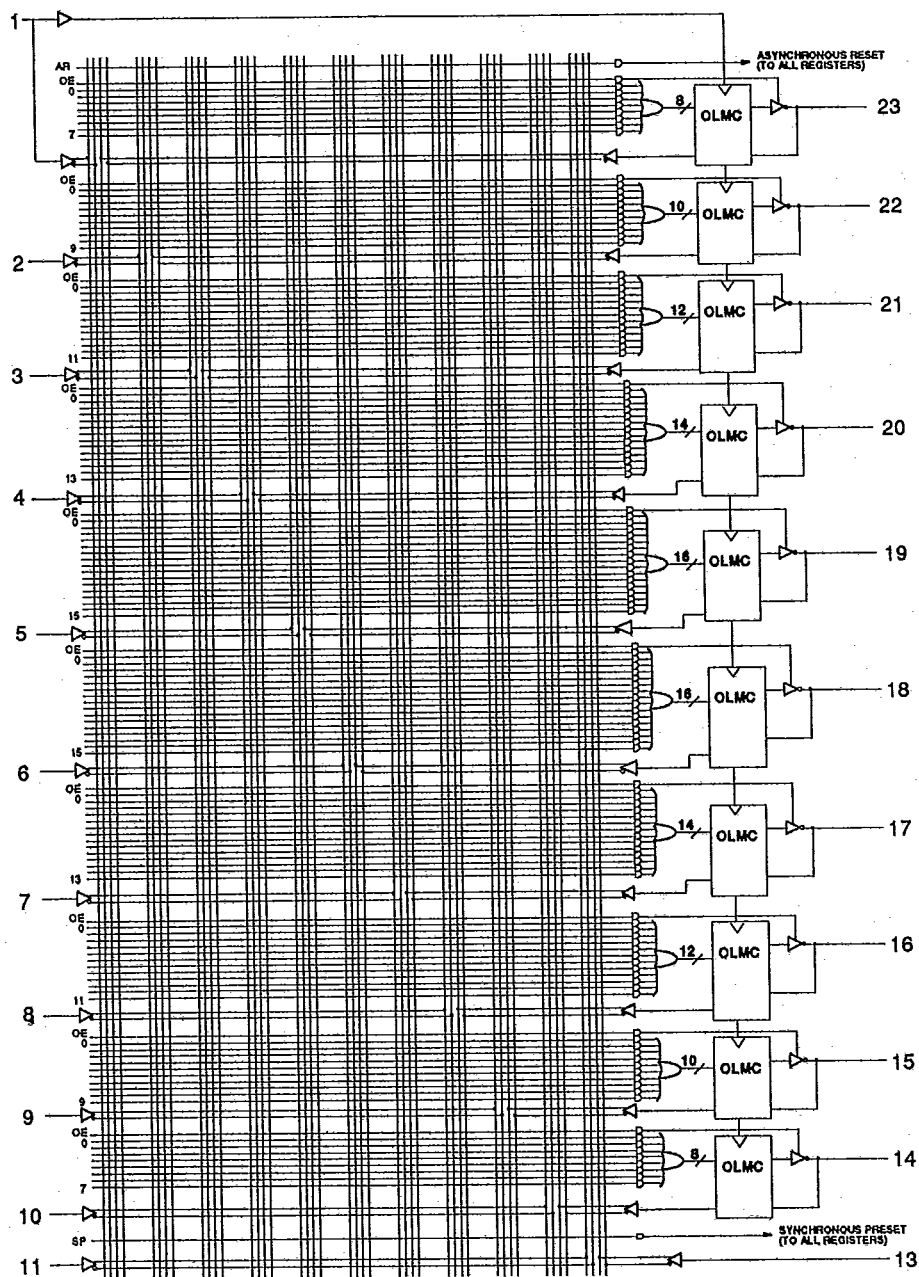
GAL26CV12 PIN DIAGRAMS



SPEED/GRADE SELECTOR GUIDE

	GRADE		
	Commercial	Industrial	Military
GAL18V10	15, 20ns	15, 20ns	15, 20ns
GAL22V10	15, 20, 25ns	15, 20, 25ns	15, 20, 30ns
GAL26CV12	15, 20ns	15, 20ns	15, 20ns
Vcc	5.00V ± 5%	5.00V ± 10%	5.00V ± 10%
Temperature	0->75°C	-40->85°C	-55->125°C
Packaging	Plastic DIP PLCC	Plastic DIP PLCC	CERDIP

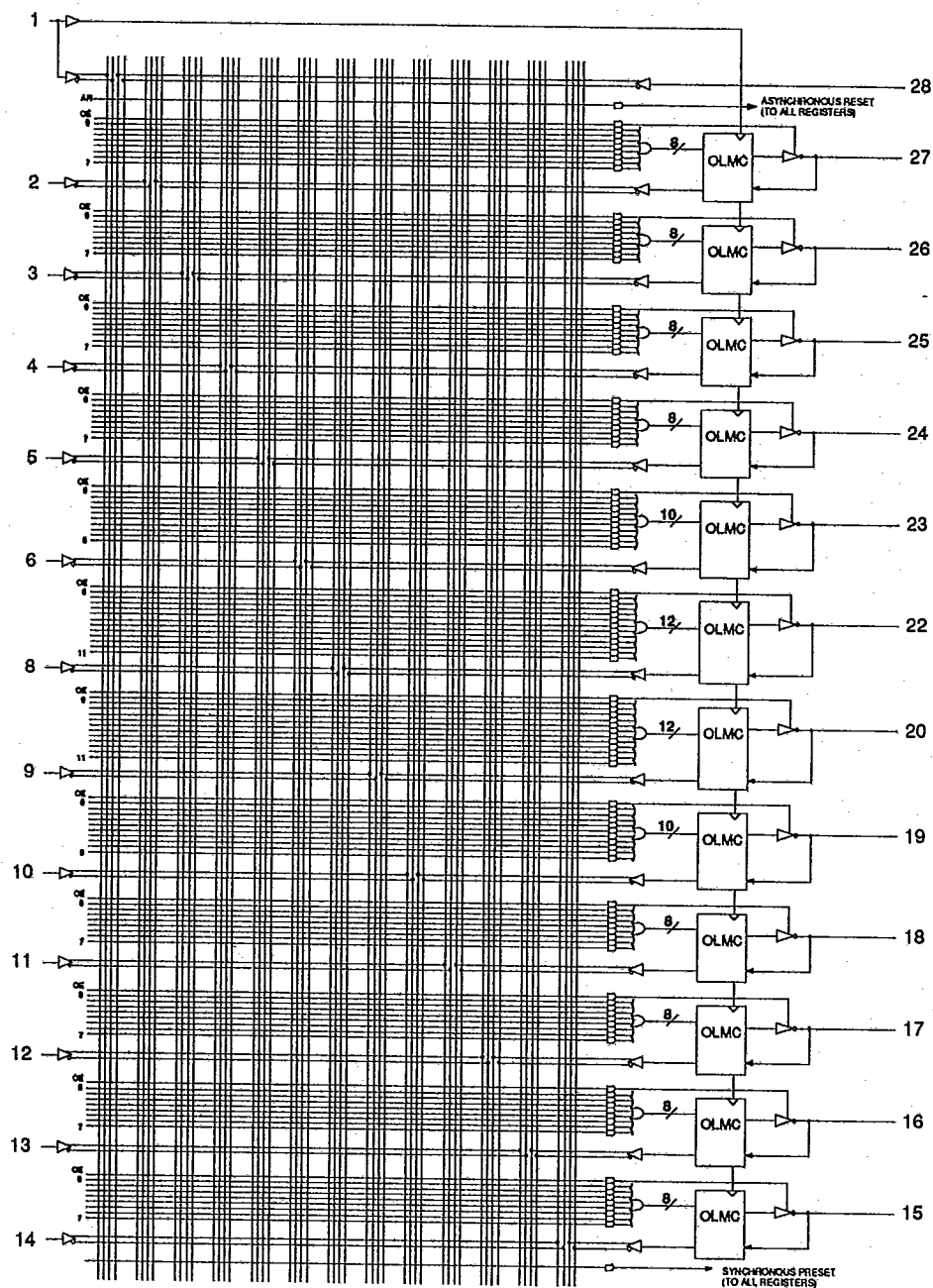
Specifications **GAL22V10 Family****GAL18V10 LOGIC DIAGRAM****GAL18V10**

Specifications **GAL22V10 Family****GAL22V10 LOGIC DIAGRAM****GAL22V10****2**

Specifications GAL22V10 Family

GAL26CV12 LOGIC DIAGRAM

GAL26CV12





Specifications GAL22V10 Family

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply voltage V_{CC} -5 to +7V
 Input voltage applied -2.5 to $V_{CC} + 1.0V$
 Off-state output voltage applied -2.5 to $V_{CC} + 1.0V$
 Storage Temperature -65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

2

SWITCHING TEST CONDITIONS

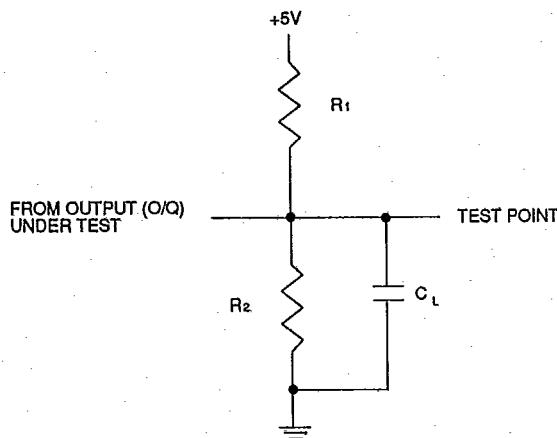
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% - 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.

	COMMERCIAL		INDUSTRIAL		MILITARY	
	R_1	R_2	R_1	R_2	R_1	R_2
GAL18V10	300Ω	390Ω	300Ω	390Ω	390Ω	750Ω
GAL22V10	300Ω	390Ω	300Ω	390Ω	390Ω	750Ω
GAL26CV12	470Ω	390Ω	470Ω	390Ω	470Ω	390Ω

AC Test Conditions:

- Cond. 1) R_1 per table; $C_L = 50pF$; R_2 per above table
 Cond. 2) Active High $R_1 = \infty$; Active Low R_1 per table;
 $C_L = 50pF$; R_2 per above table
 Cond. 3) Active High $R_1 = \infty$; Active Low R_1 per table;
 $C_L = 5pF$; R_2 per above table



C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

CAPACITANCE ($T_A = 25^\circ C$, $f = 1.0$ MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	$V_{CC} = 5.0V$, $V_i = 2.0V$
$C_{I/O,Q}$	I/O/Q Capacitance	10	pF	$V_{CC} = 5.0V$, $V_{I/O,Q} = 2.0V$

*Guaranteed but not 100% tested.



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Specifications **GAL22V10 Family****ELECTRICAL CHARACTERISTICS****18V10, 22V10, 26CV12-15L Commercial**

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage	I _{OL} = Max.	—	—	0.5	V
VOH	Output High Voltage	I _{OH} = Max.	2.4	—	—	V
IIL, IIO/QL ¹	Leakage Current Low	V _{IL} = 0V	—	—	-100	μA
		GAL26CV12 & 18V10				
		GAL22V10	—	—	-150	μA
I _{IH} , I _{VO} /QH	Leakage Current High	V _{IH} ≥ 3.5V	—	—	10	μA
I _{OS} ²	Output Short Circuit Current	V _{CC} = 5V V _{OUT} = 0.5V T = 25° C	-50	—	-135	mA
I _{CC}	Operating Power Supply Current	V _{IL} = 0.5V V _{IH} = 3.0V	—	75	115	mA
		f _{toggle} = 15MHz	—	90	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.

2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.**DC RECOMMENDED OPERATING CONDITIONS****18V10, 22V10, 26CV12-15L Commercial**

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
TA	Ambient Temperature		0	75	°C
VCC	Supply Voltage		4.75	5.25	V
VIL	Input Low Voltage		Vss – 0.5	0.8	V
VIH	Input High Voltage		2.0	Vcc+1	V
IOL	Low Level Output Current	GAL18V10 & 22V10	—	16	mA
		GAL26CV12	—	8	mA
IOH	High Level Output Current		—	–3.2	mA



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Specifications GAL22V10 Family

SWITCHING CHARACTERISTICS

18V10, 22V10, 26CV12-15L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. ¹	MIN.	MAX.	UNITS	
t _{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	15	ns	
t _{co}	2	Clk ↑	Q	Clock to Register Output	GAL22V10	1	—	8	ns
					GAL18V10 & 26CV12	1	—	10	ns
t _{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	15	ns	
t _{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	15	ns	
t _{res}	5	I, I/O	Q	Asynchronous Register Reset	1	—	20	ns	

1) Refer to Switching Test Conditions section.

AC RECOMMENDED OPERATING CONDITIONS

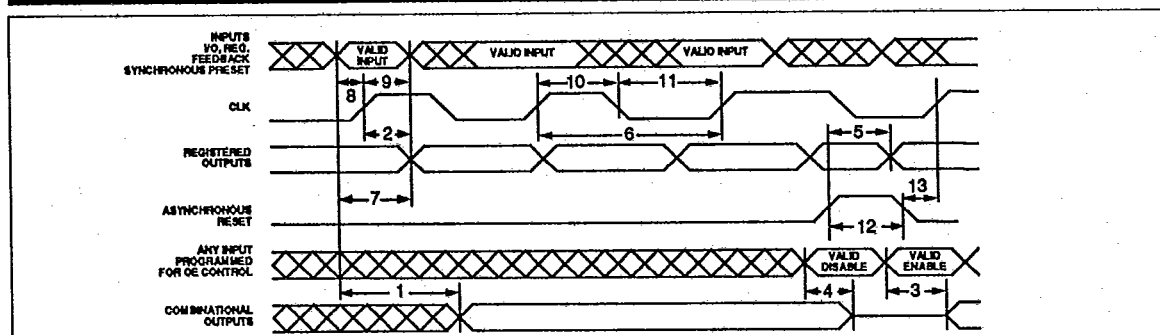
18V10, 22V10, 26CV12-15L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback ¹ = $1 / (t_{wh} + t_{wl})$	—	0	62.5	MHz
	7	Clock Frequency with Feedback ¹ = $1 / (t_{su} + t_{co})$	—	0	50	MHz
t_{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑	GAL22V10	—	12	ns
			GAL18V10 & 26CV12	—	10	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_{wh}	10	Clock Pulse Duration, High ²	—	8	—	ns
t_{wl}	11	Clock Pulse Duration, Low ²	—	8	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	GAL22V10	—	15	ns
			GAL18V10 & 26CV12	—	10	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	—	15	—	ns

1) f_{clk} is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing f_{clk} specifications.

2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS





Specifications GAL22V10 Family

ELECTRICAL CHARACTERISTICS

18V10, 22V10, 26CV12-20L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage	$I_{OL} = \text{Max.}$	—	—	0.5	V
VOH	Output High Voltage	$I_{OH} = \text{Max.}$	2.4	—	—	V
IIL, IIO/QL ¹	Leakage Current Low	$V_L = 0V$	—	—	—100	μA
		GAL26CV12 & 18V10	—	—	—150	μA
I _{IH} , I _{IO} /QH	Leakage Current High	$V_H \geq 3.5V$	—	—	10	μA
I _{OS} ²	Output Short Circuit Current	$V_{CC} = 5V$ $V_{OUT} = 0.5V$ $T = 25^\circ C$	-50	—	-135	mA
I _{CC}	Operating Power Supply Current	$V_L = 0.5V$ $V_H = 3.0V$	—	75	115	mA
		$f_{toggle} = 15MHz$	—	90	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.

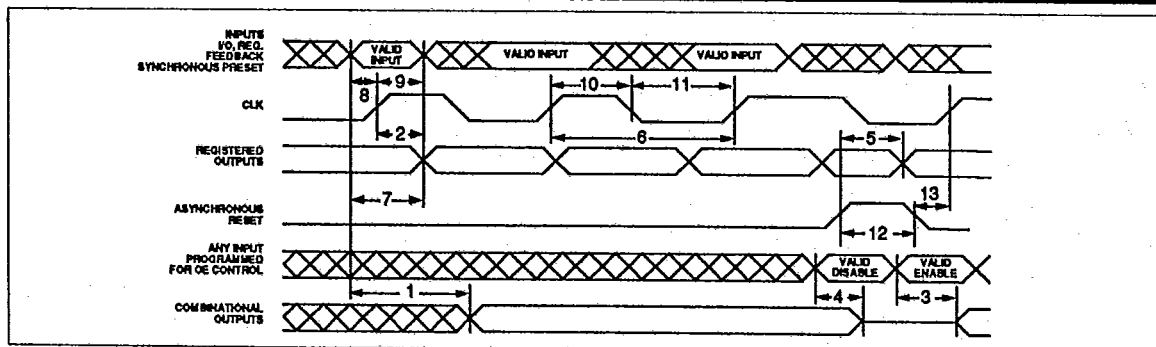
2) One output at a time for a maximum duration of one second. $V_{OUT} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS

18V10, 22V10, 26CV12-20L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T _A	Ambient Temperature	0	75	$^\circ C$
V _{CC}	Supply Voltage	4.75	5.25	V
V _{IL}	Input Low Voltage	$V_{SS} - 0.5$	0.8	V
V _{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V
I _{OL}	Low Level Output Current	—	16	mA
		—	8	mA
I _{OH}	High Level Output Current	—	-3.2	mA

SWITCHING WAVEFORMS





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Specifications GAL22V10 Family

SWITCHING CHARACTERISTICS

18V10, 22V10, 26CV12-20L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. ¹	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	20	ns
t_{co}	2	Clk ↑	Q	Clock to Register Output	GAL22V10	1	—	10 ns
					GAL18V10 & 26CV12	1	—	12 ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	20	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	20	ns
t_{res}	5	I, I/O	Q	Asynch. Register Reset	GAL22V10	1	—	25 ns
					GAL18V10 & 26CV12	1	—	20 ns

1) Refer to Switching Test Conditions section.

AC RECOMMENDED OPERATING CONDITIONS

18V10, 22V10, 26CV12-20L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
fclk	6	Clk Frequency without Feedback ¹ = $1 / (t_{wh} + t_{wl})$	GAL22V10	—	0	50.0 MHz
			GAL18V10 & 26CV12	—	0	62.5 MHz
	7	Clk Frequency with Feedback ¹ = $1 / (t_{su} + t_{co})$	GAL22V10	—	0	40.0 MHz
			GAL18V10 & 26CV12	—	0	41.6 MHz
t_{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑	GAL22V10	—	15	— ns
			GAL18V10 & 26CV12	—	12	— ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_{wh}	10	Clock Pulse Duration, High ²	GAL22V10	—	10	— ns
			GAL18V10 & 26CV12	—	8	— ns
t_{wl}	11	Clock Pulse Duration, Low ²	GAL22V10	—	10	— ns
			GAL18V10 & 26CV12	—	8	— ns
t_{rw}	12	Asynchronous Reset Pulse Duration	GAL22V10	—	20	— ns
			GAL18V10 & 26CV12	—	15	— ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	GAL22V10	—	20	— ns
			GAL18V10 & 26CV12	—	15	— ns

1) fclk is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing fclk specifications.

2) Clock pulses of widths less than the specification may be detected as valid clock signals.



Specifications GAL22V10 Family

ELECTRICAL CHARACTERISTICS

GAL22V10-25L Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage	$I_{OL} = \text{Max.}$	—	—	0.5	V
VOH	Output High Voltage	$I_{OH} = \text{Max.}$	2.4	—	—	V
IIL, I/O/QL ¹	Leakage Current Low	$V_{IL} = 0V$	—	—	-150	μA
IiH, I/O/QH	Leakage Current High	$V_{IH} \geq 3.5V$	—	—	10	μA
IOS ²	Output Short Circuit Current	$V_{CC} = 5V$ $V_{OUT} = 0.5V$ $T = 25^\circ C$	-50	—	-135	mA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V$ $V_{IH} = 3.0V$ $f_{toggle} = 15MHz$	—	90	130	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.

2) One output at a time for a maximum duration of one second. $V_{OUT} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS

GAL22V10-25L Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
TA	Ambient Temperature	0	75	$^\circ C$
VCC	Supply Voltage	4.75	5.25	V
VIL	Input Low Voltage	$V_{SS} - 0.5$	0.8	V
VIH	Input High Voltage	2.0	$V_{CC} + 1$	V
IOL	Low Level Output Current	—	16	mA
IOH	High Level Output Current	—	-3.2	mA

Specifications **GAL22V10 Family****SWITCHING CHARACTERISTICS****GAL22V10-25L Commercial**

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. ¹	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	25	ns
t_{co}	2	Clk ↑	Q	Clock to Register Output	1	—	15	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	25	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	25	ns
t_{res}	5	I, I/O	Q	Asynchronous Register Reset	1	—	25	ns

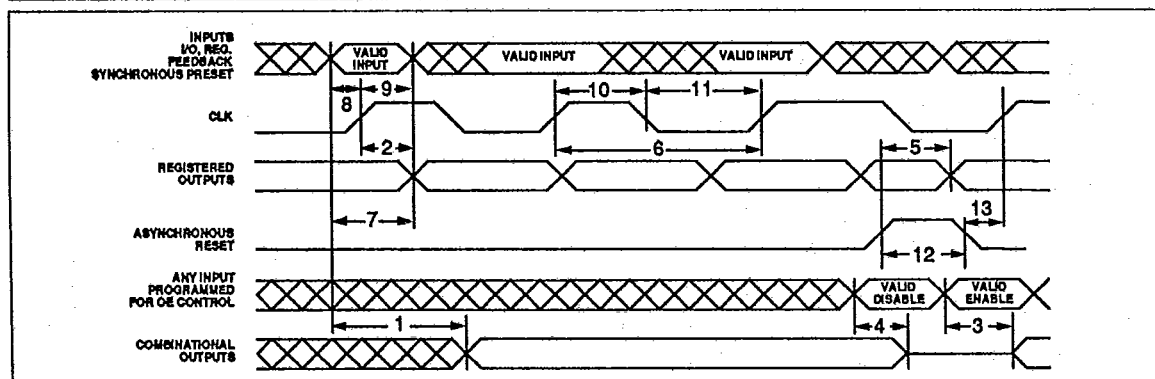
1) Refer to Switching Test Conditions section.

AC RECOMMENDED OPERATING CONDITIONS**GAL22V10-25L Commercial**

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback ¹ = $1 / (t_{wh} + t_{wl})$	—	0	33.3	MHz
	7	Clock Frequency with Feedback ¹ = $1 / (t_{su} + t_{co})$	—	0	33.3	MHz
t_{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑	—	15	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_{wh}	10	Clock Pulse Duration, High ²	—	15	—	ns
t_{wl}	11	Clock Pulse Duration, Low ²	—	15	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	—	25	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	—	25	—	ns

1) f_{clk} is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing f_{clk} specifications.

2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS



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Specifications **GAL22V10 Family****ELECTRICAL CHARACTERISTICS****18V10, 22V10, 26CV12-15L Industrial**

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage	I _{OL} = Max.	—	—	0.5	V
VOH	Output High Voltage	I _{OH} = Max.	2.4	—	—	V
IIL, IIO/QL ¹	Leakage Current Low	V _{IL} = 0V	GAL26CV12 & 18V10		—	—
			GAL22V10		—	—
IIH, IVO/QH	Leakage Current High	V _{IH} ≥ 3.5V	—	—	10	μA
IOS ²	Output Short Circuit Current	V _{CC} = 5V V _{OUT} = 0.5V T = 25°C	—50	—	—135	mA
ICC	Operating Power Supply Current	V _{IL} = 0.5V V _{IH} = 3.0V f _{toggle} = 15MHz	GAL18V10		—	75
			GAL22V10 & 26CV12		—	90

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.

2) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.**DC RECOMMENDED OPERATING CONDITIONS****18V10, 22V10, 26CV12-15L Industrial**

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
TA	Ambient Temperature	—40	85	°C
VCC	Supply Voltage	4.5	5.5	V
VIL	Input Low Voltage	V _{SS} - 0.5	0.8	V
VIH	Input High Voltage	2.0	V _{CC} + 1	V
IOL	Low Level Output Current	GAL18V10 & 22V10		—
		GAL26CV12		—
IOH	High Level Output Current	—	—3.2	mA



Specifications GAL22V10 Family

SWITCHING CHARACTERISTICS

18V10, 22V10, 26CV12-15L Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. ¹	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	15	ns
t_{co}	2	Clk ↑	Q	Clock to Register Output	1	—	8	ns
				GAL18V10 & 26CV12	1	—	10	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	15	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	15	ns
t_{res}	5	I, I/O	Q	Asynchronous Register Reset	1	—	20	ns

1) Refer to Switching Test Conditions section.

AC RECOMMENDED OPERATING CONDITIONS

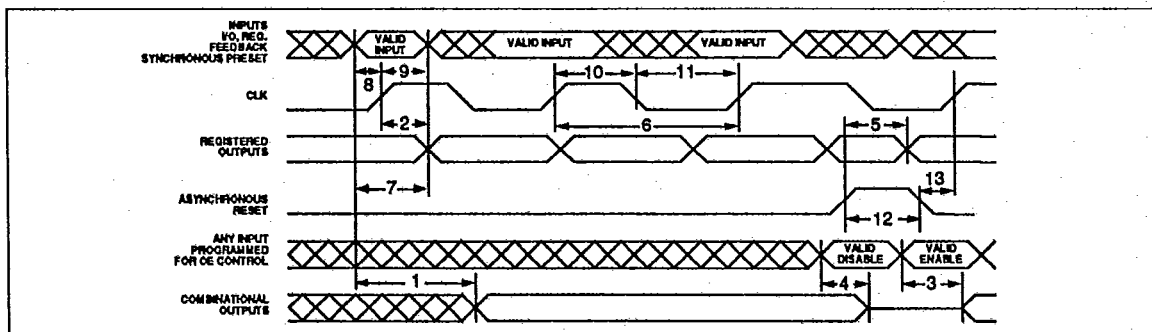
18V10, 22V10, 26CV12-15L Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback ¹ = $1 / (t_{wh} + t_{wl})$	—	0	62.5	MHz
	7	Clock Frequency with Feedback ¹ = $1 / (t_{su} + t_{co})$	—	0	50	MHz
t_{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑	GAL22V10	—	12	ns
			GAL18V10 & 26CV12	—	10	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_{wh}	10	Clock Pulse Duration, High ²	—	8	—	ns
t_{wl}	11	Clock Pulse Duration, Low ²	—	8	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	GAL22V10	—	15	ns
			GAL18V10 & 26CV12	—	10	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	—	15	—	ns

1) f_{clk} is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing f_{clk} specifications.

2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS





Specifications GAL22V10 Family

ELECTRICAL CHARACTERISTICS

18V10, 22V10, 26CV12-20L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage	$I_{OL} = \text{Max.}$	—	—	0.5	V
VOH	Output High Voltage	$I_{OH} = \text{Max.}$	2.4	—	—	V
$I_{IL}, I_{IO}/Q_L^1$	Leakage Current Low	$V_{IL} = 0V$	GAL26CV12 & 18V10		—	—
			GAL22V10		—	—
$I_{IH}, I_{IO}/Q_H$	Leakage Current High	$V_{IH} \geq 3.5V$	—	—	10	μA
I_{OS}^2	Output Short Circuit Current	$V_{CC} = 5V$ $V_{OUT} = 0.5V$ $T = 25^\circ C$	-50	—	-135	mA
ICC	Operating Power Supply Current	$V_{IL} = 0.5V$ $V_{IH} = 3.0V$	GAL18V10		—	75
		$f_{toggle} = 15MHz$	GAL22V10 & 26CV12		—	90
					125	mA
					150	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.

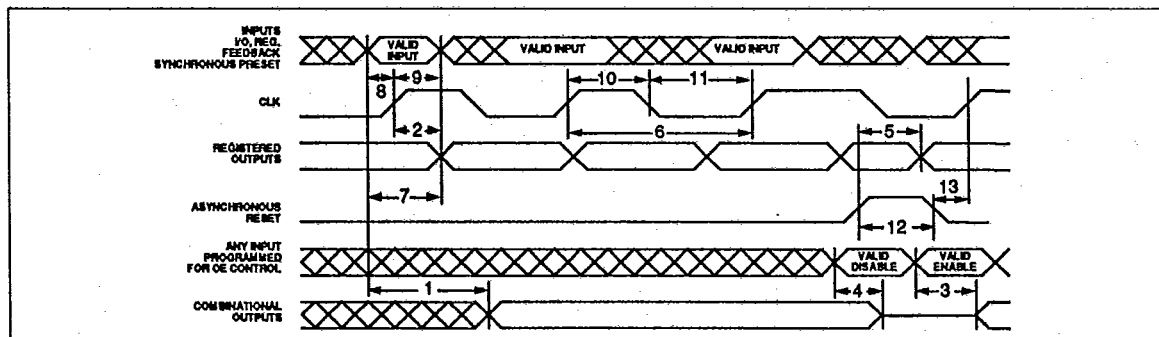
2) One output at a time for a maximum duration of one second. $V_{OUT} = 0.5V$ was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS

18V10, 22V10, 26CV12-20L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	-40	85	$^\circ C$
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IL}	Input Low Voltage	$V_{SS} - 0.5$	0.8	V
V_{IH}	Input High Voltage	2.0	$V_{CC} + 1$	V
I_{OL}	Low Level Output Current	GAL18V10 & 22V10		—
		GAL26CV12		—
				16
				8
I_{OH}	High Level Output Current	—	-3.2	mA

SWITCHING WAVEFORMS





T-46-13-27

Specifications GAL22V10 Family

SWITCHING CHARACTERISTICS**18V10, 22V10, 26CV12-20L Industrial****Over Recommended Operating Conditions**

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. ¹	MIN.	MAX.	UNITS	
t _{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	20	ns	
t _{co}	2	Clk ↑	Q	Clock to Register Output	GAL22V10	1	—	10	ns
					GAL18V10 & 26CV12	1	—	12	ns
t _{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	20	ns	
t _{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	20	ns	
t _{res}	5	I, I/O	Q	Asynch. Register Reset	1	—	25	ns	

1) Refer to Switching Test Conditions section.

AC RECOMMENDED OPERATING CONDITIONS**18V10, 22V10, 26CV12-20L Industrial**

PARAMETER	#	DESCRIPTION		TEST COND.	MIN.	MAX.	UNITS
f _{clk}	6	Clk Frequency without Feedback ¹ = 1 / (t _{wh} + t _{wl})	GAL22V10	—	0	50.0	MHz
			GAL18V10 & 26CV12	—	0	62.5	MHz
	7	Clk Frequency with Feedback ¹ = 1 / (t _{su} + t _{co})	GAL22V10	—	0	40.0	MHz
			GAL18V10 & 26CV12	—	0	41.6	MHz
t _{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑	GAL22V10	—	15	—	ns
			GAL18V10 & 26CV12	—	12	—	ns
t _h	9	Hold Time, Input or Feedback, after Clk ↑		—	0	—	ns
t _{wh}	10	Clock Pulse Duration, High ²	GAL22V10	—	10	—	ns
			GAL18V10 & 26CV12	—	8	—	ns
t _{wl}	11	Clock Pulse Duration, Low ²	GAL22V10	—	10	—	ns
			GAL18V10 & 26CV12	—	8	—	ns
t _{rw}	12	Asynchronous Reset Pulse Duration	GAL22V10	—	20	—	ns
			GAL18V10 & 26CV12	—	15	—	ns
t _{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	GAL22V10	—	20	—	ns
			GAL18V10 & 26CV12	—	15	—	ns

1) f_{clk} is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing f_{clk} specifications.

2) Clock pulses of widths less than the specification may be detected as valid clock signals.



Specifications GAL22V10 Family

ELECTRICAL CHARACTERISTICS

18V10, 22V10, 26CV12-15L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage	IOL = Max.	—	—	0.5	V
VOH	Output High Voltage	IOH = Max.	2.4	—	—	V
IIL, II/O/QL ¹	Leakage Current Low	VIL = 0V	GAL26CV12 & 18V10		—100	μA
			GAL22V10		—150	μA
IIH, II/O/QH	Leakage Current High	VIH ≥ 3.5V	—	—	10	μA
IOS ²	Output Short Circuit Current	VCC = 5V VOUT = 0.5V T = 25°C	—50	—	—135	mA
ICC	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V	GAL18V10		75	mA
		fIOCLK = 15MHz	GAL22V10 & 26CV12		90	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.

2) One output at a time for a maximum duration of one second. VOUT = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS

18V10, 22V10, 26CV12-15L Military

SYMBOL	PARAMETER		MIN.	MAX.	UNITS
Tc	Case Temperature		-55	125	°C
VCC	Supply Voltage		4.5	5.5	V
VIL	Input Low Voltage		Vss – 0.5	0.8	V
VIH	Input High Voltage		2.0	Vcc+1	V
IoL	Low Level Output Current	GAL18V10 & 22V10	—	12	mA
		GAL26CV12	—	8	mA
IoH	High Level Output Current		—	–2.0	mA



Specifications GAL22V10 Family

SWITCHING CHARACTERISTICS

18V10, 22V10, 26CV12-15L Military

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
t_{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	15	ns
t_{co}	2	Clk ↑	Q	Clock to Register Output	GAL22V10	—	8	ns
					GAL18V10 & 26CV12	—	10	ns
t_{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	15	ns
t_{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	15	ns
t_{res}	5	I, I/O	Q	Asynchronous Register Reset	1	—	20	ns

1) Refer to Switching Test Conditions section.

AC RECOMMENDED OPERATING CONDITIONS

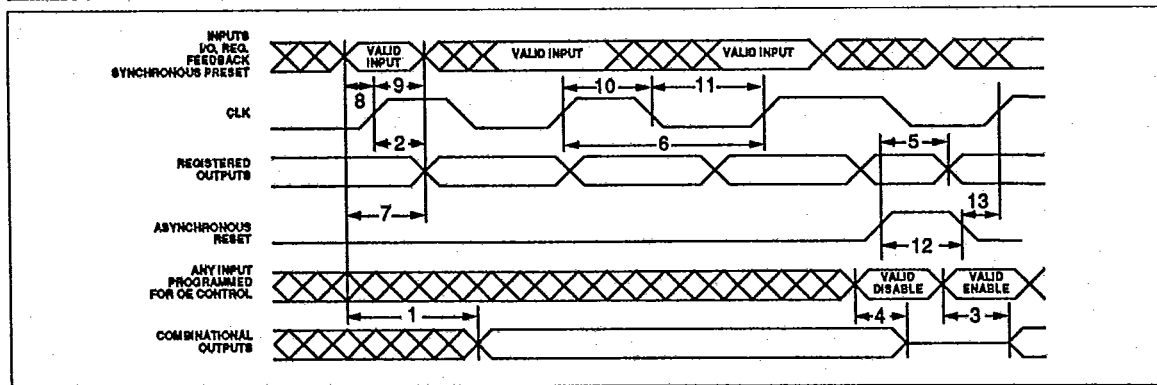
18V10, 22V10, 26CV12-15L Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS	
f _{clk}	6	Clock Frequency without Feedback* = 1 / (t _{wh} + t _{wl})	—	0	62.5	MHz	
	7	Clock Frequency with Feedback* = 1 / (t _{su} + t _{wh})	GAL22V10	—	0	50	MHz
		GAL18V10 & 26CV12	—	0	45.5	MHz	
t _{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑	—	12	—	ns	
t _h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns	
t _{wh}	10	Clock Pulse Duration, High*	—	8	—	ns	
t _{wl}	11	Clock Pulse Duration, Low*	—	8	—	ns	
t _{rw}	12	Asynchronous Reset Pulse Duration	—	15	—	ns	
t _{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	—	15	—	ns	

1) f_{clk} is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing f_{clk} specifications.

2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS





Specifications GAL22V10 Family

ELECTRICAL CHARACTERISTICS

18V10, 22V10, 26CV12-20L Military

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage	IOL = Max.	—	—	0.5	V
VOH	Output High Voltage	IOH = Max.	2.4	—	—	V
IIL, IIO/QL ¹	Leakage Current Low	VIL = 0V	—	—	—100	μA
		GAL26CV12 & 18V10			—150	μA
IIH, IIO/QH	Leakage Current High	VH ≥ 3.5V	—	—	10	μA
IOS ²	Output Short Circuit Current	VCC = 5V VOUT = 0.5V T = 25° C	—50	—	—135	mA
ICC	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V	—	75	135	mA
		f _{toggle} = 15MHz	—	90	150	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.

2) One output at a time for a maximum duration of one second. VOUT = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS

18V10, 22V10, 26CV12-20L Military

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
TC	Case Temperature	—55	125	°C
VCC	Supply Voltage	4.5	5.5	V
VIL	Input Low Voltage	V _{SS} — 0.5	0.8	V
VIH	Input High Voltage	2.0	VCC+1	V
IOL	Low Level Output Current	—	12	mA
			8	mA
IOH	High Level Output Current	—	—2.0	mA



Specifications GAL22V10 Family

SWITCHING CHARACTERISTICS

18V10, 22V10, 26CV12-20L Military

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. ¹	MIN.	MAX.	UNITS	
t _{pd}	1	I, I/O	O	Input or Feedback to Combinational Output	1	—	20	ns	
t _{co}	2	Clk ↑	Q	Clock to Register Output	GAL22V10	1	—	15	ns
					GAL18V10 & 26CV12	1	—	15	ns
t _{en}	3	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	20	ns	
t _{dis}	4	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	20	ns	
t _{res}	5	I, I/O	Q	Asynch. Register Reset	1	—	25	ns	

1) Refer to Switching Test Conditions section.

AC RECOMMENDED OPERATING CONDITIONS

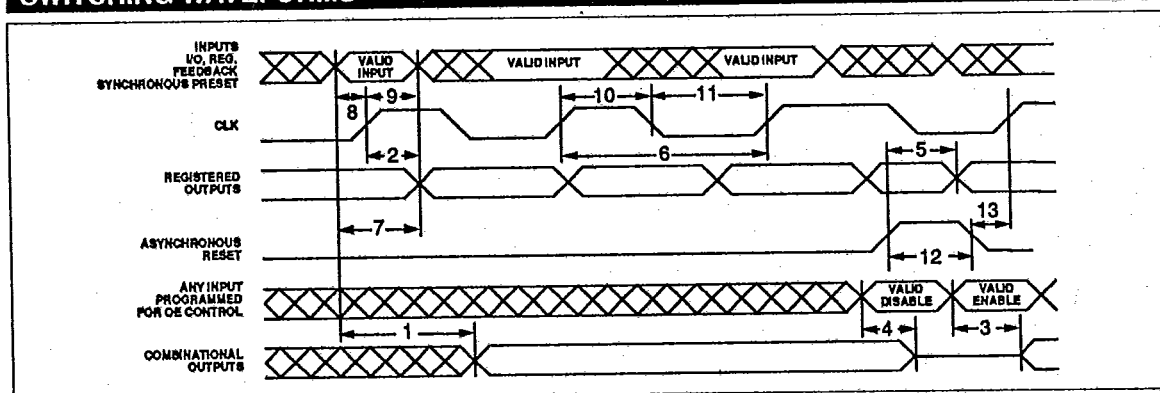
18V10, 22V10, 26CV12-20L Military

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	6	Clock Frequency without Feedback ¹ = $1 / (t_{wh} + t_{wl})$	—	0	33.3	MHz
	7	Clock Frequency with Feedback ¹ = $1 / (t_{su} + t_{co})$	—	0	31.2	MHz
t_{su}	8	Setup Time, Input, Feedback, or SP before Clk ↑	—	17	—	ns
t_h	9	Hold Time, Input or Feedback, after Clk ↑	—	0	—	ns
t_{wh}	10	Clock Pulse Duration, High ²	—	15	—	ns
t_{wl}	11	Clock Pulse Duration, Low ²	—	15	—	ns
t_{rw}	12	Asynchronous Reset Pulse Duration	—	20	—	ns
t_{rec}	13	Asynchronous Reset to Clk ↑ Recovery Time	—	20	—	ns

1) f_{clk} is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing f_{clk} specifications.

2) Clock pulses of widths less than the specification may be detected as valid clock signals.

SWITCHING WAVEFORMS





T-46-13-27 Specifications GAL22V10 Family

OUTPUT LOGIC MACROCELL ARCHITECTURE

The GAL18V10, 22V10, and 26CV12 each have a variable number of product terms per OLMC.

Of the ten OLMCs available in the GAL18V10, eight OLMCs have access to eight product terms and two have ten product terms (refer to GAL18V10 Logic Diagram).

Of the ten OLMCs available in the GAL22V10, two OLMCs have access to eight product terms, two have ten product terms, two have twelve product terms, two have fourteen product terms, and two OLMCs have sixteen product terms (refer to GAL22V10 Logic Diagram).

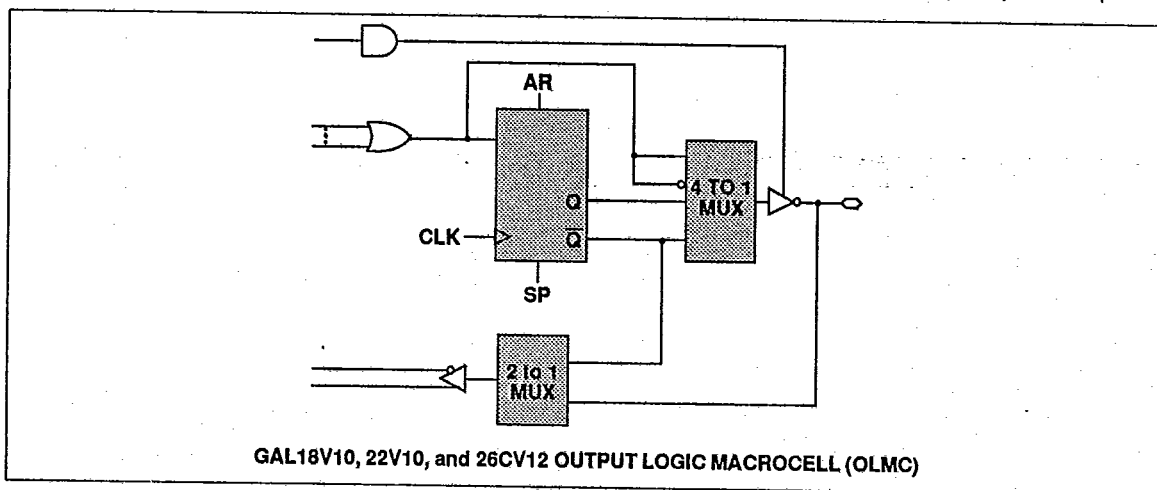
Of the twelve OLMCs available in the GAL26CV12, eight OLMCs have access to eight product terms, two have ten product terms,

and two have twelve product terms (refer to GAL26CV12 Logic Diagram).

The output polarity of each OLMC can be individually programmed to be true or inverting, in either combinational or registered mode. This allows the user to reduce the overall number of product terms required in a design and/or to invert the output signal.

GAL22V10 Family devices have a product term for AR (Asynchronous Reset) and a product term for SP (Synchronous Preset). These two product terms are common to all registered OLMCs.

NOTE: Output polarity selection does NOT affect the behavior of the OLMC's integral "D" flip-flop but does affect the value (0 or 1) of the output. The AR and SP product terms will force the flip-flop into the same state regardless of the polarity of the output.



OUTPUT LOGIC MACROCELL CONFIGURATIONS

The GAL18V10, 22V10, and 26CV12 have two primary functional modes which may be selected when compiling source equations (registered and combinational / input). Each of these two primary modes are described below.

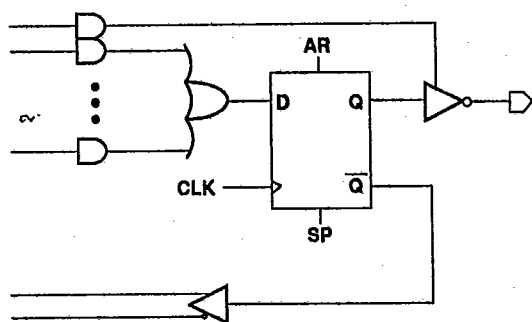
REGISTERED

In registered mode the output pin associated with an individual OLMC is driven by the "Q" output of that OLMC's "D" flip-flop. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or invert (active low). Output tri-state control is available and can be individually selected as either "on", "off", or dynamically "product-term driven." The "D" flip-flop's "Q" output is fed back into the "AND" array via the "AND" array buffer. Both polarities (true and invert) of the OLMC are fed back into the "AND" array.

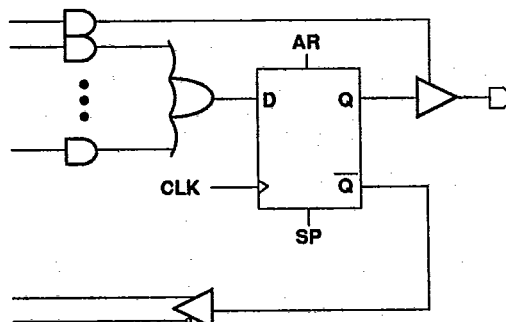
NOTE: In registered mode a tri-stated output pin may NOT be used as an input into the "AND" array.

COMBINATIONAL / INPUT

In combinational mode the pin associated with an individual OLMC is driven by the output of the sum term gate. Logic polarity of the output signal at the pin may be selected by specifying that the output buffer drive either true (active high) or invert (active low). Output tri-state control is available and may be individually selected as either "on" (dedicated output), "off" (dedicated input), or "product-term driven" (dynamic I/O). Feed back into the "AND" array is from the device pin, via the "AND" array buffer. Both polarities (true and invert) of the pin are fed back into the "AND" array.

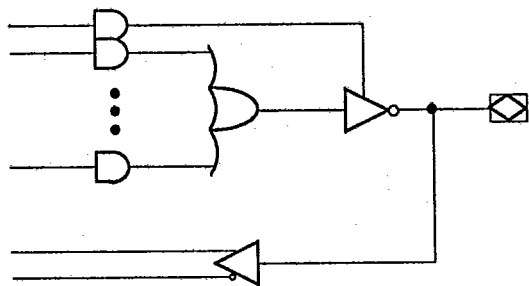
Specifications **GAL22V10 Family****REGISTERED MODE**

ACTIVE LOW

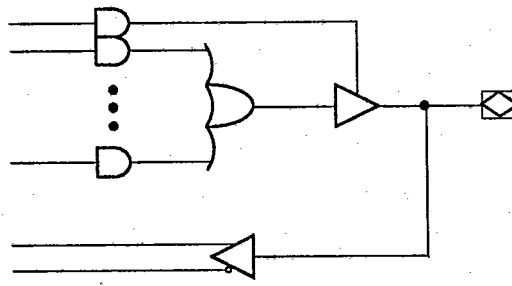


ACTIVE HIGH

2

COMBINATIONAL MODE

ACTIVE LOW



ACTIVE HIGH



T-46-13-27

Specifications GAL22V10 Family

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every GAL18V10, 22V10, and 26CV12 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

SECURITY CELL

A security cell is provided with every GAL18V10, 22V10, and 26CV12 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE MODE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

LATCH-UP PROTECTION

GAL18V10, 22V10, and 26CV12 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input under-shoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pullup instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

OUTPUT REGISTER PRELOAD

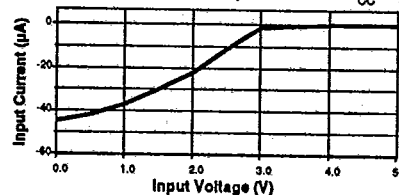
When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

GAL18V10, 22V10, and 26CV12 devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

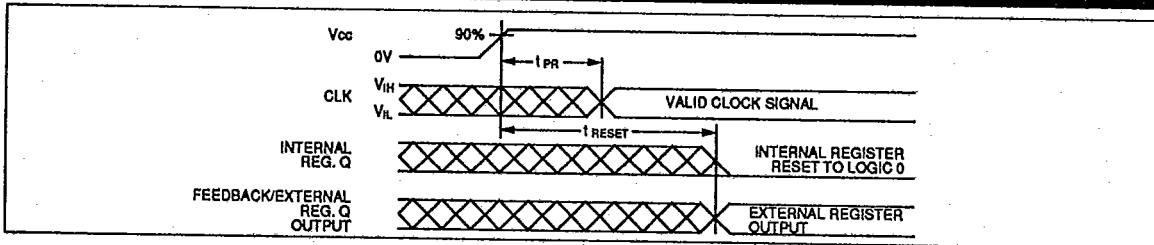
INPUT BUFFERS

GAL22V10 Family devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than bipolar logic.

The buffers also possess active pull-ups within their input structure. Unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice recommends that all unused inputs and tri-stated I/O pins be connected to an adjacent active input, V_{CC} , or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.



POWER-UP RESET



Circuitry within GAL18V10, 22V10, and 26CV12 devices provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET} , 45µs MAX). This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the device. First,

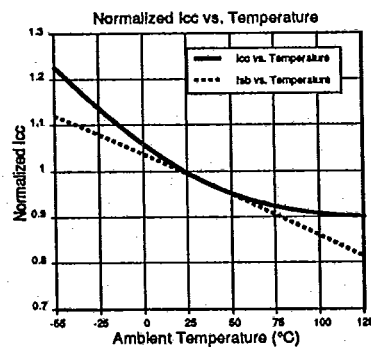
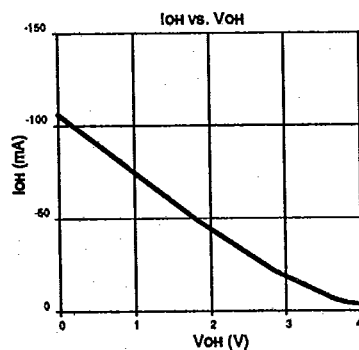
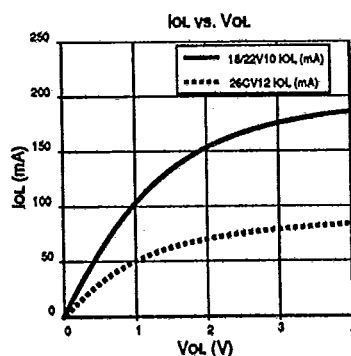
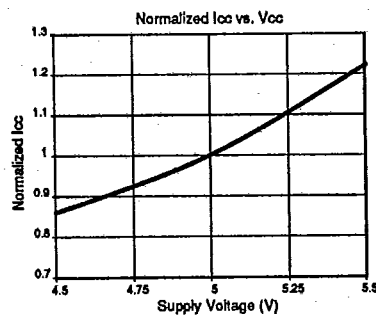
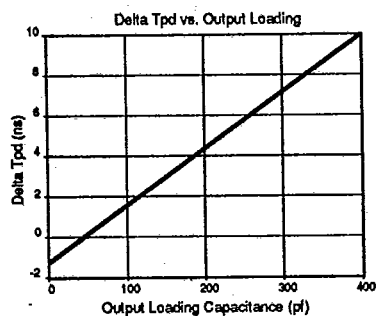
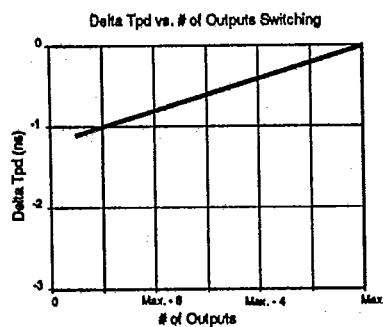
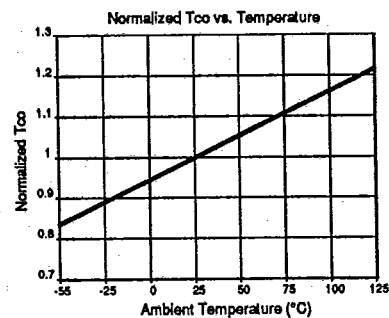
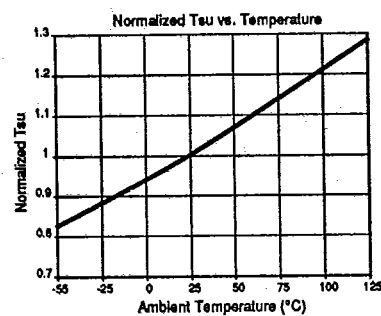
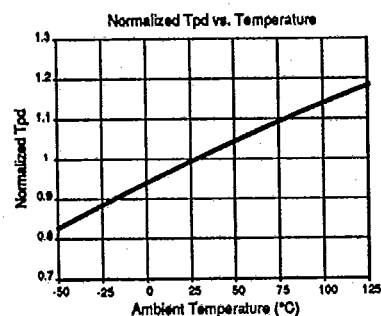
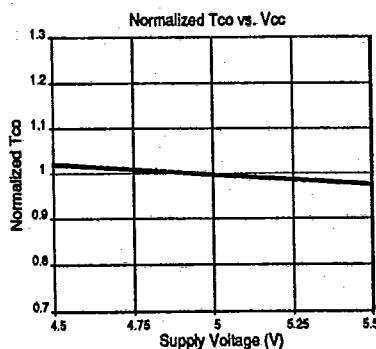
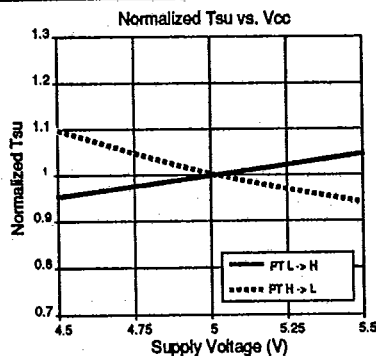
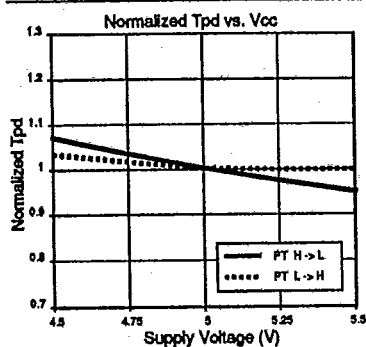
the V_{CC} rise must be monotonic. Second, the clock input must become a proper TTL level within the specified time (t_{PR} , 100ns MAX). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

Note that the internal register powers-up to a logic 0. The device pin state is determined by the user-defined polarity control bit on each macrocell (refer to OLMC description).



T-46-13-27
Specifications **GAL22V10 Family**

2

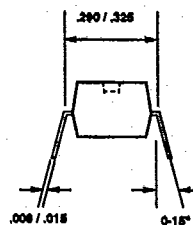
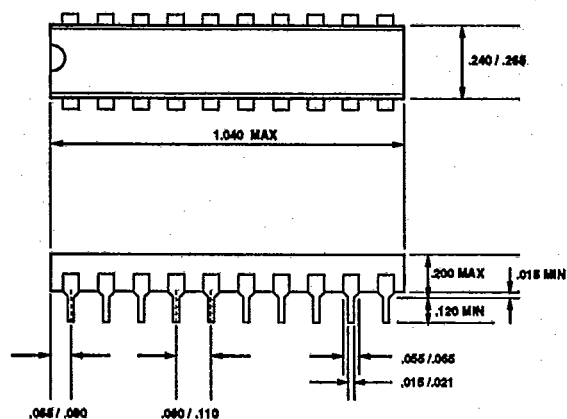


PACKAGE DIAGRAMS

T-90-20

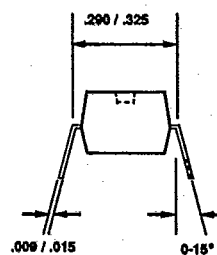
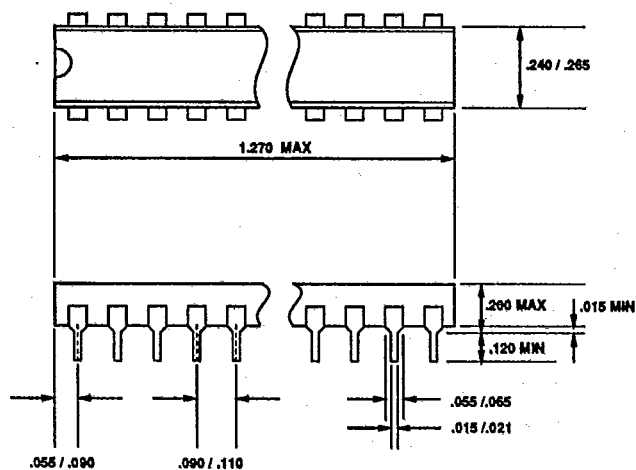
20-Pin Plastic DIP

Dimensions in Inches MIN. / MAX.



24-Pin Plastic DIP

Dimensions in Inches MIN. / MAX.



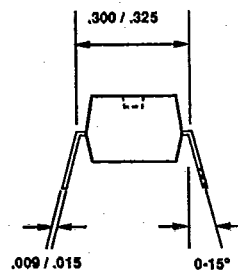
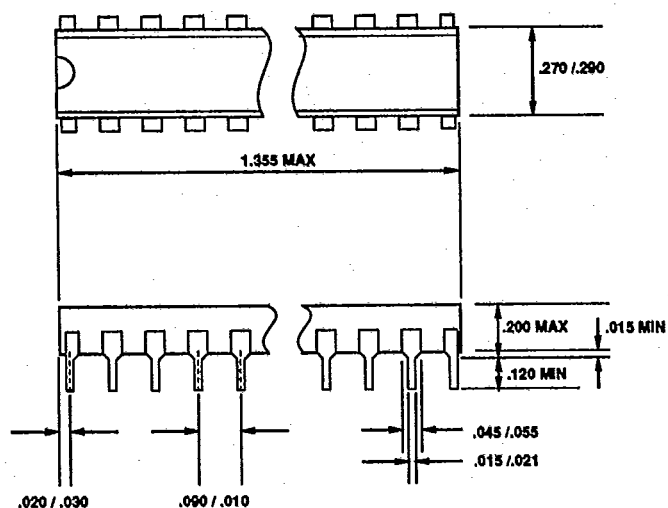


Package Diagrams

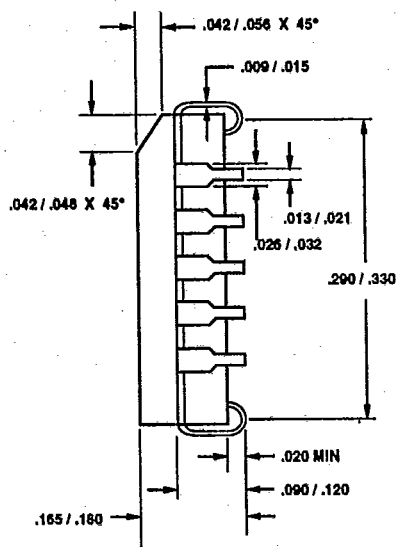
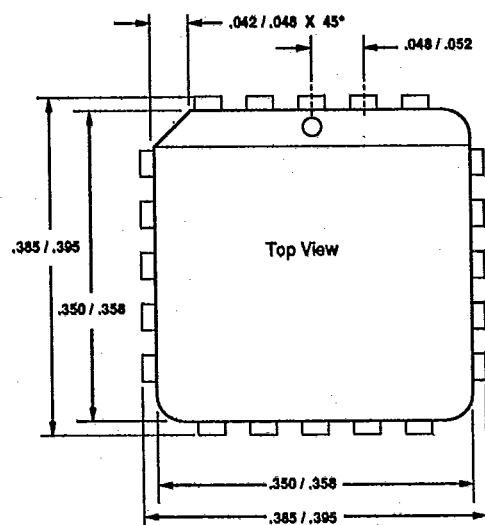
T-90-20

28-Pin Plastic DIP

Dimensions in Inches MIN. / MAX.

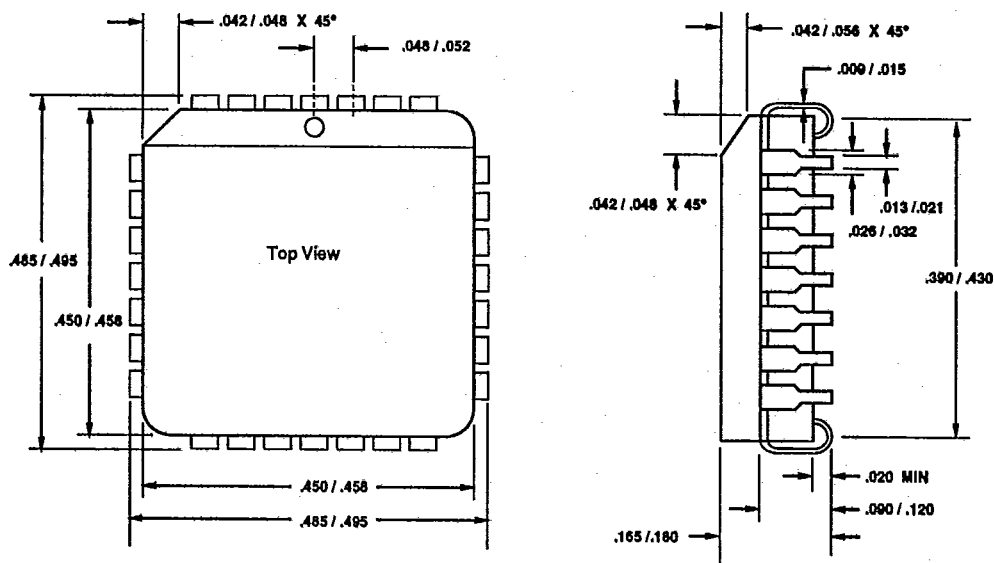
**20-Pin PLCC Package**

Dimensions in Inches MIN. / MAX.

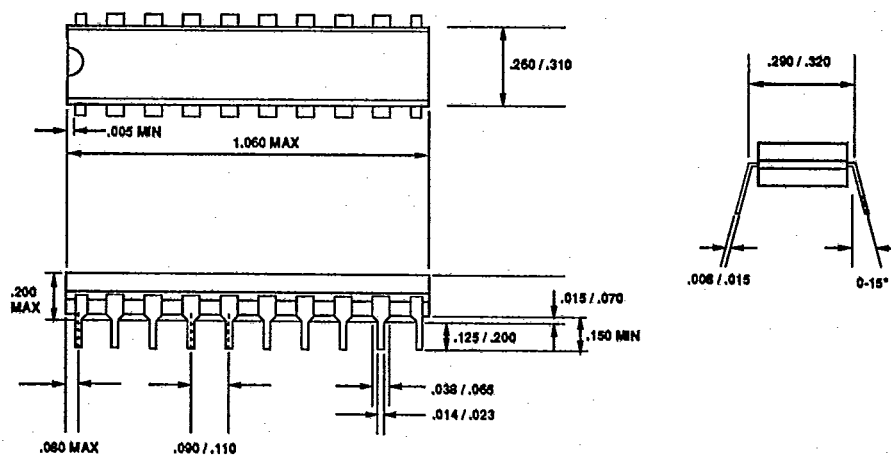


**28-Pin PLCC Package**

Dimensions in Inches MIN. / MAX.

**20-Pin (300 MIL) Cerdip**

Dimensions in Inches MIN. / MAX.



**24-Pin (300 MIL) Cerdip**

Dimensions in Inches MIN. / MAX.

