T-50-09

PLESSEY
Semiconductors

NJ8821, NJ8821B

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE) WITH RESETTABLE COUNTERS

The NJ8821/NJ8821B is a synthesiser circuit fabricated on the Plessey 5-micron CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 11-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'M' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

The NJ8821 is available in Plastic DIL (DP) and Miniature Plastic DIL (MP) packages, both with operating temperature range of -30°C to +70°C. The NJ8821B is available only in Ceramic DIL package with operating temperature range of -40°C to +85°C.

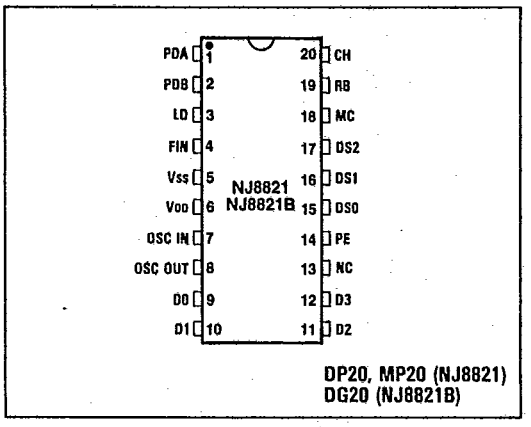

Fig.1 Pin connections

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- >10MHz Input Frequency

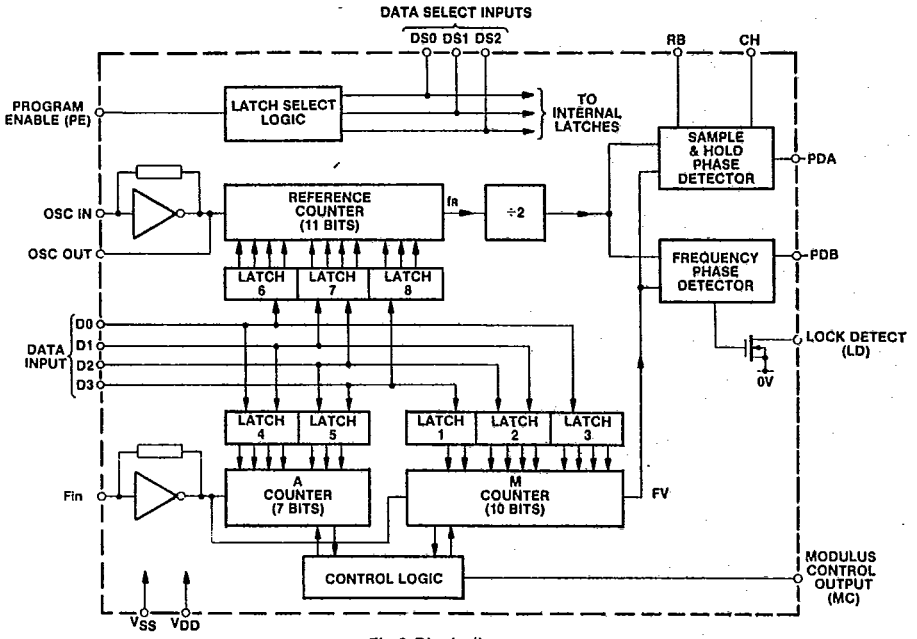

Fig.2 Block diagram

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ELECTRICAL CONDITIONS

Test conditions (unless otherwise stated):

V_{DD}-Vss 5V ± 0.5V

Temperature range NJ8821: -30°C to +70°C, NJ8821B: -40°C to +85°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5.5	mA	FOSC, FIN = 10MHz, 0 to 5V square wave
		0.7	1.5	mA	FOSC, FIN = 1.0MHz, 0 to 5V square wave
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input					
High level	4.25			V	
Low level			0.75	V	
DS INPUTS					
High level	4.25			V	
Low level			0.75	V	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-Vss.Note 4
Propagation delay, clock to modulus control		30	50	ns	Note 2
Strobe pulse width external mode, $t_{w(ST)}$	2			μs	
Data set-up time, $t_{s(DATA)}$	1			μs	
Data hold time, $t_{H(DATA)}$	1			μs	
Address set-up time, t_{SE}	1			μs	
Address hold time, t_{HE}	1			μs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.6
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	

NOTES

1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5 microseconds.
4. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

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Pin No.	Name	Description
1	PDA	Analog output from the sample and hold phase comparator for use as a 'fine' error signal. **Output at (V_{DD}-V_{SS})/2 when in lock.** Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	V_{SS}	Negative supply (normally ground)
6	V_{DD}	Positive supply
7,8	OSC.IN/ OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal-generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The program range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
9,10,11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
14	PE	This pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
15,16,17	DS0-DS2	Data-select inputs to control the addressing of data latches.
18	MC	Signal for controlling an external dual-modulus prescaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'M' counter completes its cycle at which point both counters are reset. This gives a total division ratio of M.N +A where N and N +1 represent the dual modulus prescale values. The program range of the 'A' counter is 0-127 and therefore can control prescalers with a division ratio up to and including ÷128/129. The program range of the 'M' counter is 3-1023 and for correct program operation M ≥A. Where every possible channel is required, the minimum division ratio should be N^2-N.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD} - V_{SS})	-0.5V to 7V
Input voltage	
Open drain O/P (pin 3)	7V
All other pins	V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature	-65°C to +150°C (DG Package, NJ8821B)
Storage temperature	-55°C to +125°C (DP and MP packages, NJ8821)

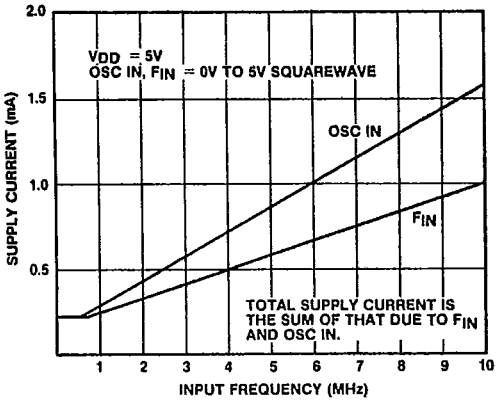


Fig.3 Typical supply current versus input frequency

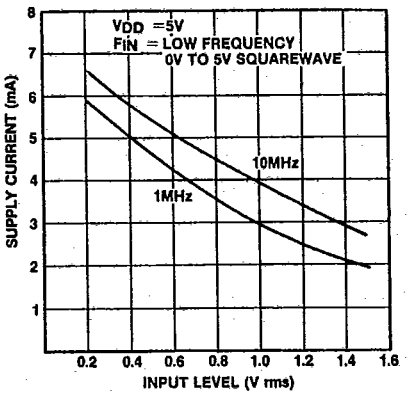


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is Fig.5 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.6.

When re-programming, a reset to zero state is followed by reloading with the new counter values. This means the synthesiser loop lock up time will be well defined and less than 10msec. If shorter lock up times are required, when making only small changes in frequency, the non-resettable version NJ8823 should be considered.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	M1	M0	-	-
2	0	0	1	M5	M4	M3	M2
3	0	1	0	M9	M8	M7	M6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

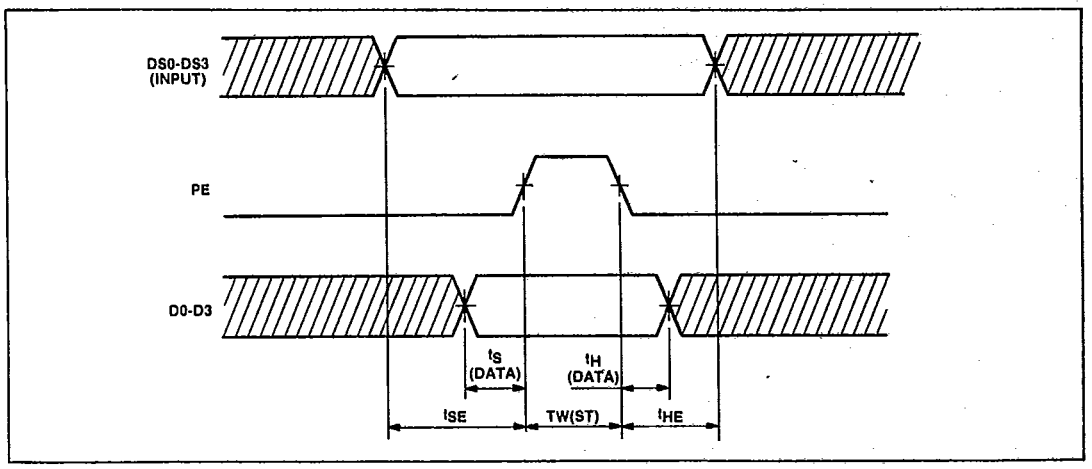


Fig.6 Timing diagram

PHASE COMPARATORS

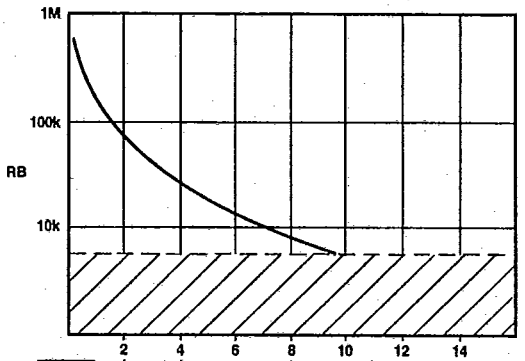
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at (V_{DD}-V_{SS})/2 and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}\text{-}V_{SS}\text{-}0.7\text{-}89(RB^{-½})]}{2 \times \pi\ 50\times10^{-12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.7 for example shows that to achieve a gain of 380V per radian at 10kHz requires approximately 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.7 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.7 RB versus gain and reference frequency

CRYSTAL OSCILLATOR

When using the internal oscillator, the stability may be enhanced at high frequencies by the use of an external resistor between Pin 8 and the other components. A value of 150-270Ω is advised.

PROGRAMMING/POWER UP

All data and signal input pins should have no input applied to them prior to the application of V_{DD}, as otherwise 'latch up' may occur.