

Description

The GCD5412 is a timing and sync one chip controller IC with auto IRIS function for B/W CCD camera systems, which is fabricated in the LGS 0.8 μ CMOS process.

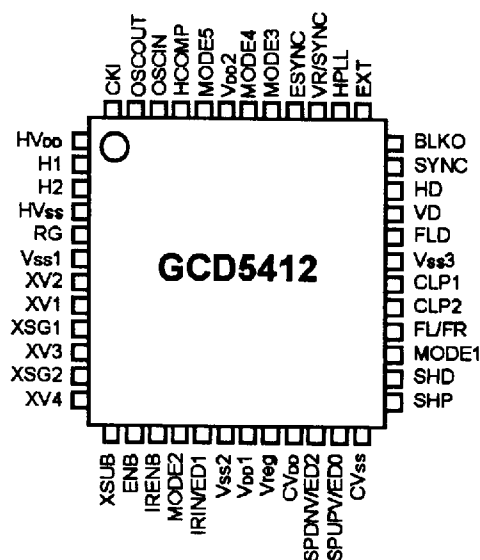
Feature

- EIA / CCIR standards
- Auto IRIS function
- Supports field / frame accumulation mode
- Supports external sync mode
- Supports non-interlacing mode
- Oscillator frequency : 1212fh
(EIA : 19.0699MHz, CCIR : 18.9375MHz)
- 48 pin TQFP package
- Kit with GCD4402, GCD1001S
- Built-in sync signal generation function

Application

CCD monochrome camera systems.

Pin Configuration



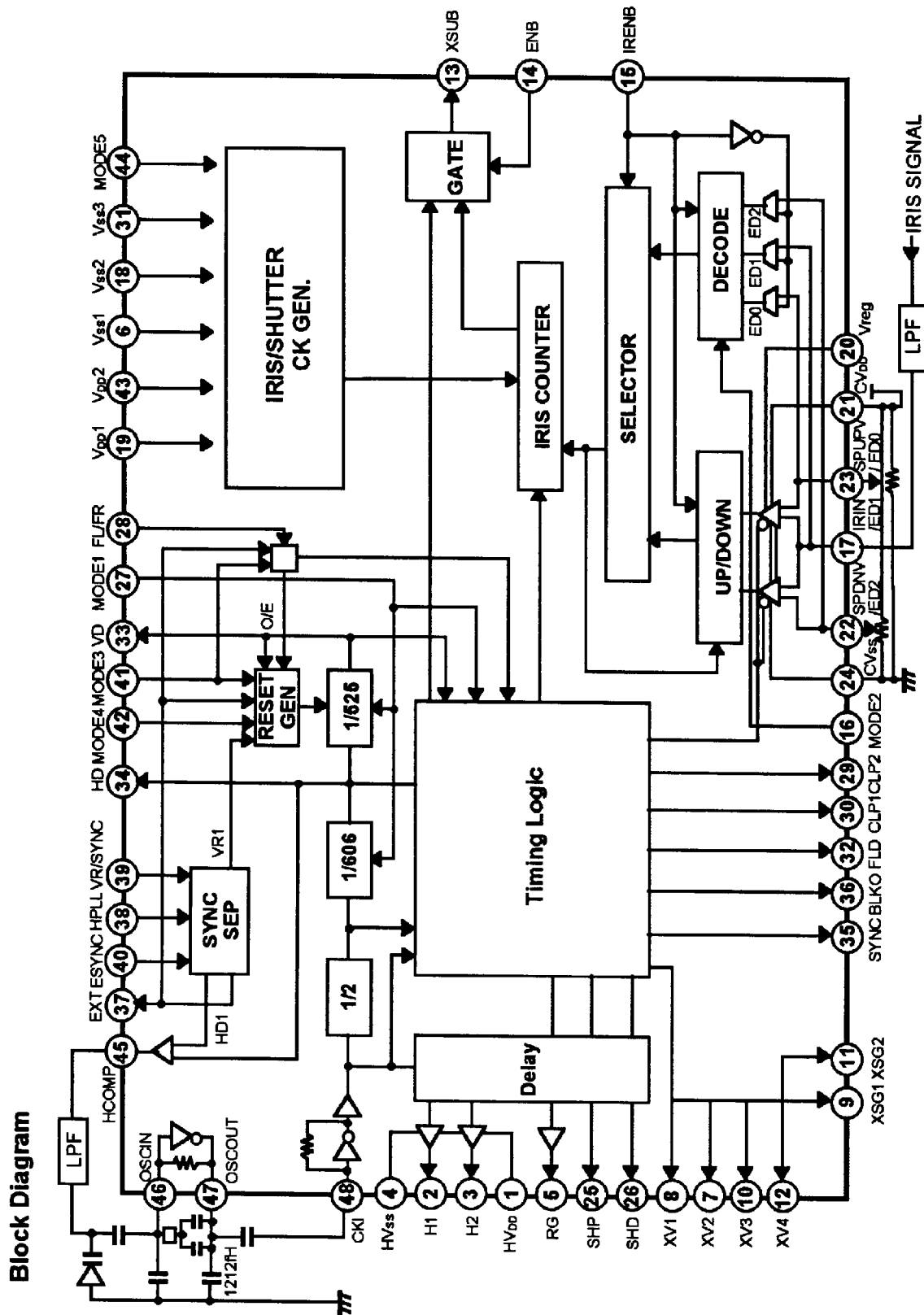
48 PIN TQFP

Absolute Maximum Ratings (Ta = 25°C, Vss=0V)

Symbol	Parameter	Rating	Unit
V _{DD}	Supply Voltage	V _{ss} -0.5 to +7.5	V
V _I	Input Voltage	V _{ss} -0.5 to V _{DD} +0.5	V
V _O	Output Voltage	V _{ss} -0.5 to V _{DD} +0.5	V
T _{OPR}	Operating Temperature	-20 ~ +75	°C
T _{STG}	Storage Temperature	-55 ~ +150	°C

Operating Conditions

Symbol	Parameter	Rating	Unit
V _{DD}	Supply Voltage	5.0 ± 0.25	V
T _{OPR}	Operating Temperature	-20 ~ +75	°C



Pin Description

NO.	Symbol	I/O	Description
1	HV _{DD}	-	Power supply (for H1, H2)
2	H1	O	H1 clock output for CCD horizontal register drive
3	H2	O	H2 clock output for CCD horizontal register drive
4	HV _{SS}	-	GND(for H1, H2)
5	RG	O	Reset gate pulse output
6	V _{SS} 1	-	GND
7	XV2	O	XV2 clock output for CCD vertical register drive
8	XV1	O	XV1 clock output for CCD vertical register drive
9	XSG1	O	CCD sensor charge readout pulse output
10	XV3	O	XV3 clock output for CCD vertical register drive
11	XSG2	O	CCD sensor charge readout pulse output
12	XV4	O	XV4 clock output for CCD vertical register drive
13	XSUB	O	CCD discharge pulse output
14	ENB	I	XSUB pulse output ON/OFF control (with pull-up resistance) Low : XSUB pulse output stop ; High : XSUB pulse output
15	IRENB	I	Low : Electronic shutter mode ; High : Auto iris mode (with pull-up resistance)
16	MODE2	I	Electronic shutter speed input switchover (with pull-up resistance) Low : serial input ; High : parallel input
17	IRIN/ED1	I*1	Iris signal input/shutter speed setting ; clock input in serial mode
18	V _{SS} 2	-	GND
19	V _{DD} 1	-	Power supply
20	V _{reg}	-	Bias current supply for comparator
21	CV _{DD}	-	Power supply (for comparator)
22	SPDNV /ED2	I*1	Shutter speed down reference voltage/ Shutter speed setting ; data input in serial mode
23	SPUPV /ED0	I*1	Shutter speed up reference voltage / Shutter speed setting ; strobe input in serial mode
24	CV _{SS}	-	GND(for comparator)
25	SHP	O	Precharge level sample-and-hold pulse
26	SHD	O	Data sample-and-hold pulse
27	MODE1	I	Low : EIA ; High : CCIR (with pull-down resistance)
28	FL/FR	I	Field accumulation/frame accumulation, odd field/even field switchover (with pull-down resistance)
29	CLP2	O	Pulse output for clamp
30	CLP1	O	Pulse output for clamp

NO.	Symbol	I/O	Description
31	V _{ss3}	-	GND
32	FLD	O	Field identification signal output ; High : odd field ; Low : even field
33	VD	O	Vertical drive output
34	HD	O	Horizontal drive output
35	SYNC	O	Composite sync output
36	BLKO	O	Composite blanking output
37	EXT	O	External sync/internal sync identification signal;High : external sync ; Low : internal sync
38	HPLL	I	Horizontal drive signal input (with pull-up resistance)
39	VR/SYNC	I	Vertical drive signal input/composite sync input (with pull-up resistance)
40	ESYNC	I	Low : SYNC sync or internal sync ; High : VD/HD sync (with pull-down resistance)
41	MODE3	I	Low : interlace mode ; High : non-interlace mode (with pull-down resistance)
42	MODE4	I	Line number selection pin (with pull-down resistance) Low : EIA 262H/CCIR 312H ; High : EIA 263H/CCIR 313H
43	V _{DD2}	-	Power supply
44	MODE5	I*2	Low : Normal mode ; High : Test mode (with pull-down resistance)
45	HCOMP	O	Comparator output (H phase comparator)
46	OSCIN	I*3	Oscillation (crystal oscillator) inverter input
47	OSCOUT	O	Oscillation (crystal oscillator) inverter output
48	CKI	I*4	Clock input

I*1 → Comparater Input

I*2 → Fixed to low level

I*3 → OSCILLATOR Cell

I*4 → Input cell with feedback resistance



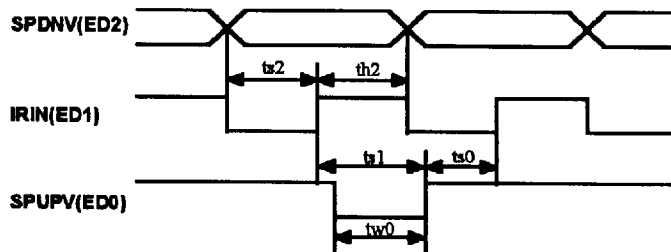
Electrical Characteristics

1) DC Characteristics

(VDD = 5V ± 0.25V, Topr = -20 to 75 °C)

Item	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	VDD		4.75	5.0	5.25	V
Input voltage	V _{IH}		0.7VDD			V
	V _{IL}				0.3VDD	V
Output voltage 1 (All output pins except those below)	V _{OH1}	I _{OH} = -2mA	VDD - 0.8			V
	V _{OL1}	I _{OL} = 4mA			0.4	V
Output voltage 2 (Pins 25, 26)	V _{OH2}	I _{OH} = -4mA	VDD - 0.8			V
	V _{OL2}	I _{OL} = 8mA			0.4	V
Output voltage 3 (Pin 5, 45)	V _{OH3}	I _{OH} = -8mA	VDD - 0.8			V
	V _{OL3}	I _{OL} = 8mA			0.4	V
Output voltage 4 (Pins 2, 3)	V _{OH4}	I _{OH} = -12mA	VDD - 8			
	V _{OL4}	I _{OL} = 12mA			0.4	
Output voltage 5 (Pin 47)	V _{OH5}	I _{OH} = -1mA	VDD / 2			V
	V _{OL5}	I _{OL} = 1mA			0.4	V
Feedback resistance	RFB	V _{IN} = Vss or VDD	250K	1M	2.5M	Ω
Pull-up current	I _{PU}	V _{IL} = 0V	-80		-30	μA
Pull-down current	I _{PD}	V _{IH} = VDD	40		110	μA
Current consumption	I _{DD}	VDD = 5V GCA325KBL in normal operating state		28		mA

2) AC Characteristics



Symbol	Item	Min.	Max.
ts2	SPDNV (ED2) setup time for IRIN (ED1) rise	20ns	-
th2	SPDNV (ED2) hold time for IRIN (ED1) rise	20ns	-
ts1	IRIN (ED1) setup time for SPUPV (ED0) rise	20ns	-
tw0	SPUPV (ED0) pulse width	20ns	50 μs
ts0	SPUPV (ED0) setup time for IRIN (ED1) rise	20ns	-



Electronic Shutter/Auto IRIS

By setting the ENB pin (Pin 14) high, the XSUB pulse is output for a specific period to activate the electronic shutter and auto iris.

1) Auto Iris (IRENB=high, MODE2=any level)

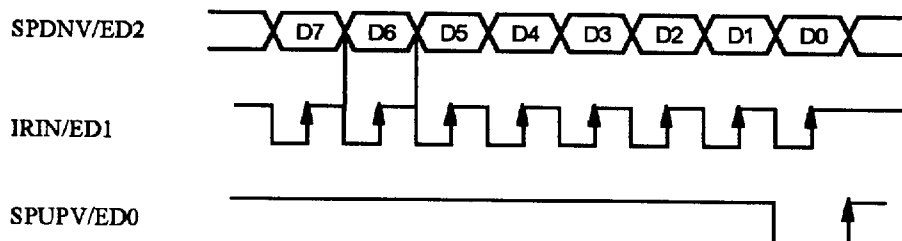
Symbol	NO.	Function
IRIN/ED1	17	Iris signal input
SPDNV/ED2	22	Shutter speed down reference voltage
SPUPV/ED0	23	Shutter speed up reference voltage

2) Parallel input electronic shutter (IRENB=low, MODE2=high)

Symbol	NO.	Mode							
SPDNV/ED2	22	H	H	H	H	L	L	L	L
IRIN/ED1	17	H	H	L	L	H	H	L	L
SPUPV/ED0	23	H	L	H	L	H	L	H	L
Shutter speed	EIA: 1/100 CCIR: 1/120	1/250	1/500	1/1000	1/2000	1/5000	1/10000	1/100000	

3) Serial input electronic shutter (IRENB=low, MODE2=high)

Serial input data format



The ED2 data is latched in the register at the ED1 rise, and retrieved internally at the ED0 rise.

External Synchronization

1) External/Internal sync selection

External or internal synchronization is selected automatically by a combination of 3 pins (VR/SYNC, HPLL and ESYNC) to which the sync signal is input externally. The table below shows the input pattern combinations.

Input pattern	VR/SYNC pin : SYNC signal HPLL pin : Open ESYNC pin : Open	VR/SYNC pin : VD signal HPLL pin : HD signal ESYNC pin : V _{DD}	VR/SYNC pin : Open HPLL pin : Open ESYNC pin : Open
EXT pin output	High	High	Low
Sync state	External sync	External sync	Internal sync

Note) Operation is possible even if the VD cycle of the VD input in the VD/HD sync mode is longer than normal.

The EXT pin is the external/internal sync identification signal output pin. This output signal can be used as the signal to select LC oscillation for expanding the lock range for external synchronization or the oscillator for improving the oscillation accuracy for internal synchronization.

2) Modes for external synchronization

		Field accumulation	Frame accumulation
SYNC synchronization	Interlace	O	O
	Non-interlace	X (Cannot be accomplished since interlace operation is the prior condition)	X (Cannot be accomplished since interlace operation is the prior condition)
VD/HD synchronization	Interlace	O	O
	Non-interlace	O	X (Not practically applicable since the sensitivity is halved)

3) Reset operation

SYNC synchronization

The VR1 signal component is extracted from the SYNC signal supplied externally and, for EIA, V reset is performed so that the VD pulse falls at the count of 259H (262.5-3.5H) from the fall of the VR1 pulse. For CCIR, it is reset in such a way that the VD pulse falls at the count of 309H (312.5-3.5H). For these reasons, it is a prerequisite that the SYNC signal input comply with the EIA or CCIR standard.

VD/HD synchronization

V reset is performed so that the VD pulse 1H later after detecting the fall of the VD(VDR) pulse supplied externally. Therefore, this enables V reset operation regardless of the field line number. The phase difference between the VDR pulse and HD pulse which is locked horizontally at PLL circuit identifies whether the field is odd or even.
(VDR must have a pulse width of 2H or more.)



Mode Control

Symbol	NO.	I/O	Low	High	Remarks
ENB	14	I	XSUB stop	XSUB output	
IRENB	15	I	Electronic shutter	Auto iris	Valid only when ENB is high.
MODE2	16	I	Serial input	Parallel input	Valid only when ENB is high and IRENB is low
IRIN/ED1	17	I	Auto iris control signal input pin (IRENB = high) Shutter speed setting pin (IRENB = low)		Valid only when ENB is high.
SPDNV/ED2	22	I			
SPUPV/ED0	23	I			
MODE1	27	I	EIA	CCIR	
FL/FR	28	I	Odd field	Even field	Valid only when MODE3 is high and EXT is low.
			Field accumulation	Frame accumulation	Valid in all other modes.
HPLL	38	I	Internal sync : HPLL (open) VR/SYNC (open) SYNC sync : HPLL (open) VR/SYNC (SYNC input) VD/HD sync : HPLL (HD input) VR/SYNC (VD input)		
VR/SYNC	39	I			
ESYNC	40	I	SYNC sync Internal sync	VD/HD sync	
MODE3	41	I	Interlace	Non-interlace	Valid only when EXT is low.
MODE4	42	I	EIA : 262H CCIR : 312H	EIA : 263H CCIR : 313H	Valid only when EXT is low and MODE 3 is high.
EXT	37	O	Internal sync	External sync	Switchover between internal and external sync is automatically identified by input state at Pins 38, 39 and 40.

Mode Tables

1) Internal sync mode

HPLL pin (Pin 38) : Open
VR/SYNC pin (Pin 39) : Open
ESYNC pin (Pin 40) : Open

	Interlace		Non-interlace			
			Odd field *2		Even field *2	
	Field readout	Frame readout	Field readout	Frame readout	Field readout	Frame readout
XSUB pulse OFF*1	O	O	O	X	O	X
Electronic shutter ON	O	O	O	X	O	X
Auto iris ON	O	O	O	X	O	X

*1 EIA for 1/60 s accumulation ; CCIR for 1/50 s accumulation

*2 Line number is 262H or 263H for EIA and 312H or 313H for CCIR.

O : Can be used.

X : Cannot be used.

2) SYNC sync (external sync) mode

HPLL pin (Pin 38) : Open
VR/SYNC pin (Pin 39) : SYNC input
ESYNC pin (Pin 40) : Open

	Interlace		Non-interlace			
			Odd field *2		Even field *2	
	Field readout	Frame readout	Field readout	Frame readout	Field readout	Frame readout
XSUB pulse OFF*1	O	O	X	X	X	X
Electronic shutter ON	O	O	X	X	X	X
Auto iris ON	O	O	X	X	X	X

*1 EIA for 1/60 s accumulation ; CCIR for 1/50 s accumulation

*2 Line number is 262H or 263H for EIA and 312H or 313H for CCIR.

O : Can be used.

X : Cannot be used.

3) VD/HD sync (external sync) mode

HPLL pin (Pin 38) : HD input
VR/SYNC pin (Pin 39) : VD input
ESYNC pin (Pin 40) : VDD (power supply)

	VD input with normal cycle						VD Input with longer cycle than normal Interlace	
	Interlace		Non-interlace					
			Odd field *2		Even field *2			
	Feild readout	Frame readout	Feild readout	Frame readout	Feild readout	Frame readout	Feild readout	Frame readout
XSUB pulse OFF*1	O	O	O	X	O	X	O	X
Serial input electronic shutter ON	O	O	O	X	O	X	X	X
Parallel input electronic shutter ON	O	O	Δ	X	Δ	X	X	X
Auto iris ON	O	O	O	X	O	X	X	X

*1 EIA for 1/60 s accumulation ; CCIR for 1/50 s accumulation

*2 Line number is 262H or 263H for EIA and 312H or 313H for CCIR.

O : Can be used.

Δ : The shutter speed may change from its value in the interlace mode.

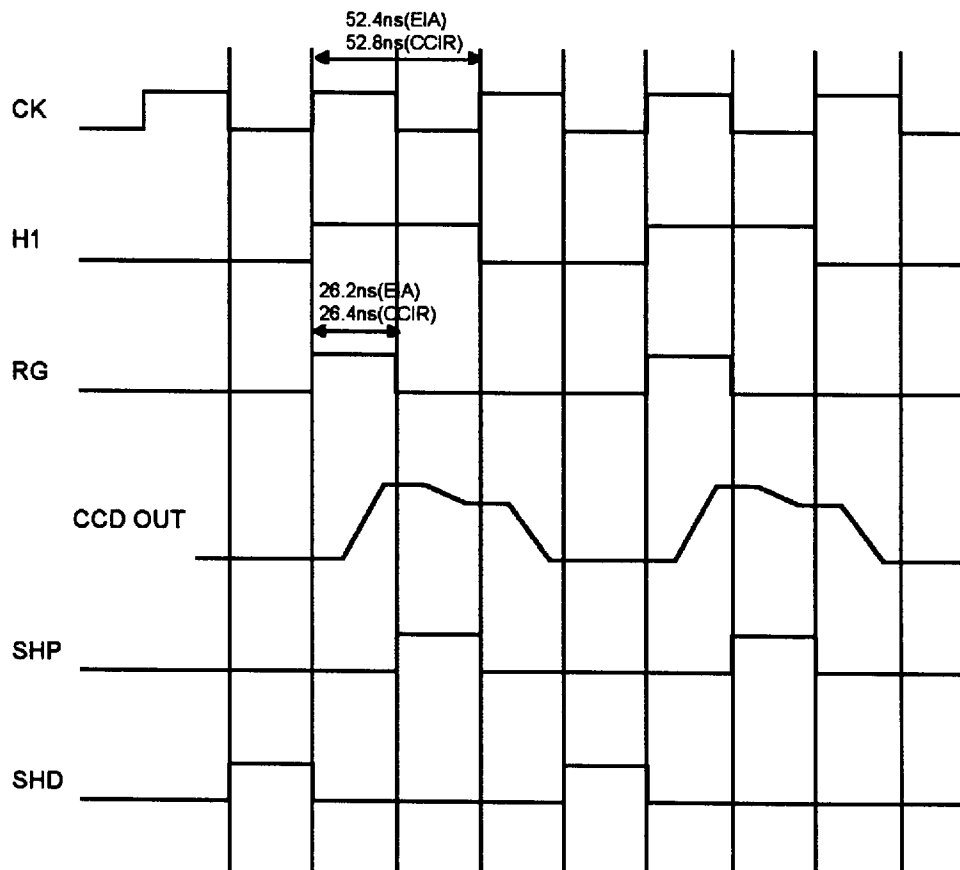
X : Cannot be used.

Note) Only in the VD/HD sync mode, the external synchronization is possible during which VD pulses with longer cycle than normal are input to the VR/SYNC pin.

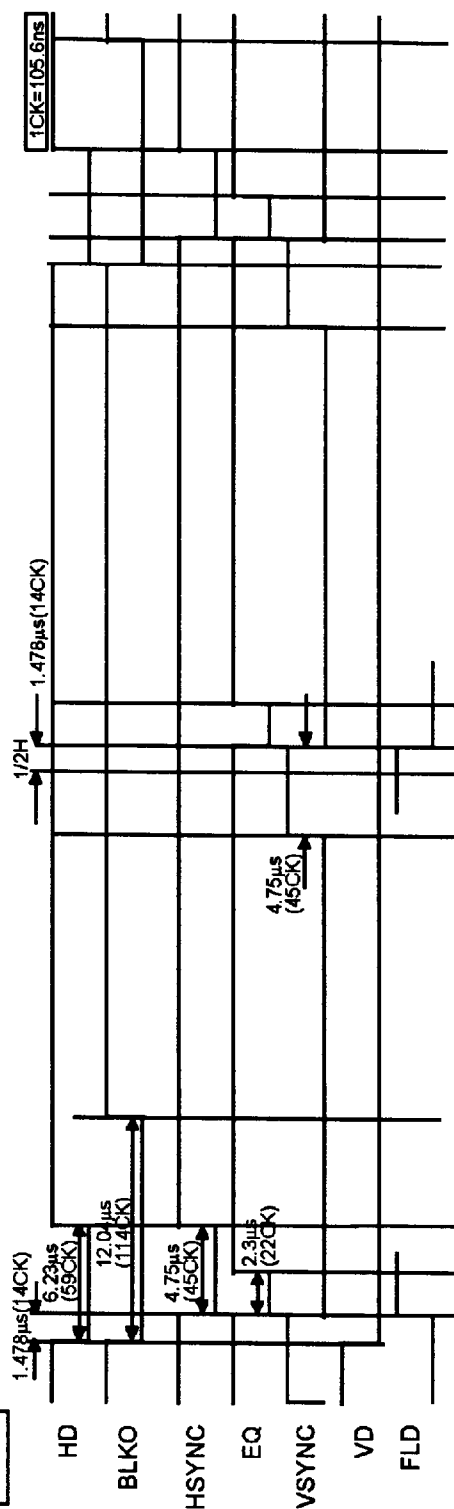


(Timing Chart 1) High-Speed phase

EIA/CCIR



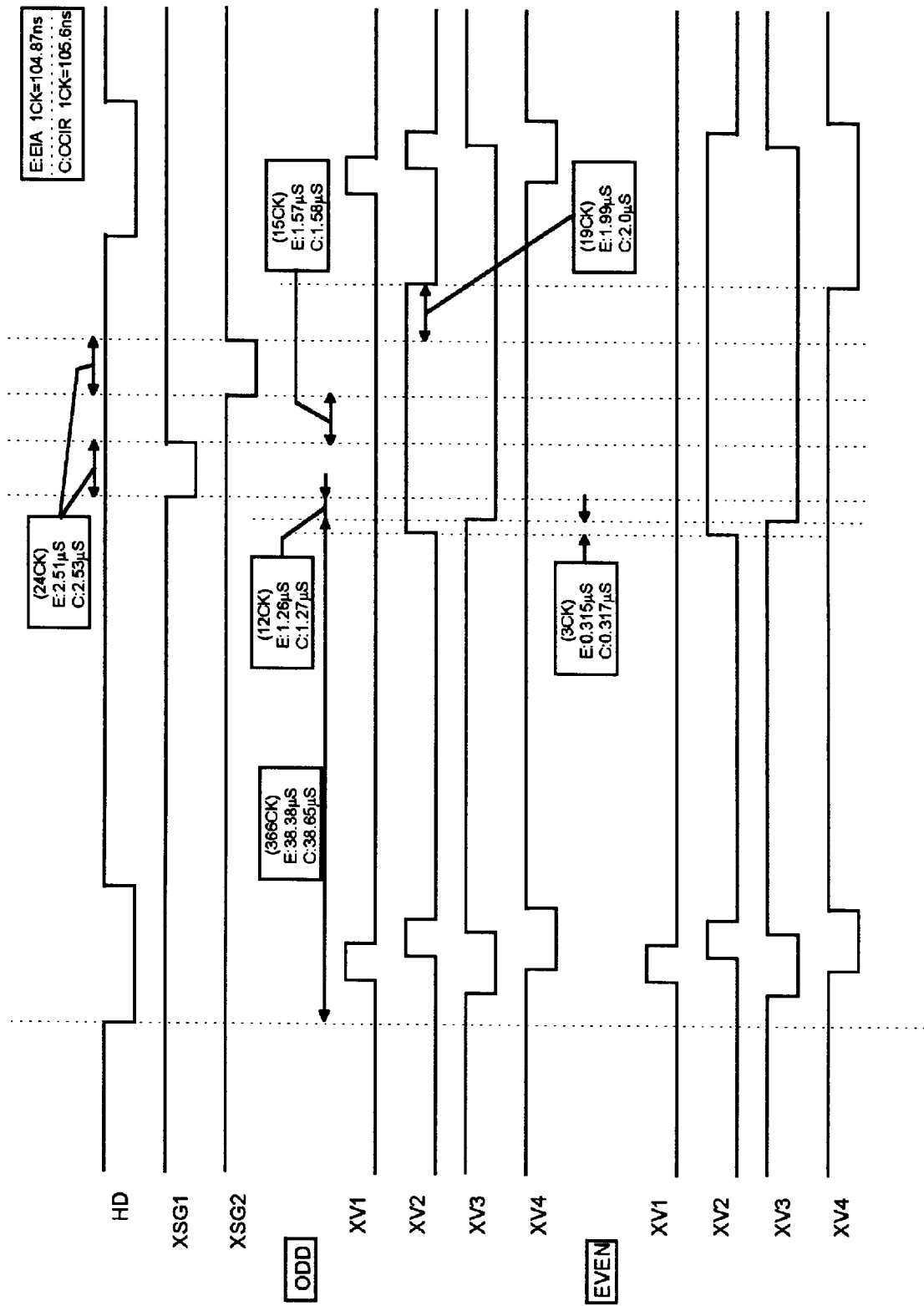
EIA





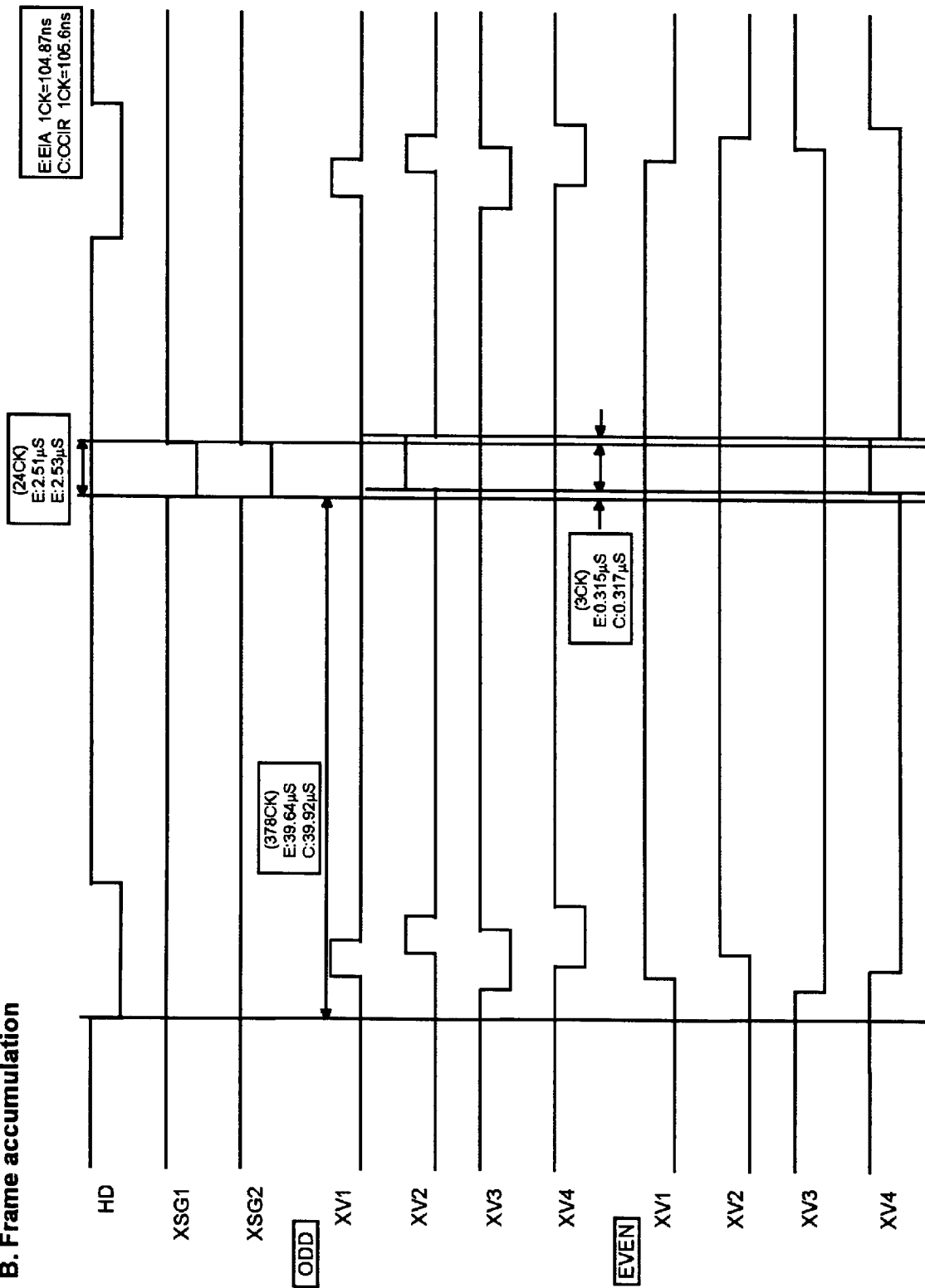
(Timing Chart 3) Charge Readout Timing

A. Field accumulation





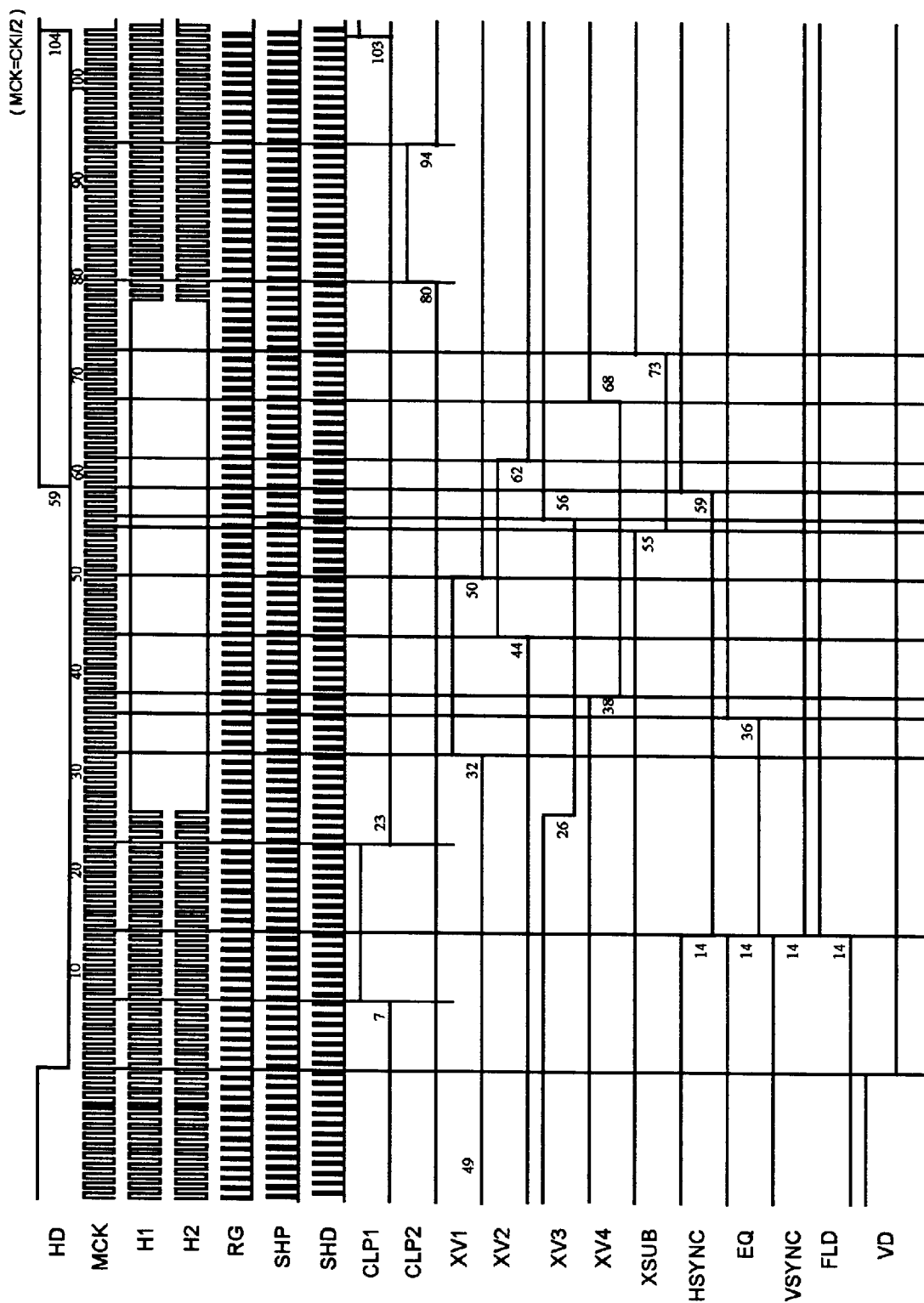
B. Frame accumulation





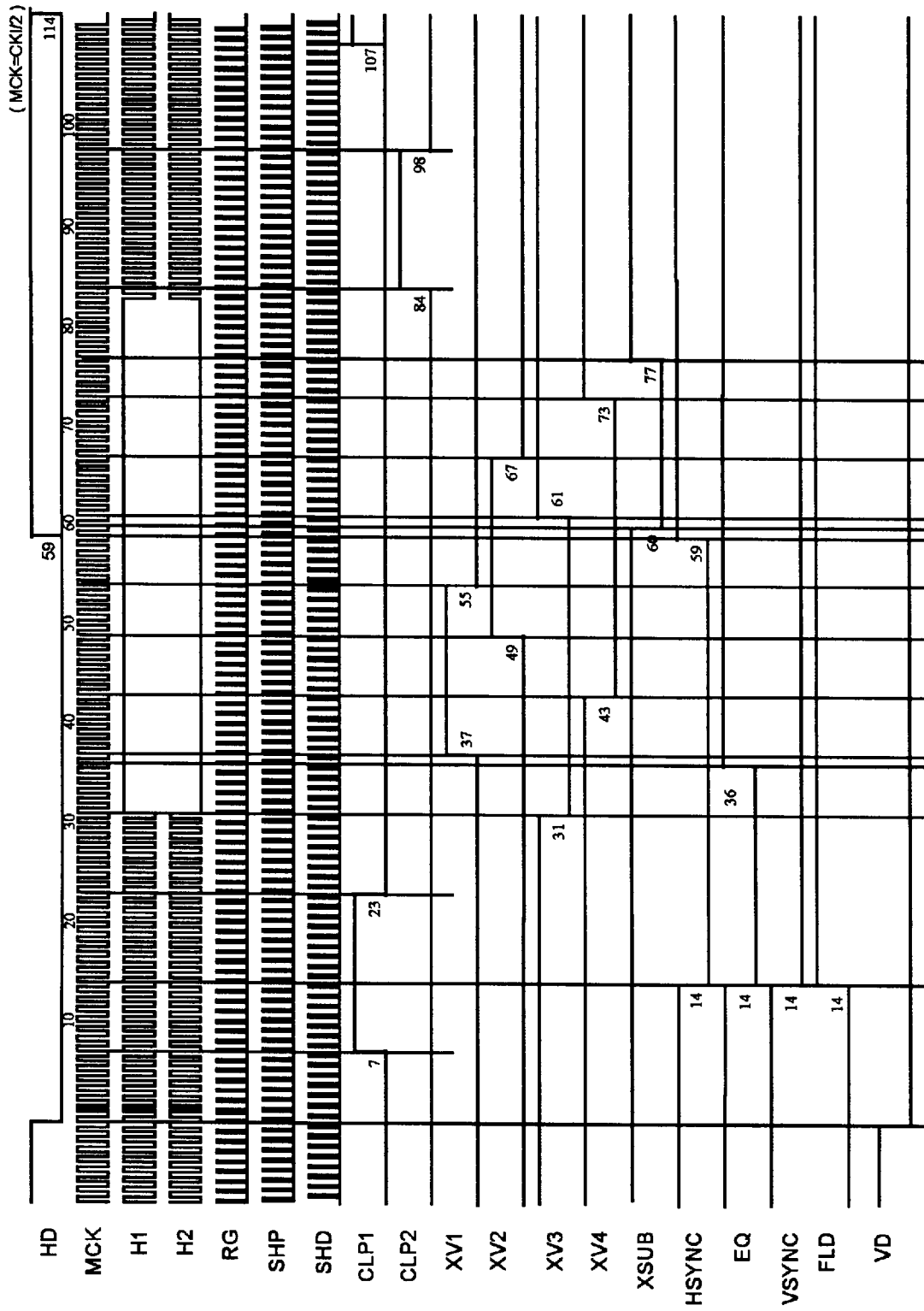
(Timing Chart 4)

A. H direction, EIA

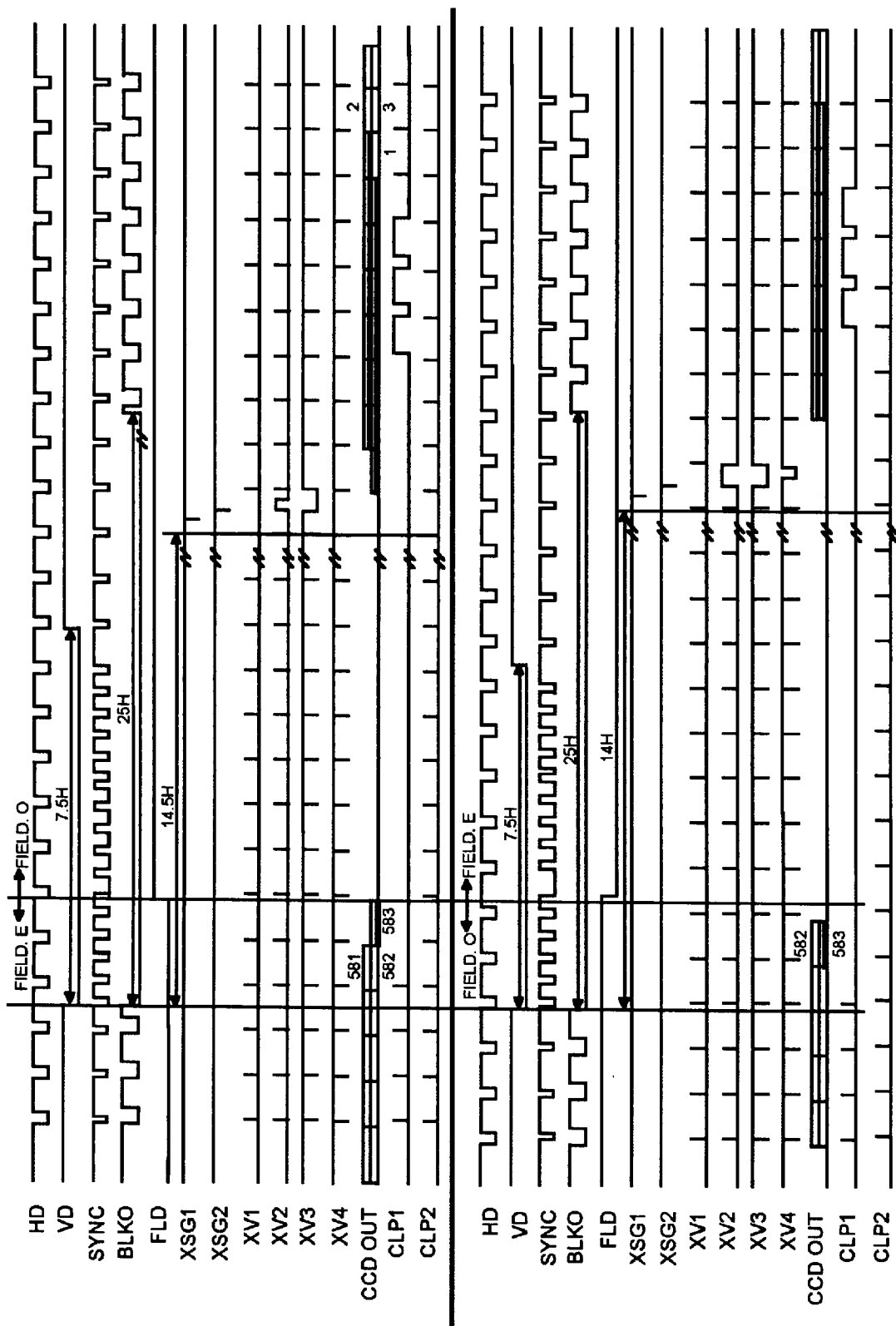




B. H direction, CCIR



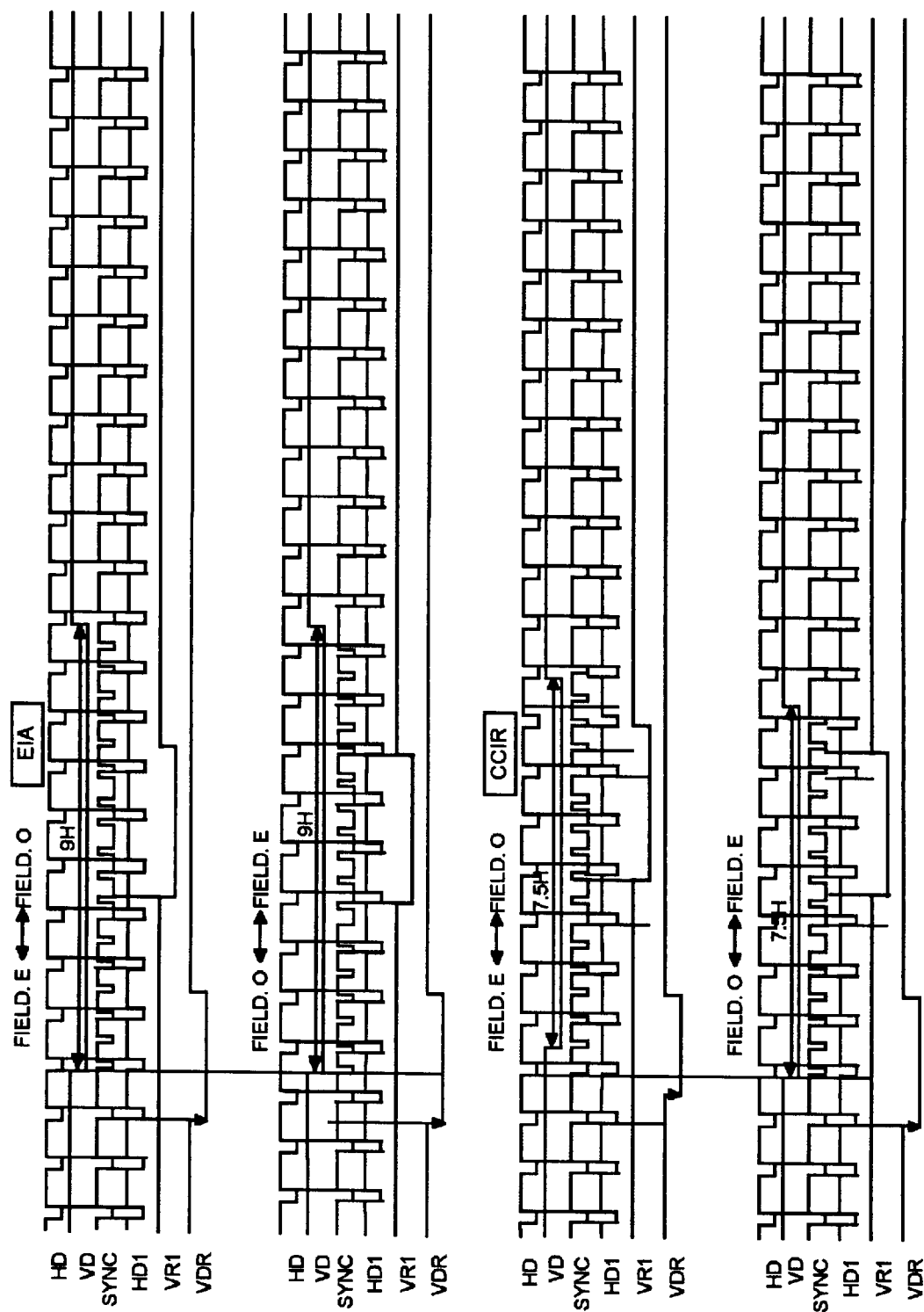
B. V direction, CCIR





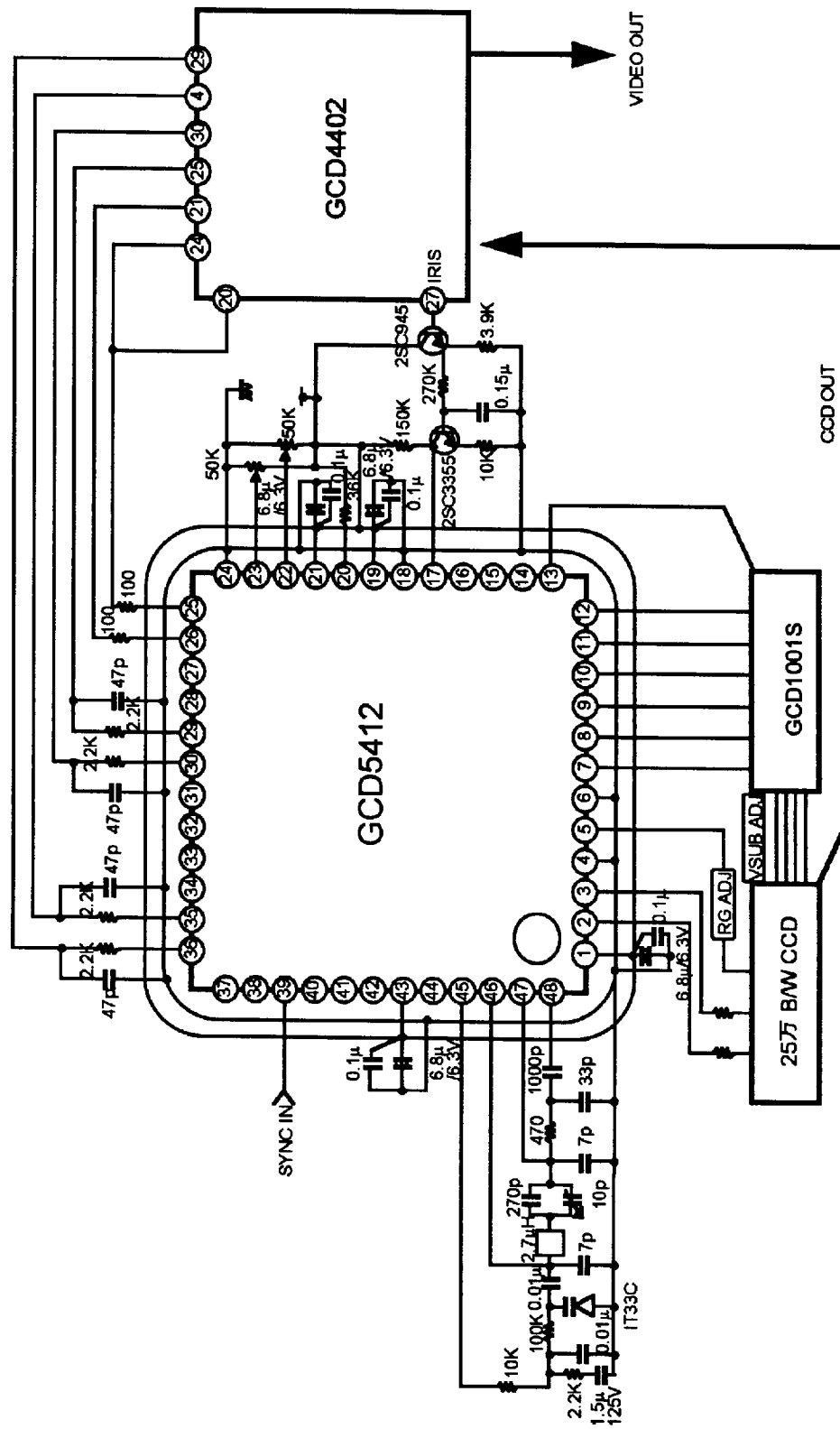
(Timing Chart 6)

External Synchronization reset Operation

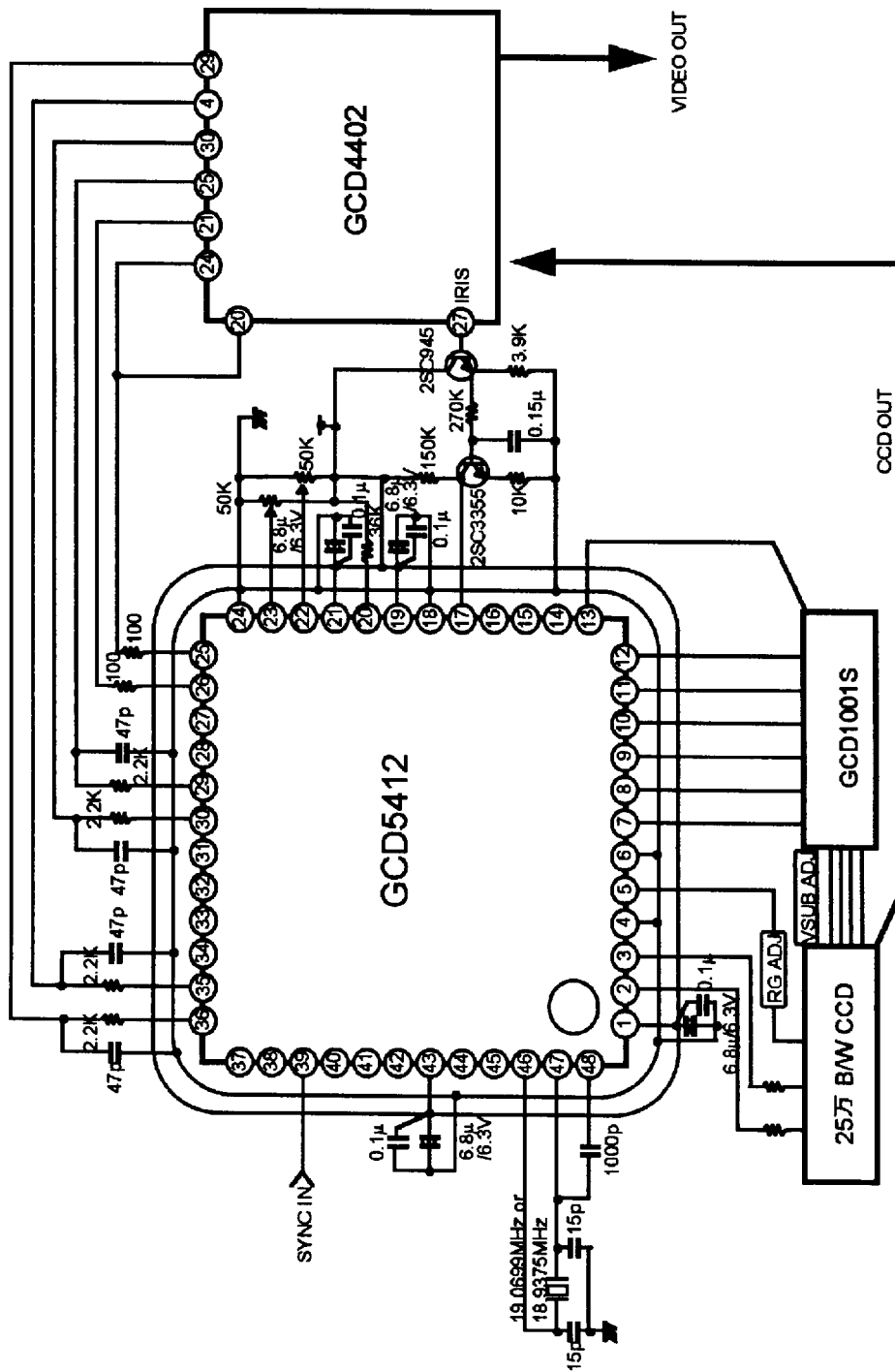




Application Circuit (for External sync.)



Application Circuit (for External sync.)

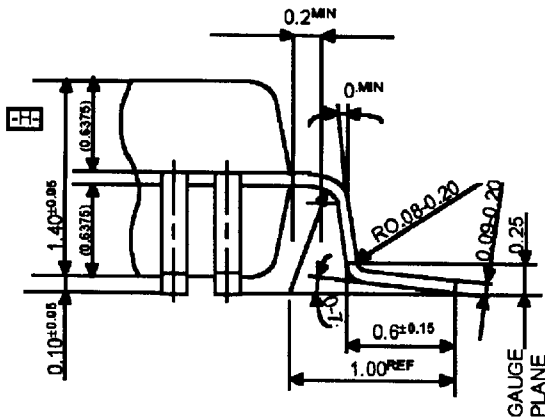
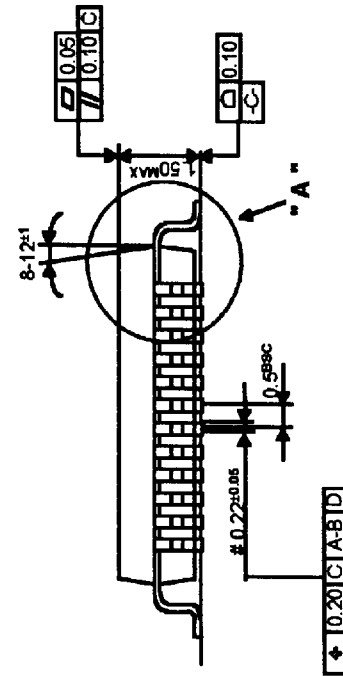
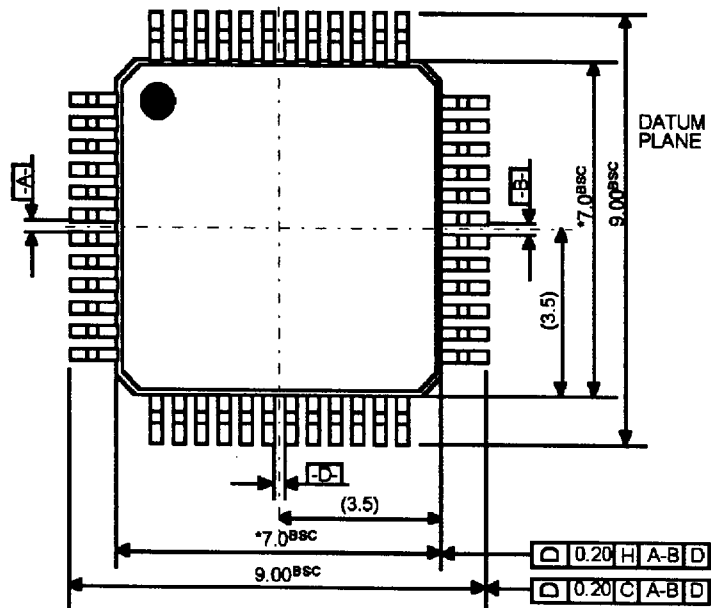




Package Outline

48pin TQFP(PLASTIC)

UNIT : mm



DETAILS of " A "

Note)

1. DIMENSION * MARK DOES NOT INCLUDE MOLD FLASH
2. DIMENSION # MARK DOES NOT INCLUDE DAMBAR PROTRUSION
3. UNSPECIFIED IS ACCORDING TO JEDEC MO-136, VARIATION "BE"