an Intel company

STM-4/STM-1/E4 3.3 V Multifunction Transmitter and Receiver GD16591A/GD16592A

General Description

The GD16591A and GD16592A is a front-end transmitter/receiver chip set designed for multiple line interfaces:

- STM-4 / OC-12
- STM-1 / OC-3
- PDH E4

This chip set is designed to interconnect the high speed line interface to standard CMOS ASICs providing low speed data interface.

The GD16591A and GD16592A devices are designed for use in both electrical and optical line interface modules. The devices support line speeds of:

- 140/155 Mbit/s NRZ mode for E4/ OC-3/STM-1 for an optical line interface.
- 280/311 Mbit/s for E4/OC-3/STM-1 in CMI mode for electrical line interface, where en-/decoding is made at the system site.
- 622 Mbit/s NRZ mode line speed for OC-12/STM-4 operation.

The on-chip VCO and PLL blocks for clock generation eliminate the need for an external high-speed clock signal.

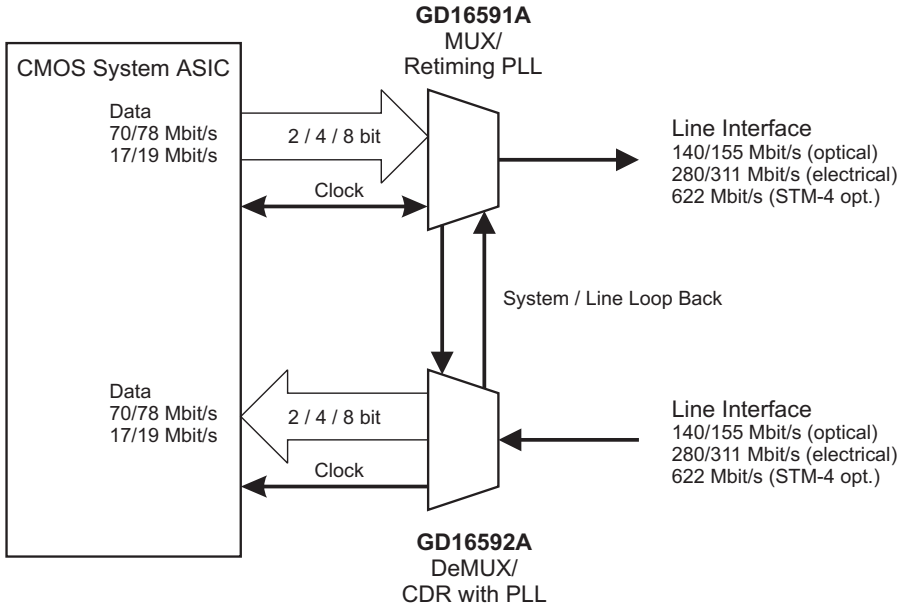
The GD16592A comprises a Limiting Input Amplifier (LIA), Clock & Data Recovery, and a configurable DeMUX circuit. The LIA offers a differential input sensitivity of 10 mV peak to peak for the high-speed serial input. A Lock Detect output monitors the PLL locked onto the received serial data.

The low-speed interface I/O´s are LVTTL-level, and the high-speed I/O´s are differential LVPECL levels (The LIA input is usable as LVPECL input).

System (local) Loop-back and Line (remote) Loop-back functions offer simplified manufacturing and field testing.

Low power consumption is achieved by the 3.3 V single power supply and by omitting all circuitry, which can easily be implemented in the low speed system ASIC, thus reducing the overall power consumption.

The devices are housed in 48 pin EDQUAD TQFP™ plastic packages.



Features

General

- Low jitter on-chip VCO and PLL.
- Jitter performance exceeds the recommendations of ITU-T and Bellcore.
- The chip set offers seven line and system speed mode:
  622 Mbit/s ↔ 78 Mbit/s, 8 bit
  311 Mbit/s ↔ 78 Mbit/s, 4 bit
  155 Mbit/s ↔ 78 Mbit/s, 2 bit
  155 Mbit/s ↔ 19 Mbit/s, 8 bit
  280 Mbit/s ↔ 70 Mbit/s, 4 bit
  140 Mbit/s ↔ 70 Mbit/s, 2 bit
  140 Mbit/s ↔ 17 Mbit/s, 8 bit
- Four phase selectable clock to data timing at parallel interface.
- Selectable reference clock input frequencies:
  17.408/19.44MHz, 34.816/ 38.88MHz, and 69.632/77.76MHz.
- Loop Back for System & Line test modes.
- 48 pin EDQUAD TQFP™ packages.
- Single supply: 3.1 ... 3.6 V.

GD16591A (Transmitter)

- 8:1 / 4:1 / 2:1 MUX.
- Differential transmitted clock output.
- LVPECL data outputs.
- Optional forward/counter clocking scheme.
- Power dissipation, typ.: 350 mW

GD16592A (Receiver)

- 1:8 / 1:4 / 1:2 DeMUX.

Functional Details

General

The Transmitter and Receiver functional blocks are split up into two devices in order to reduce cross talk and pin count per device.

The telecommunication system (line speed group) is choosen by the select pin ($\overline{\text{SELPDH}}$):

- For SDH/SONET (622/311/155 Mbit/s) set $\overline{\text{SELPDH}}$ High.
- For PDH (280/140 Mbit/s) set $\overline{\text{SELPDH}}$ Low.

The devices can operate in different line and system speed modes; selected by DSEL1, DSEL2 and $\overline{\text{SELPDH}}$, see Table 1.

The bit order on the low speed parallel interface is defined with bit 0 as the first bit transferred (ID0 for the transmitter and OD0 for the receiver).

The bit rate per connection can be kept at 78(70) Mbit/s regardless of the line speed. In addition a separate low speed 1:8 mode support the transmission of 155(140) Mbit/s serial to 19(17) Mbit/s, 8 bit parallel. All data pins are used.

Both devices have a selectable clock divider for the system reference clock, which allows the circuits to be driven from either 19 (17), 38(35), or 78(70) MHz reference, independantly of the line and system speed. The reference clock frequency is selected by RSEL1, RSEL2, and $\overline{\text{SELPDH}}$, see table 2.

Connecting the differential Line Loop Signals and Clocks (LLxxx) between GD16591A and GD16592A allows clock recovered loop-back of the received line signal, when $\overline{\text{LLB}}$ on both devices is low.

Connecting the differential System Loop Signals (SLSxx) between GD16591A and GD16592A allows system loop-back, when $\overline{\text{SLB}}$ on both devices is low.

Both circuits comprise fully integrated PLL functions for re-timing data at the transmit site, and for clock and data recovery at the receive site.

A passive loop filter (consisting of a resistor and a capacitor) is used for both devices. The external loop filter connecting OUCHP to VCTL is shown in Figure 1 (for the transmitter GD16591A) and Figure 2 (for the receiver GD16592A). The loop filter values are optimized at the evaluation board GD90591/592.

The optimal values depends on the actual application. The suggested values in Figures 1 and 2 are optimized for best jitter transfer at the evaluation board.

The loop filter values should be optimized for the actual application.

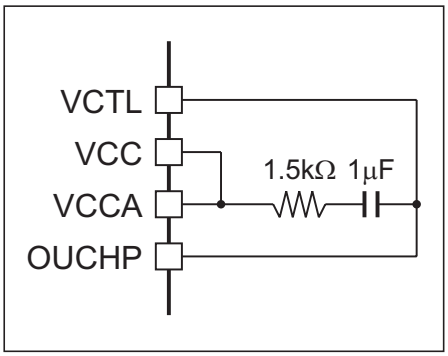


Figure 1. *Loop Filter for the Transmitter, GD16591A.*

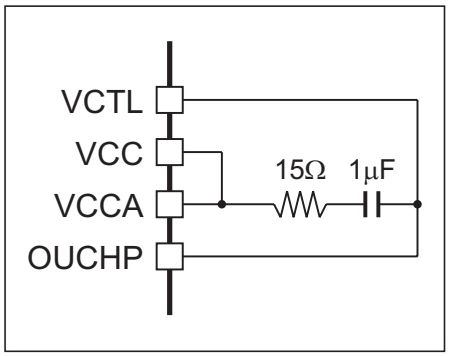


Figure 2. *Loop Filter for the Receiver, GD16592A.*

$\overline{\text{SELPDH}}$	DSEL1	DSEL2	Line Speed	System Speed	Used Bits
0	0	0	140 Mbit/s	70 Mbit/s	0 & 1
0	0	1	140 Mbit/s	17 Mbit/s	0...7
0	1	0	280 Mbit/s	70 Mbit/s	0...3
0	1	1	---	---	---
1	0	0	155 Mbit/s	78 Mbit/s	0 & 1
1	0	1	155 Mbit/s	19 Mbit/s	0...7
1	1	0	311 Mbit/s	78 Mbit/s	0...3
1	1	1	622 Mbit/s	78 Mbit/s	0...7

Table 1. *Line and system speed mode selection.*

$\overline{\text{SELPDH}}$	RSEL1	RSEL2	Ref. Clock
0	0	0/1	69.632 MHz
0	1	0	34.816 MHz
0	1	1	17.408 MHz
1	0	0/1	77.76 MHz
1	1	0	38.88 MHz
1	1	1	19.44 MHz

Table 2. *Reference clock frequency selection.*

The Transmitter - GD16591A

The schematic block diagram of GD16591A is shown in Figure 3.

By the select signal (CSEL) two different reference clock inputs can be selected (CKR0/CKR1). This allows for line timing in normal operation with a selection of a separate reference when the received line input data is flawed. Thus, allowing forwarding alarm status in the event of a loss of received data.

Forward Clocking

Co-directional timing for input data is provided. The phase can with the select pins PSEL1-2 be set to 0°/ 90°/ 180°/ 270° difference between data input sampling and reference clock (CKR0/CKR1).

When forward clocking, the frequency of the reference clock must be identical to the input data bit rate.
I.e. for 78(70) Mbit/s use 78(70) MHz reference clock, and for 19(17) Mbit/s use 19(17) MHz reference clock. Refer to AC Characteristics on page 12.

Counter Clocking

In addition, contra directional timing is provided. The phase between input and CKOUT is adjustable with (0°/90°/180°/270°). Refer to AC Characteristics on page 12.

CKOUT is kept synchronous to the reference clock by the Phase Frequency Comparator (PFC).

Outputs

The outputs from the multiplexer is fed to differential LVPECL output stages. See Figures 4 and 5 for output temination.

The serial data output (SOP/SON) are accompanied by a serial clock output (COP/CON). See timing data on page 12.

SLSOP/SLSON is enabled when $\overline{SLB}$ is low. When $\overline{SLB}$ is high (e.g. by internal pull-up resistor) SLSOP = 0 and SLSON = 1; thus avoiding noise injection at normal operation.

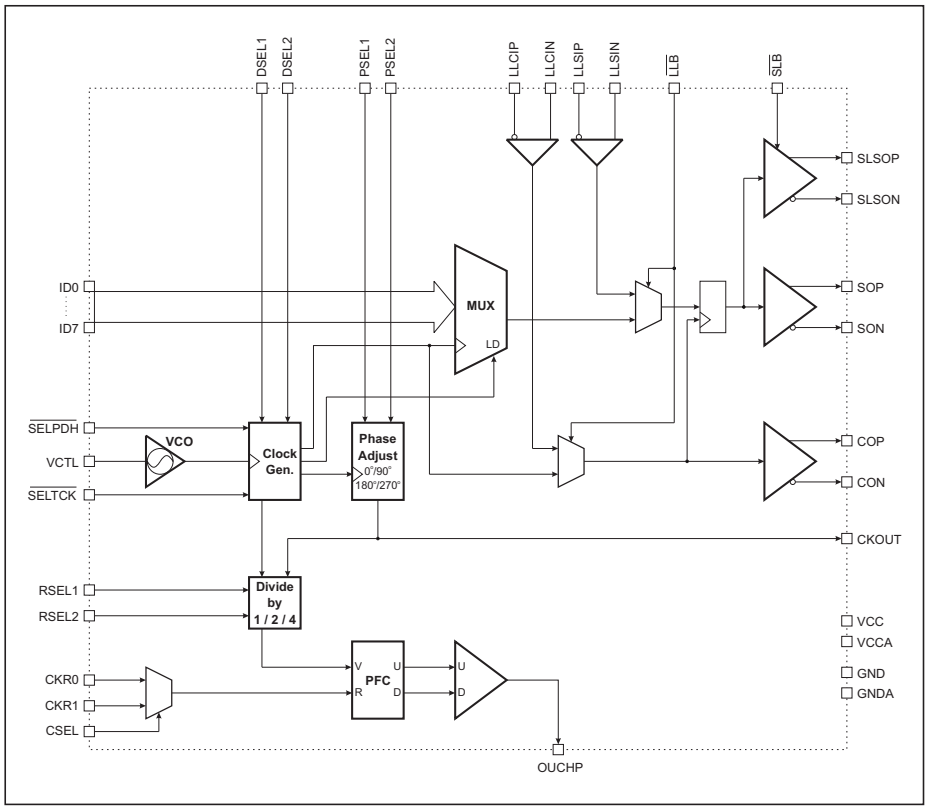


Figure 3. *The GD16591A Multifunction Transmitter.*

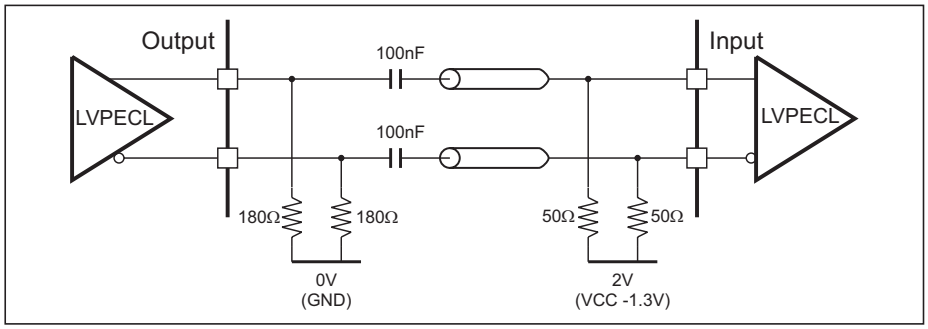


Figure 4. *LVPECL Output Termination, AC-coupled.*

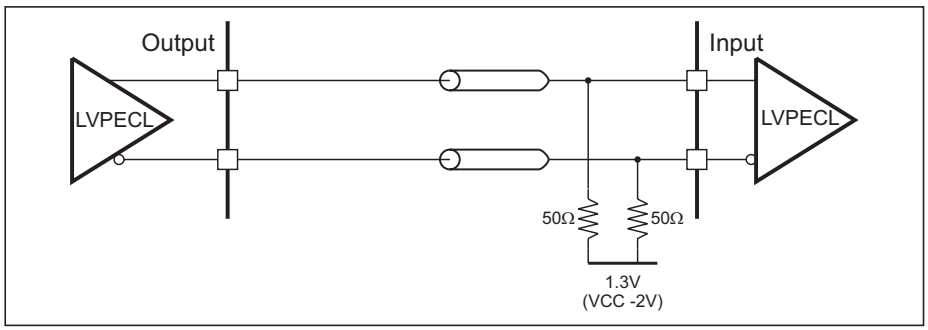


Figure 5. *LVPECL Output Termination, DC-coupled.*

The schematic block diagram of GD16592A is shown in Figure 6.

Lock Detect Circuit

The lock detect circuit continuously monitors the frequency difference between the reference clock and the divided VCO clock. If the reference clock and the divided VCO frequency differs by more than 500 ppm (or 2000 ppm, selectable), it switches the PFC into the PLL in order to pull the VCO back inside the lock-in range. This mode is called **the acquisition mode**.

The PFC is used to ensure predictable lock up conditions for the GD16592A by locking the VCO to an external reference clock source. It is only used during acquisition and pulls the VCO into the lock range where the Bang-Bang phase detector is capable of acquiring lock to incoming data. The PFC is made with digital set/reset cells giving it a true phase and frequency characteristic.

Once the VCO is inside the lock-range the lock-detection circuit switches the Bang-Bang phase detector into the PLL in order to lock to the data signal. This mode is called **CDR mode**.

Bang-Bang Phase Detector

The Bang-Bang phase detector is used in **CDR mode** as a true digital type detector, producing a binary output. It samples the incoming data twice each bit period: once in the transition of the (previous) bit period and once in the middle of the bit period. When a transition occurs between 2 consecutive bits - the value of the sample in the transition between the bits will show whether the VCO clock leads or lags the data. Hence the PLL is controlled by the bit transition point, thereby ensuring that data is sampled in the middle of the eye, once the system is in CDR mode. The external loop filter components control the characteristics of the PLL.

The binary output of either the PFC or the Bang-Bang phase detector (depending of the mode of the lock-detection circuit) is fed to a charge pump capable of sinking or sourcing current or tristating. The output of the charge pump is filtered through the loop filter and controls the tuning-voltage of the VCO.

As a result of the continuous monitoring lock-detect circuit the VCO frequency never deviates more than 500 ppm (2000 ppm) from the reference clock before the PLL is considered to be 'Out of Lock'. Hence the acquisition time is predictable and short and the output clock CKOUT is always kept within the 500 ppm (2000 ppm) limits, ensuring safe clocking of down stream circuitry.

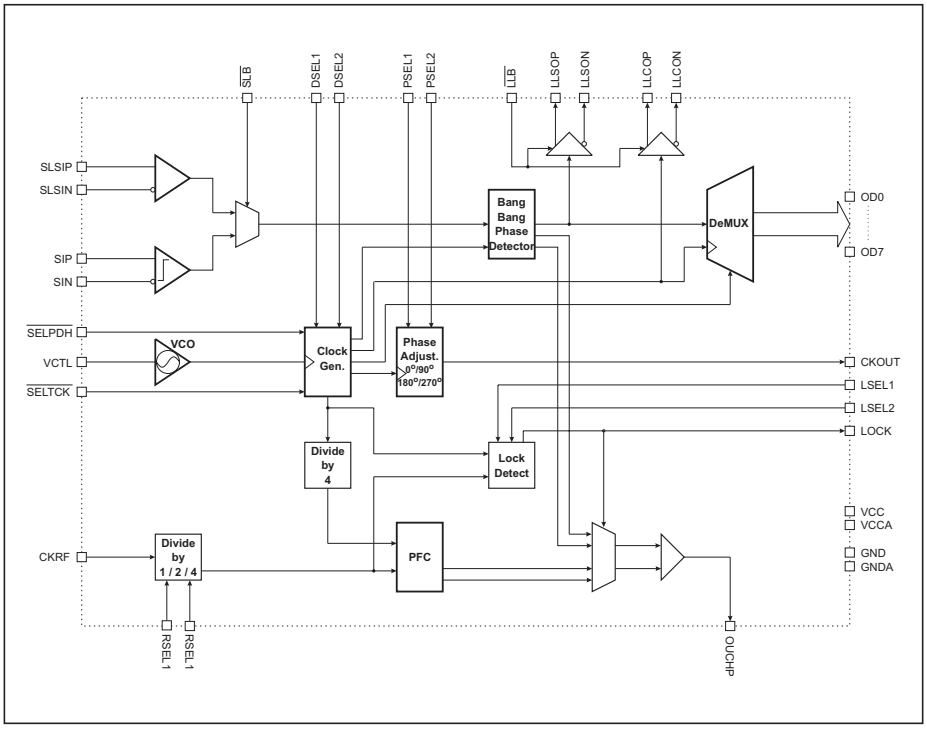


Figure 6. *The GD16592A Multifunction Receiver.*

The LOCK Signal

The status of the lock-detection circuit is given by the LOCK signal. In CDR mode LOCK is steady high. In acquisition mode LOCK is alternating indicating the continuous shifts between the Bang-Bang Detector (high) and the PFC (low).

The LOCK output may be used to generate a pseudo *Loss Of Signal* (LOS). The time for LOCK to assert is predictable and short, equal to the time to go into lock, but the time for LOCK to de-assert must be considered. When the line is down (i.e. no information received) the optical receiver circuit may produce random noise. It is possible that this random noise will keep the GD16592A within the 500 ppm (2000 ppm) range of the line frequency, hence LOCK will remain asserted for a non-deterministic time. This may be prevented by injecting a small current at the loop filter node, which actively pulls the PLL out of the lock range when the output of the phase detector acts randomly.

The negligible penalty paid is a static phase error on the sampling time in the decision gate. However, due to the nature of the phase detector the error will be small (few degrees), forcing the loop to be at one edge of the error-function shaped transfer characteristic of the detector.

Inputs

The input amplifier (pin SIP / SIN) is designed as a limiting amplifier with a sensitivity of 10 mV (differential). Standard LVPECL levels may be applied as well.

The inputs may be either AC or DC coupled. If the inputs are AC coupled the amplifier features an internal offset cancelling DC feedback. Notice that the offset cancellation will only work when the input is differential and AC-coupled as shown in the Figures 7 and 8 on page 5.

The serial input SLSIP/SLSIN is selected when $\overline{\text{SLB}}$ is low.

Outputs

The CKOUT provides the necessary control for clocking the received data into the system ASIC. The phase can be adjusted with PSEL1-2 (0°/90°/180°/270°).

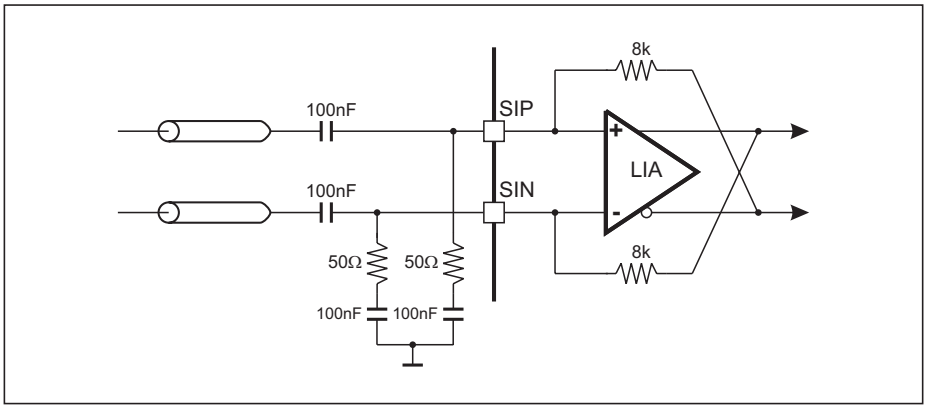


Figure 7. *AC Coupled Input (using internal offset compensation).*

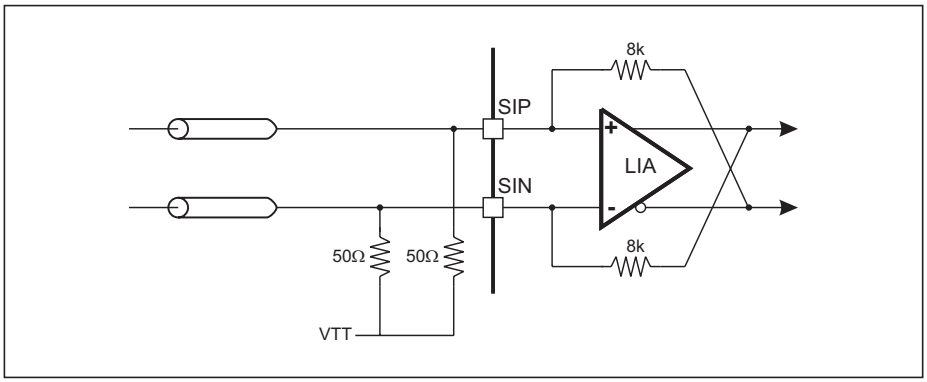


Figure 8. *DC Coupled Input (ignoring internal offset compensation). V_{TT} depends on the termination requirements of the previous stage, and the resulting amplitude on the input.*

Practical Considerations

The PCB must be designed with shortest possible conductors for the signals to the line interfaces. These connections should be designed as transmission lines. De-coupling capacitors should be applied to each power supply pin. Care should be taken to reduce ground bounce.

The line loop signal and clock must be terminated close to the transmitter device (GD16591A).

The system loop signal must be terminated close to the receiver device (GD16592A).

Pin List, GD16591A - Transmitter

Mnemonic:	Pin No.:	Pin Type:	Description:
CKR0, CKR1 CSEL	38, 40 39	LVTTL IN	Reference clock inputs selectable by CSEL. Usable for forward clocking (co-directional timing), see AC-characteristics on page 12. The CKRx input must be noise free, since noise injected here passes onto the line. The frequency is determined by RSEL1-2. Maximum frequency is 78 MHz. CSEL=0 => CKR0; CSEL=1 =>CKR1
ID0..ID7	31, 29, 28, 22, 21, 19, 18, 17	LVTTL IN	Data input port to MUX. See DSEL1-2 for bit use. ID0 is the first bit transmitted. See PSEL1-2 for timing.
DSEL1, DSEL2	27, 26	LVTTL IN	DSEL1 DSEL2 Line speed System speed Used bit 0 0 155 Mbit/s 78 Mbit/s 0 & 1 0 1 155 Mbit/s 19 Mbit/s 0 .. 7 1 0 311 Mbit/s 78 Mbit/s 0 .. 3 1 1 622 Mbit/s 78 Mbit/s 0 .. 7
$\overline{\text{SELPDH}}$	1	LVTTL IN	PDH(E4) mode select: 0 Line speeds 140 or 280 Mbit/s 1 Line speeds 155, 311, or 622 Mbit/s $\overline{\text{SELPDH}}$ is used as test clock input when SELTCK is low.
RSEL1, RSEL2	35, 34	LVTTL IN	Reference clock frequency select: RSEL1 RSEL2 CKREF (MHz) 0 0/1 77.76 1 0 38.88 1 1 19.44
PSEL1, PSEL2	42, 41	LVTTL IN	IDx input phase versus CKOUT/CKRx select: (Note 2) PSEL2 PSEL1 0 0 T_{DEL} = 0° 0 1 T_{DEL} = 90° 1 0 T_{DEL} = 180° 1 1 T_{DEL} = 270°
$\overline{\text{SELTCK}}$	47	LVTTL IN	Connect to VCC. Used for test purpose (selects $\overline{\text{SELPDH}}$ as test clock when low).
$\overline{\text{LLB}}$	25	LVTTL IN	Line Loop-Back, enabled when low.
$\overline{\text{SLB}}$	3	LVTTL IN	System Loop-Back, enabled when low.
LLSIP, LLSIN	16, 15	LVPECL IN	Line Loop-back serial differential data. Connect to LLSOP/LLSON of GD16592A .
LLCIP, LLCIN	14, 13	LVPECL IN	Line Loop-back serial differential clock. Connect to LLCOP/LLCON of GD16592A.
CKOUT	32	LVTTL OUT	77.76 MHz /19.44 MHz output clock. Usable for counter clocking (contra-directional timing) .
SLSOP, SLSON	10, 9	LVPECL OUT	System loop-back serial differential data. Connect and terminate close to SLSIP/SLSIN of GD16592A.
SOP, SON	5, 4	LVPECL OUT	Differential data output from MUX. SOP is true output, SON is inverted.
COP, CON	8, 7	LVPECL OUT	Differential clock output from MUX.
VCTL	45	Analog IN	VCO control voltage input. Connect to OUCHP and terminate with 1 kΩ in series with 1 µF to VCCA.
OUCHP	43	Analog OUT	Charge pump output.
VCC	2, 11, 20, 23, 30, 37	PWR	+3.3 V power for core and I/O.
VCCA	44	PWR	+3.3 V power for VCO.
GND	6, 12, 24, 33, 36, 48	GND	0 V power for core and I/O.
GNDA	46	GND	0 V power for VCO.
Heat sink			Connected to GND.

Note 1: Only standard line speeds for SDH/SONET applications are indicated. For PDH (E4) usage, corresponding values apply, i.e. substitute 19 MHz clock with 17 MHz, 78 MHz with 70 MHz, 155 Mbit/s with 140 Mbit/s, 311 Mbit/s with 280 Mbit/s.

Note 2: When forward clocking, the frequency of the reference clock must be identical to the input data bit rate.

Pin List, GD16592A - Receiver

Mnemonic:	Pin No.:	Pin Type:	Description:
CKRF	32	LVTTL IN	Reference clock input (19 / 39 / 78 MHz), determined by RSEL1, RSEL2.
DSEL1, DSEL2	39, 38	LVTTL IN	DSEL1 DSEL2 Line speed System speed Used bit 0 0 155 Mbit/s 78 Mbit/s 0 & 1 0 1 155 Mbit/s 19 Mbit/s 0 .. 7 1 0 311 Mbit/s 78 Mbit/s 0 .. 3 1 1 622 Mbit/s 78 Mbit/s 0 .. 7
$\overline{\text{SELPDH}}$	1	LVTTL IN	Active low, PDH(E4) mode select: 0 Line speeds 140 or 280 Mbit/s 1 Line speeds 155, 311, or 622 Mbit/s $\overline{\text{SELPDH}}$ is used as test clock input when $\overline{\text{SELTCK}}$ is low.
RSEL1, RSEL2	3, 34	LVTTL IN	RSEL1 RSEL2 Reference clock frequency select: 0 0/1 CKRF = 78 MHz 1 0 CKRF = 38 MHz 1 1 CKRF = 19 MHz
LSEL1, LSEL2	10, 9	LVTTL IN	LSEL1 LSEL2 Lock Select inputs for clock and data recovery set-up. 0 0 Manual, Phase Freq. Comp. (PFC) 0 1 Manual, Phase Detect (BB) 1 0 Auto lock, 2000 ppm 1 1 Auto lock, 500 ppm (*Default, when not connected*)
$\overline{\text{SELTCK}}$	47	LVTTL IN	Connect to VCC. Test purpose (selects $\overline{\text{SELPDH}}$ as test clock when low).
$\overline{\text{LLB}}$	41	LVTTL IN	Line Loop-Back, enabled when low.
$\overline{\text{SLB}}$	40	LVTTL IN	System Loop-Back, enabled when low.
PSEL1, PSEL2	25, 35	LVTTL IN	PSEL2 PSEL1 ODx output phase versus CKOUT select: 0 0 T_{DEL} = 0° 0 1 T_{DEL} = 90° 1 0 T_{DEL} = 180° 1 1 T_{DEL} = 270°
SIP, SIN	4, 5	Analog IN	Differential serial data input.
SLSIP, SLSIN	7, 8	LVPECL IN	System loop-back serial differential data. Connect to SLSOP/N of GD16591A.
CKOUT	29	LVTTL OUT	Regenerated output clock (77.76 / 19.44 MHz). Used for ODx timing.
OD0...OD7	28, 27, 26, 22, 21, 19, 18, 17	LVTTL OUT	Re-timed data output from DeMUX. See DSEL1-2 for bit use. OD0 is the first bit received. See PSEL1-2 for timing.
LLSOP, LLSON	13, 14	LVPECL OUT	Line loop-back serial differential data. Connect and terminate close to LLSIP/LLSIN of GD16591A.
LLCOP, LLCON	15, 16	LVPECL OUT	Line loop-back serial differential clock. Connect and terminate close to LLCIP/LLCIN of GD16591A.
LOCK	42	LVTTL OUT	High level indicates PLL locked to incoming data signal. Low level indicates PLL out of lock.
VCTL	45	Analog IN	VCO control voltage input. Connect to OUCHP and terminate with 22 Ω in series with 1 μF to VCCA.
OUCHP	43	Analog OUT	Charge Pump output for PLL.
VCC	2, 11, 20, 23, 30, 37	PWR	+3.3 V power for core and I/O.
VCCA	44	PWR	+3.3 V power for VCO.
GND	6, 12, 24, 33, 36, 48	GND	0 V power for core and I/O.
GNDA	46	GND	0 V power for VCO.
NC	31	NC	Not Connected.
Heat sink			Connected to GND.

Note: Only standard line speeds for SDH/SONET applications are indicated. For PDH (E4) usage, corresponding values apply, i.e. substitute 19 MHz clock with 17 MHz, 78 MHz with 70 MHz, 155 Mbit/s with 140 Mbit/s, 311 Mbit/s with 280 Mbit/s.

Package Pinouts

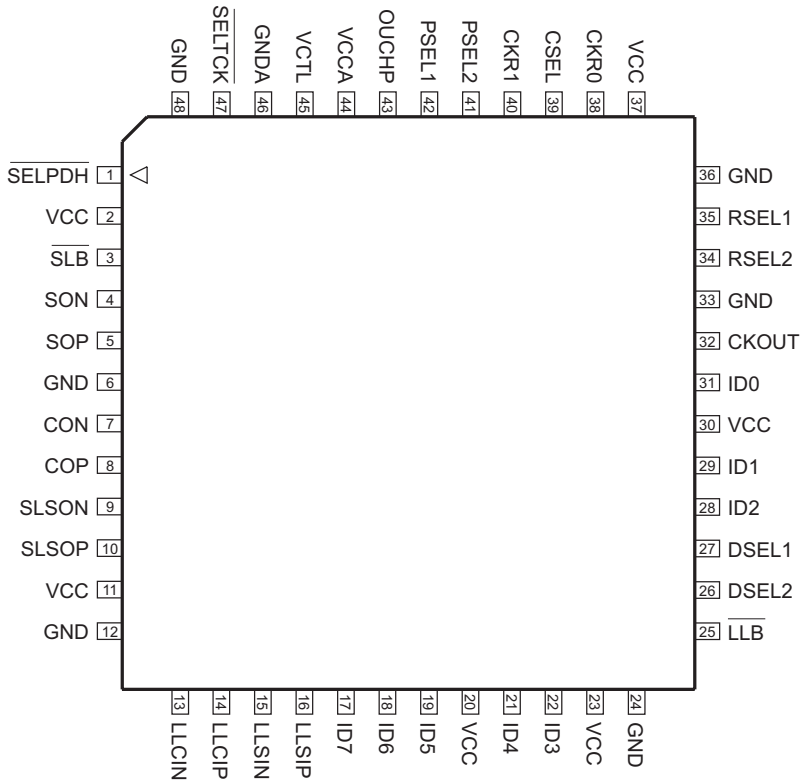


Figure 9. *GD16591A, Package 48 pin TQFP - Top View.*

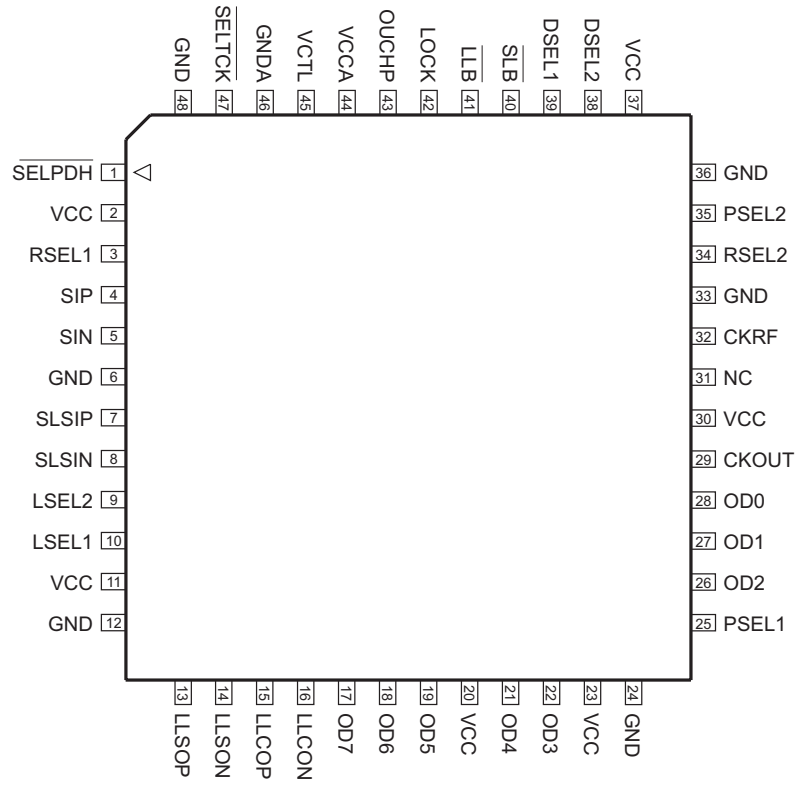


Figure 10.*GD16592A, Package 48 pin TQFP - Top View.*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in the table are referred to GND.
All currents in the table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT.:
V_{CC}, V_{CCA}	Supply Voltage		0		6	V
$V_{0\ MAX}$	Output Voltage		-0.5		V_{CC}+0.5	V
$I_{0\ MAX,\ LVPECL}$	Output Current				30	mA
$I_{0\ MAX,\ VCTL}$	Output Current				0.5	mA
$I_{OO,\ LVTTL}$	LVTTL Output Source Current				24	mA
$I_{OI,\ LVTTL}$	LVTTL Output Sink Current				-24	mA
$V_{I\ MAX}$	Input Voltage		-0.5		V_{CC}+0.5	V
$I_{I\ MAX}$	Input Current		-1.0		1.0	mA
T_0	Operating Temperature	Junction	-55		125	°C
T_S	Storage Temperature		-65		150	°C
V_{ESD}	Electro Static Discharge Voltage	Note 1		500		V

Note1: According to MIL std. 883, method 3015, Human Body Model.

Thermal Characteristics

The worst case thermal resistance from junction to ambient is Θ_{JA} = 75 °C/W in still air, using a low conductivity board (2 layers) according to JEDEC standard JESD51.3.

When using a low conductivity board with no air flow it is recommended that the heat sink is soldered to the board, and that the board is a multilayer.

DC Characteristics

$T_{AMBIENT}$ = -25 °C to 85 °C.
All voltages in the table are referred to GND.
All input signal and power currents in the table are defined positive into the pin.
All output signal currents are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{CC}, V_{CCA}	Positive Supply Voltage		3.1	3.3	3.6	V
$I_{CC,GD16591A}$	Positive Supply Current (GD16591A)	Note 1		105	130	mA
$I_{CC,GD16592A}$	Positive Supply Current (GD16592A)	Note 1		135	160	mA
$V_{SIN,SIP}$	Data Input Voltage Swing, Differential	Note 5	10		1400	mV_{P-P}
$V_{ICM,\ LVPECL}$	LVPECL Input Common Mode Voltage		V_{CC} -1.5		V_{CC} -1.1	V
$V_{IDIFF,\ LVPECL}$	LVPECL Input Differential Voltage		0.25	0.5	1.4	V
$I_{I,\ LVPECL}$	LVPECL Input Current		-100		100	µA
$V_{OH,\ LVPECL}$	LVPECL Output HI Voltage	Note 2	V_{CC} -1.2		V_{CC} -0.6	V
$V_{OL,\ LVPECL}$	LVPECL Output LO Voltage	Note 2	V_{CC} -2.0		V_{CC} -1.6	V
$V_{ODIFF,\ LVPECL}$	LVPECL Output Differential Voltage	Note 2	0.6		1.1	V
$V_{IH,\ LVTTL}$	LVTTL Input HI Voltage	Note 3, 4	2.0		V_{CC}	V
$V_{IL,\ LVTTL}$	LVTTL Input LO Voltage	Note 3, 4	0.0		0.8	V
$I_{IH,\ LVTTL}$	LVTTL Input HI Current	Note 3, 4			100	µA
$I_{IL,\ LVTTL}$	LVTTL Input LO Current	Note 3, 4	-500			µA
$V_{OH,\ LVTTL}$	LVTTL Output HI Voltage	I_{OH} = 3 mA, Note 4, 6	V_{CC} -1.1			V
$V_{OL,\ LVTTL}$	LVTTL Output LO Voltage	I_{OL} = -1 mA, Note 4	0		0.5	V

Note 1: Power: 0.8 x P_{TYP} < P < 1.2 x P_{TYP}; add to this variations due to power supply voltage. It is noted that the AC power depends on the frequency and load at the outputs (LVTTL).
Note 2: R_{LOAD} = 50 Ω to V_{CC} -2.0 V
Note 3: All LVTTL inputs are provided with an internal pull-up resistor of 16 kΩ ±20 %, room temperature. Thus, the default LVTTL input value is “1” when not connected.
Note 4: Under the condition of typical supply voltage (3.3 V).
Note 5: Standard LVPECL differential voltages may be applied to input SIP, SIN. If single-ended input is used, the minimum required peak to peak voltage is 25 mV.
Note 6: For I_{OH} = 1 mA the minimum HI voltage is increased 100 mV (i.e. V_{CC} -1 V).

AC Characteristics - General

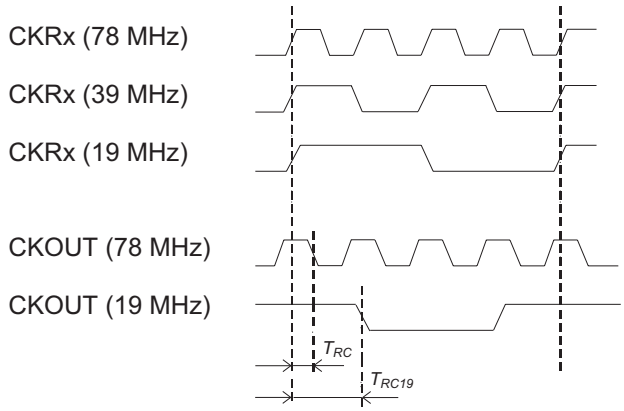
$T_{AMBIENT}$ = -25 °C to +85 °C.

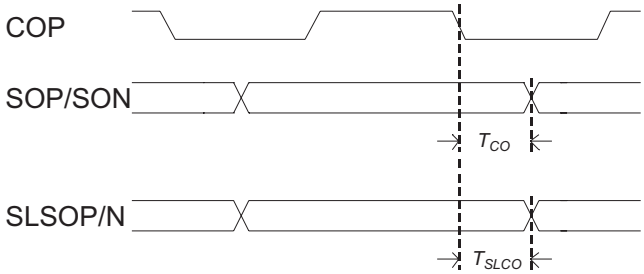
Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
FTR_{SDH}	SDH Tuning Range Relative to Center Frequency	Note 1	98		102	%
FTR_{PDH}	PDH Tuning Range Relative to Center Frequency	Note 1	97		101	%
$T_{R\text{-}LVPECL}$	LVPECL Output Rise Time	Note 2		270	500	ps
$T_{F\text{-}LVPECL}$	LVPECL Output Fall Time	Note 2		200	500	ps
$T_{R\text{-}LVTTL}$	LVTTL Output Rise Time	Note 3		0.8	1	ns
$T_{F\text{-}LVTTL}$	LVTTL Output Fall Time	Note 3		0.8	1	ns
DC_{CKOUT}	Duty Cycle, CKOUT @ 78 MHz	Note 4	40	50	60	%

Note 1: The frequency tuning range may be larger. The minimum/maximum values define the worst case range of the VCO at temperature and power extremes.
Note 2: 20 - 80 %, 50 Ω to V_{CC} -2.0 V.
Note 3: 20 - 80 %, 10 pF. The 20 - 80 % rise and fall times are 2 ns (maximum) with 20 pF load.
Note 4: Measured at V_{TH} = 1.4 V, 10 pF.

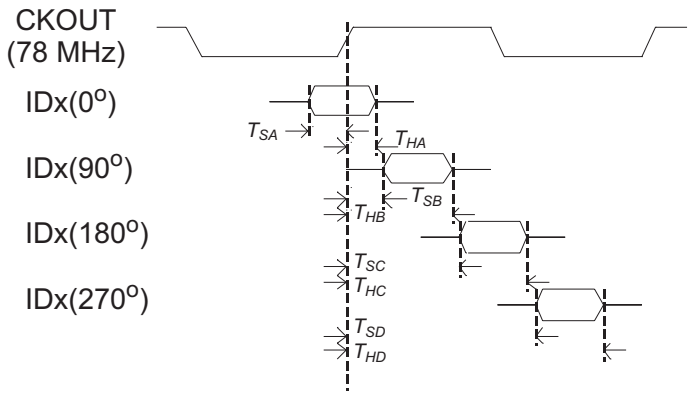
AC Characteristics - GD16591A

$T_{AMBIENT}$ = -25 °C to +85 °C.





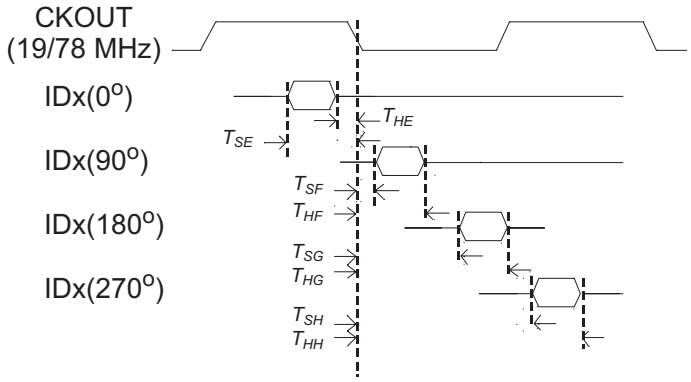
Forward Clocking



Intrinsic VCO Jitter Generation

GD16591A	Frequency Range:	Period [s]	Jitter: [UIp-p]
PDH E4	200 Hz - 3.5 MHz	10	0.05
STM-1 / OC-3 (CMI)	500 Hz - 1.3 MHz	60	0.05
STM-1 / OC-3 (optical)	100 Hz - 1.3 MHz	60	0.1
STM-4 / OC-12	1000 Hz - 5 MHz	60	0.05

Counter Clocking



Maximum Allowed RMS Jitter on Reference Clocks Inputs

Line Rate / Ref. Clk. Frq.	622 Mbit/s	311 Mbit/s	155 Mbit/s
78 MHz	13 ps	26 ps	52 ps
39 MHz	9 ps	18 ps	36 ps
19 MHz	5 ps	10 ps	20 ps
3 dB - PLL BW (Note 1)	12 → 500 kHz	12 → 250 kHz	12 → 125 kHz

Note 1: Measure the RMS jitter on the reference clock within the 3 dB PLL bandwidth used for the actual line rate.

Note 2: Adding the maximum allowed jitter on the reference clock inputs the resulting output jitter will meet the standard recommendations (ITU-T G.751, G.813, G.952, and DE/TM-3017-4).

AC Characteristics - GD16591A - Continued

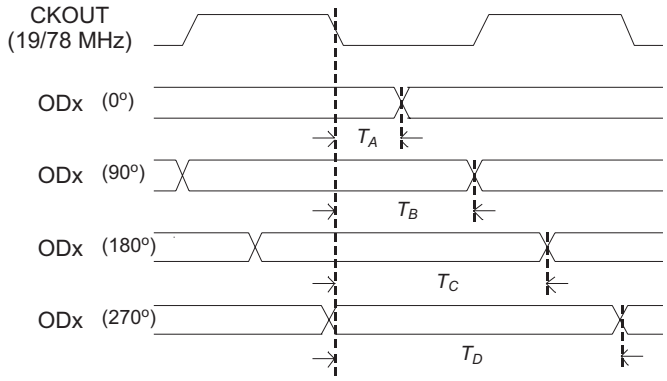
$T_{AMBIENT}$ = -25 °C to +85 °C.

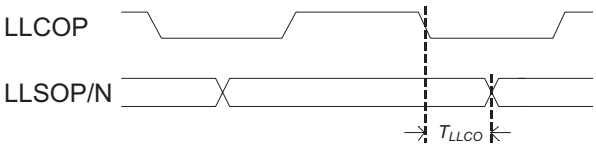
Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
T_{CO}	COP (falling edge) to SOP/SON Valid		100	200	400	ps
T_{SLCO}	COP (falling edge) to SLSOP/N Valid		100	200	400	ps
T_{SLL}	LLSIP/N Set-up Time before LLCIP falling edge		500			ps
T_{HLL}	LLSIP/N Hold Time after LLCIP falling edge		50			ps
T_{SA}	IDx Set-up Time before CKRx rising edge	Note 5	3.5			ns
T_{SB}	IDx Set-up Time after CKRx rising edge	Note 1, 5			T/4 - 3.5	ns
T_{SC}	IDx Set-up Time after CKRx rising edge	Note 1, 5			T/2 - 3.5	ns
T_{SD}	IDx Set-up Time after CKRx rising edge	Note 1, 5			3×T/4 - 3.5	ns
T_{HA}	IDx Hold Time after CKRx rising edge	Note 5	2.5			ns
T_{HB}	IDx Hold Time after CKRx rising edge	Note 1, 5	T/4 + 2.5			ns
T_{HC}	IDx Hold Time after CKRx rising edge	Note 1, 5	T/2 + 2.5			ns
T_{HD}	IDx Hold Time after CKRx rising edge	Note 1, 5	3×T/4+2.5			ns
T_{RC}	Delay from CKRx rising edge to CKOUT falling edge	78 MHz, 5 pF load	2.5	3.5	4.5	ns
T_{RC19}	Delay from CKRx rising edge to CKOUT falling edge	19 MHz, 5 pF load Note 6	12	13	14	ns
$PW_{HI, CKRx}$	High Pulse Width, CKRx Inputs	Note 2	3			ns
T_{SE}	IDx Set-up Time before CKOUT falling edge	Note 3	T_{RC} + 3.5			ns
T_{SF}	IDx Set-up Time after CKOUT falling edge	Note 1, 3			T/4-T_{RC}-3.5	ns
T_{SG}	IDx Set-up Time after CKOUT falling edge	Note 1, 3			T/2-T_{RC}-3.5	ns
T_{SH}	IDx Set-up Time after CKOUT falling edge	Note 1, 3			3×T/4-T_{RC}-3.5	ns
T_{HE}	IDx Hold Time before CKOUT falling edge	Note 3	T_{RC}-2.5			ns
T_{HD}	IDx Hold Time after CKOUT falling edge	Note 1, 3	T/4-T_{RC}+2.5			ns
T_{HF}	IDx Hold Time after CKOUT falling edge	Note 1, 3	T/2-T_{RC}+2.5			ns
T_{HG}	IDx Hold Time after CKOUT falling edge	Note 1, 3	3×T/4-T_{RC}+2.5			ns
JT	Jitter Transfer	Note 4		0.0	0.1	dB

Note 1: T equals the period time for CKOUT, which is the bit period for the parallel data; i.e. 12.9 ns for 78 Mbit/s or 51.4 ns for 19 Mbit/s.
Note 2: Measured at V_{TH} = 1.4 V. It is the rising edge, which is used for the timing and frequency comparison. The 20% - 80% rise time should be less than 1 ns to minimise jitter at the reference clock inputs.
Note 3: Set-up and Hold times with respect to the delay T_{RC}.
Note 4: PLL 3 dB bandwidth 12 kHz to N × 125 kHz for STM-N. Peaking and bandwidth depends on actual loop filter values.
Note 5: Valid for 78 MHz forward clocking. For 19 MHz forward clocking the setup and hold windows are delayed 9.6 ns.
Note 6: T_{RC19} is actually T_{RC} + 9.6 ns.

AC Characteristics - GD16592A

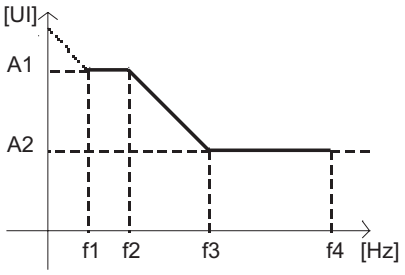
$T_{AMBIENT}$ = -25 °C to +85 °C.





Jitter Tolerance

GD16592A	f1 [Hz]	f2 [Hz]	f3 [Hz]	f4 [Hz]	A1 [UI_{p-p}]	A2 [UI_{p-p}]
PDH E4	200	500	10k	3.5M	2	0.15
STM-1 / OC-3 (CMI)	500	3.25k	65k	1.3M	2	0.15
STM-1 / OC-03 (optical)	500	6.5k	65k	1.3M	2	0.2
STM-4 / OC-12	300	25k	250k	2.5M	2	0.2

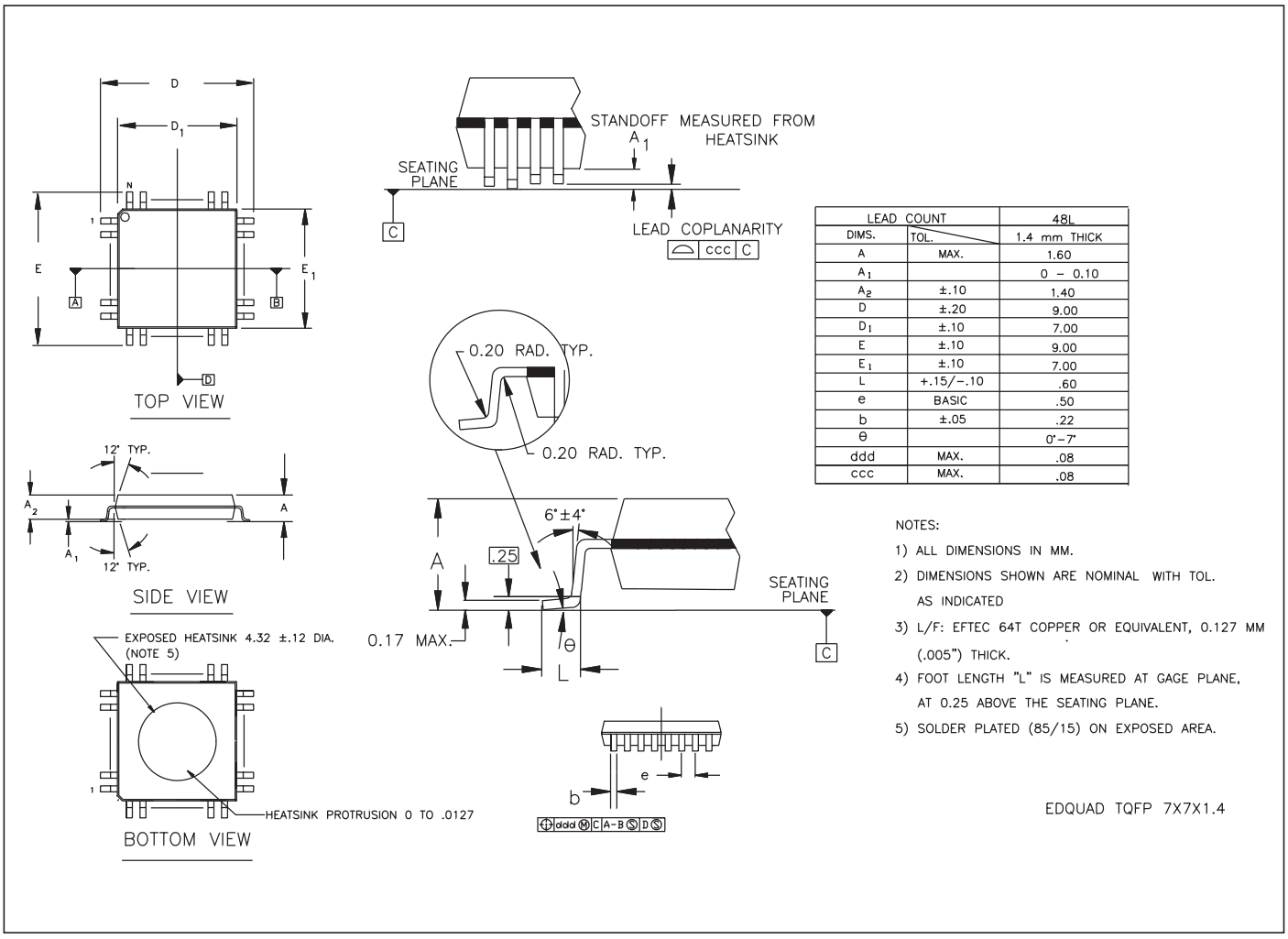


Note: The stated jitter tolerance of GD16592A exceeds the standard recommendations (ITU-T G.823, G.825, and DE/TM-03067).

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
T_{LLCO}	LLCOP to LLSOP/N Valid		100	200	400	ps
T_A	CKOUT to ODx Valid	Note 3	0		1	ns
T_B	CKOUT to ODx Valid	Note 1, 3	T/4		T/4+1	ns
T_C	CKOUT to ODx Valid	Note 1, 3	T/2		T/2+1	ns
T_D	CKOUT to ODx Valid	Note 1, 3	3×T/4		3×T/4+1	ns
$T_{ACQUISITION}$	Acquisition Time	Transition density = 0.5		25		µs
CID	Consecutive Indentical Digits	# bits without transition		250		
D_{CKRF}	CKRF Frequency Deviation from Nominal Line Frequency			±200		ppm
JT	Jitter Transfer	Note 2		0.0	0.1	dB

Note 1: T equals the period time for CKOUT, which is the bit period for the parallel data; i.e. 12.9 ns for 78 Mbit/s or 51.4 ns for 19 Mbit/s.
Note 2: PLL 3 dB bandwidth 12 kHz to 500 kHz; N × 125 kHz for STM-N. Peaking and bandwidth depends on actual loop filter values.
Note 3: 10 pF load at CKOUT and ODx outputs.

Package Outline



LEAD COUNT		48L
DIMS.	TOL.	1.4 mm THICK
A	MAX.	1.60
A_1		0 – 0.10
A_2	±.10	1.40
D	±.20	9.00
D_1	±.10	7.00
E	±.10	9.00
E_1	±.10	7.00
L	+.15/−.10	.60
e	BASIC	.50
b	±.05	.22
θ		0°–7°
ddd	MAX.	.08
ccc	MAX.	.08

Figure 11.*Package 48 pin EDQUAD TQFP™ (7 x 7 x 1.4 mm).*

External References

GD90591/592	: Data sheet for the evaluation board for the GD16591A/GD16592A chip set.
ITU-T G.751 (11/88)	: Digital multiplex equipments operating at the third order bit rate of 34368 kbit/s.
ITU-T G.813 (8/96)	: Timing characteristics of SDH equipment slave clocks.
ITU-T G.823 (3/93)	: The control of jitter and wander within digital networks based on the 2048 kbit/s hierarchy.
ITU-T G.825 (3/93)	: The control of jitter and wander within digital networks based on SDH.
ITU-T G. 958 (11/94)	: Digital line system based on the SDH for use on optical fibre channels.
DE/TM-3017-4 (Draft)	: Transmission and multiplexing; generic requirements for synchronisation networks.
DE/TM-03067 (Draft)	: Transmission and multiplexing; the control of jitter and wander in transport networks.
MIL Std. 883 (3/89)	: Method 3015, Human Body Model.
JEDEC JESD51 (12/95)	: Methology for the Thermal Measurement of Component Packages (Single Semiconductor Device)
JEDEC JESD51.3 (8/96)	: Low effective Thermal Conductivity Test Boards for Leaded Surface Mount Packages.

Device Marking

Figure 12.*Device Marking - GD16591A. Top View.*

Figure 13.*Device Marking - GD16592A. Top View.*

Ordering Information

To order, please specify as shown below:

Product Name:	Type:	Package Type:	Ambient Temperature Range:
GD16591A-48BA	Transmitter	EDQUAD TQFP™, 48 pin	-25...85°C
GD16592A-48BA	Receiver	EDQUAD TQFP™, 48 pin	-25...85°C

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Web site : http://www.giga.dk

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Distributor: