GD4052B

DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION – The 4052B is a Dual 4-Channel Analog Multiplexer/Demultiplexer with common channel select logic. Each Multiplexer/Demultiplexer has four independent inputs/outputs (Y_0–Y_3) and a Common Input/Output (Z). The common channel select logic includes two Address inputs (A_0, A_1) and an active LOW Enable Input ($\overline{E}$).

Both multiplexer/demultiplexers contain four bidirectional analog switches, each with one side connected to an independent Input/Output (Y_0–Y_3) and the other side connected to a Common Input/Output (Z). With the Enable Input LOW, one of the four switches is selected (low impedance, ON state) by the two Address Inputs. With the Enable Input HIGH, all switches are in the high impedance OFF state, independent of the Address Inputs.

V_{DD} and V_{SS} are the two supply voltage connections for the digital control inputs (A_0, A_1, $\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog inputs/outputs (Y_0–Y_3, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}–V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- **DIGITAL OR ANALOG MULTIPLEXER/DEMULTIPLEXER**
- **COMMON ENABLE INPUT (ACTIVE LOW)**

PIN NAMES

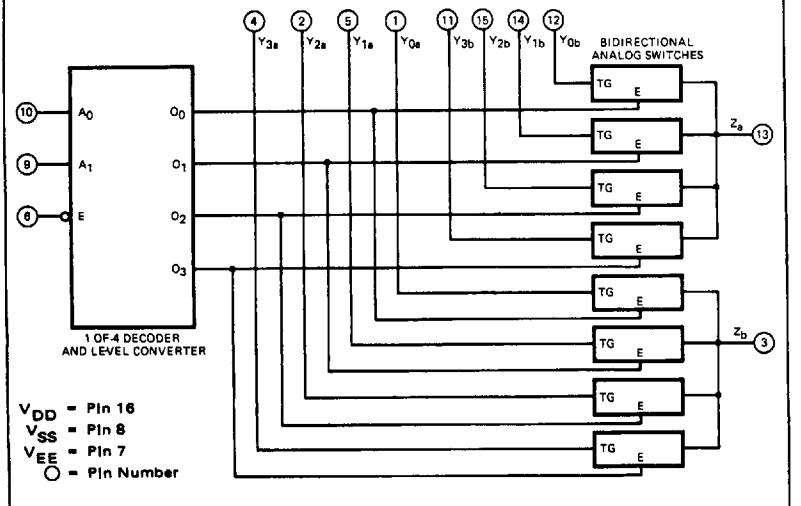
Y_{0a}–Y_{3a}	Independent Inputs/Outputs
Y_{0b}–Y_{3b}	Independent Inputs/Outputs
A_0, A_1	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
Z_a, Z_b	Common Input/Output

TRUTH TABLE

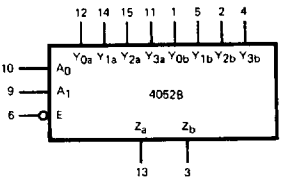
INPUTS			CHANNELS			
$\overline{E}$	A_1	A_0	Y_0–Z	Y_1–Z	Y_2–Z	Y_3–Z
L	L	L	ON	OFF	OFF	OFF
L	L	H	OFF	ON	OFF	OFF
L	H	L	OFF	OFF	ON	OFF
L	H	H	OFF	OFF	OFF	ON
H	X	X	OFF	OFF	OFF	OFF

L = LOW Level, H = HIGH Level, X = Don't care

4052B FUNCTIONAL LOGIC DIAGRAM

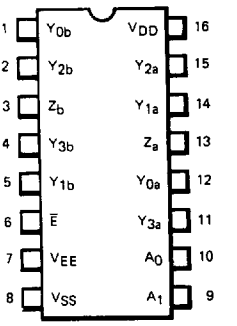


LOGIC SYMBOL



V_{DD} = PIN 16
V_{SS} = PIN 8
V_{EE} = PIN 7

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

DC CHARACTERISTICS: V_{DD} as shown, V_{EE} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R_{ON}	ON Resistance	XC		95	900		55	380		35	210	Ω	MIN	V_{IS} = V_{DD} to V_{EE} Note 2
				100	1000		65	500		40	280		25°C	
				125	1100		100	600		65	340		MAX	
		XM		90	850		50	340		30	190	Ω	MIN	
				100	1000		65	500		40	280		25°C	
				150	1150		110	660		70	370		MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels			25			10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				nA	25°C	$\overline{E}$ = V_{DD}, V_{SS} = $V_{DD}/2$ V_{IS} = V_{DD} or V_{EE} V_{OS} = V_{EE} or V_{DD}
		XM						80						
	Any Channel OFF	XC						100						$\overline{E}$ = V_{SS} = $V_{DD}/2$ V_{IS} = V_{DD} or V_{EE} V_{OS} = V_{EE} or V_{DD}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40			80	μA	MIN, 25°C	V_{SS} = V_{EE} All inputs at V_{DD} or V_{EE}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

Notes on following page

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{EE} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		25			10			6		ns	C_L = 50 pF, R_L = 200 kΩ
t_{PHL}	Input to Output		10			6			4			$\overline{E}$ = V_{SS} = V_{EE},
t_{PLH}	Propagation Delay,		170			95			80		ns	A_n or V_{is} = V_{DD} or V_{EE}
t_{PHL}	Address to Output		210			125			95			Note 5
t_{PZL}	Output Enable Time		185			95			75		ns	C_L = 50 pF, R_L = 1 kΩ
t_{PZH}			205			105			85			$\overline{E}$ or A_n = V_{SS} = V_{EE}
t_{PLZ}	Output Disable Time		1250			1130			1080		ns	V_{is} = V_{DD} or V_{EE}
t_{PHZ}			1240			1120			1070			Note 5
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	R_L = 10 kΩ V_{SS} = V_{DD}/2, $\overline{E}$ = V_{EE}, V_{is} = V_{DD}/2 (sine wave) p-p f_{is} = 1 kHz
	Crosstalk Between Any Two Channels										MHz	R_L = 1 kΩ, $\overline{E}$ = V_{EE} V_{is} = V_{DD}/2 (sine wave) p-p at -40 dB V_{SS} = V_{DD}/2, 20 Log_{10} (V_{os}/V_{is}) = -40 dB
	OFF State Feedthrough					1					MHz	R_L = 1 kΩ, V_{SS} = V_{DD}/2 $\overline{E}$ = V_{DD} V_{is} = V_{DD}/2 (sine wave) p-p 20 Log_{10} (V_{os}/V_{is}) = -40 dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	R_L = 1 kΩ, $\overline{E}$ = V_{SS} V_{is} = V_{DD}/2 (sine wave) p-p V_{SS} = V_{DD}/2 20 Log_{10} (V_{os}/V_{os} @ 1 kHz = -3 dB

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. $\overline{E}$ = V_{SS}, R_L = 10 kΩ, any channel selected and V_{SS} = V_{EE} or V_{DD}/2.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. V_{is}/V_{os} is the voltage signal at an Input/Output terminal (Y_n/Z_n).
5. V_{IN} = V_{DD} (Square Wave), Input transition times ≤ 20 ns
6. In certain applications, the current through the external load resistor (R_L) may include both V_{DD} and signal line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 2, 4, 5, 11, 12, 14, or 15 the voltage drop across the bidirectional switch must not exceed 0.5 V at T_A ≤ 25°C, or 0.3 V at T_A > 25°C. No V_{DD} current will flow through R_L if the switch current flows into terminals 3 or 13.