

GD54/74HC273, GD54/74HCT273

OCTAL D-TYPE FLIP-FLOPS WITH COMMON CLOCK & CLEAR

General Description

These devices are identical in pinout to the 54/74LS273. They consist of eight master/slave D-type flip-flops with a common Clock and common Clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the rising edge of the Clock input. The Clear input when low, sets all outputs to a low state. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts for HCT 4.5 to 5.5 volts
- Low input current. 1 μ A Max.
- Low quiescent current: 80 μ A Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS			OUTPUTS
	$\overline{\text{CLR}}$	CLK	D_n	Q_n
reset (clear)	L	X	X	L
load "1"	H	$\uparrow$	h	H
load "0"	H	$\uparrow$	l	L

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
 $\uparrow$ = LOW-to-HIGH transition
X = don't care

Logic Diagram

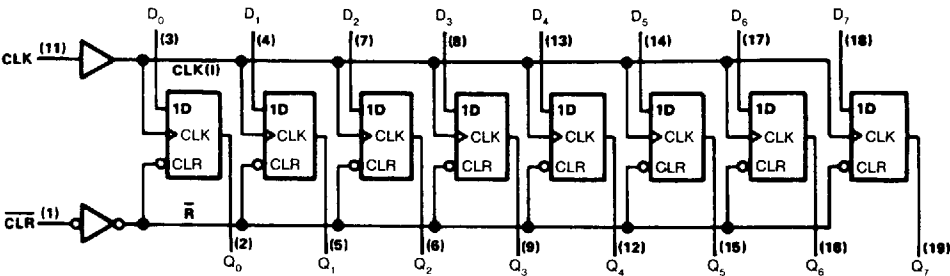
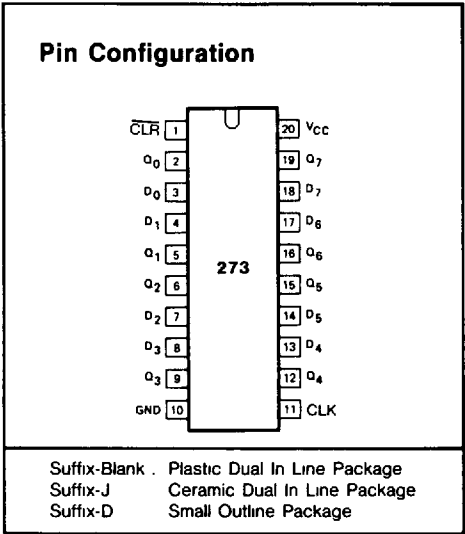


Fig. 1 Logic diagram



Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC Supply voltage		-0.5	+7	V
I_{IK}, I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC} + 0.5V$		20	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC} + 0.5V$		25	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		-65	150	°C
P_D	Power dissipation per package	above +70°C derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance $1/16 \pm 1/32$ in from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN	MAX	
Supply-Voltage Range V_{CC} : GD54/74HC Types GD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A : GD74 Types GD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall times t_r, t_f : GD54/74HC Types at 2V at 4.5V at 6V GD54/74HCT Types at 4.5V		1000 500 400 500	ns

Logic Diagram

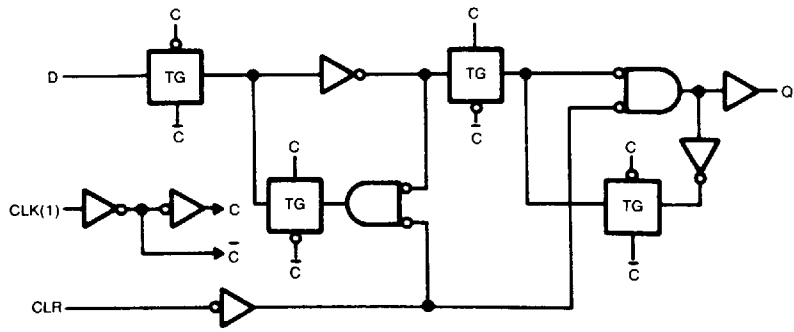


Fig. 2 Logic diagram (one gate)

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HC273		GD54HC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{IH}	HIGH level input Voltage		2 0 4 5 6 0	1 5 3 15 4 2			1 5 3 15 4 2		1 5 3 15 4 2		V
V _{IL}	LOW level input voltage		2 0 4 5 6 0			0 3 0 9 1 2		0 3 0 9 1 2		0 3 0 9 1 2	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	2 0 4 5 6 0	1 9 4 4 5 9	2 0 4 5 6 0	1 9 4 4 5 9		1 9 4 4 5 9		V
		or V _{IL}	I _{OH} =-4mA I _{OH} =-5 2mA	4 5 6 0	3 98 5 48	4 3 5 2	3 84 5 34		3 7 5 2		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	2 0 4 5 6 0			0 1 0 1 0 1	0 1 0 1 0 1		0 1 0 1 0 1	V
		or V _{IL}	I _{OL} =4mA I _{OL} =5 2mA	4 5 6 0	0 17 0 15	0 26 0 26		0 33 0 33		0 4 0 4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	6 0			0 1		1 0		1 0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	6 0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION	V _{CC} (V)	T _A =25°C			GD74HCT273		GD54HCT273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{IH}	HIGH level input Voltage		4 5 to 5 5	2 0			2 0		2 0		V
V _{IL}	LOW level input voltage		4 5 to 5 5			0 8		0 8		0 8	V
V _{OH}	HIGH level output voltage	V _{IN} =V _{IH}	I _{OH} =-20μA	4 5	4 4	4 5	4 4		4 4		V
		or V _{IL}	I _{OH} =-4mA	4 5	3 98	4 3	3 84		3 7		
V _{OL}	LOW level output voltage	V _{IN} =V _{IH}	I _{OL} =20μA	4 5			0 1	0 1		0 1	V
		or V _{IL}	I _{OL} =4mA	4 5		0 17	0 26	0 33		0 4	
I _{IN}	Input leakage Current	V _{IN} =V _{CC} or GND	5 5			0 1		1 0		1 0	μA
I _{CC}	Quiescent Supply Current	V _{IN} =V _{CC} or GND I _{out} =0μA	5 5			8		80		160	μA

GD54/74HC273, GD54/74HCT273

Timing Requirements for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC}	$T_A=25^\circ\text{C}$			GD74HC273		GD54HC273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	$\overline{\text{CLR}}$ (low)	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
		CLK (high or low)	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{su}	Set up time	Data before CLK $\uparrow$	2.0	60	30		80		100		ns
			4.5	15	10		18		20		
			6.0	14	8		16		18		
t_{rec}	Recovery time	$\overline{\text{CLR}}$ inactive	2.0	5	0		5		5		ns
			4.5	5	0		5		5		
			6.0	5	0		5		5		
t_h	Hold time	data after CLK $\uparrow$	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC}	$T_A=25^\circ\text{C}$			GD74HC273		GD54HC273		UNIT
				MIN.	TYP	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Pulse frequency Maximum clock		2.0	6	20		5		4		MHz
			4.5	30	65		25		20		
			6.0	35	75		30		25		
t_{PLH} / t_{PHL}	Propagation Delay Time CLK to Q_n		2.0		46	160		200		240	ns
			4.5		15	30		40		50	
			6.0		14	28		35		45	
t_{PLH} / t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q_n		2.0		45	155		190		230	ns
			4.5		15	28		38		45	
			6.0		14	26		34		40	
t_{TLH} / t_{THL}	Output Transition Time		2.0		25	70		85		100	ns
			4.5		8	15		18		22	
			6.0		7	13		16		18	

GD54/74HC273, GD54/74HCT273

Timing Requirements for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER		V_{CC}	$T_A=25^\circ\text{C}$			GD74HCT273		GD54HCT273		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_w	pulse duration	$\overline{\text{CLR}}$ (low)	4 5	18	10		20		25		ns
		CLK (high or low)	4 5	17	10		20		25		ns
t_{su}	Set up time	Data before CLK $\uparrow$	4 5	15	10		18		20		ns
t_{rec}	Recovery time	CLR inactive	4 5	5	0		5		5		ns
t_h	Hold time/d time,	data after CLK $\uparrow$	4 5	3	0		3		3		ns

AC Characteristics for HCT: $t_r=t_f=6\text{ns}$ $C_L=50\text{ pF}$

SYMBOL	PARAMETER	V_{CC}	$T_A=25^\circ\text{C}$			GD74HCT273		GD54HCT273		UNIT
			MIN.	TYP	MAX	MIN	MAX	MIN.	MAX	
f_{max}	Pulse frequency Maximum clock	4 5	27	54		22		18		MHz
t_{PLH} / t_{PHL}	Propagation Delay Time CLK to Q_n	4 5		16	30		40		50	ns
t_{PLH} / t_{PHL}	Propagation Delay Time $\overline{\text{CLR}}$ to Q_n	4 5		17	30		40		50	ns
t_{TLH} / t_{THL}	Output Transition Time	4 5		8	15		18		22	ns

AC Waveforms

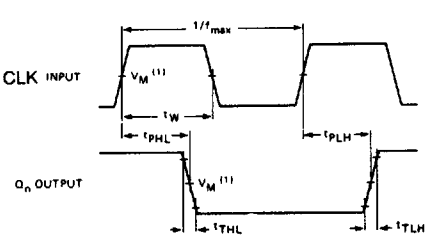


Fig. 3 Waveforms showing the clock (CLK) to output (Qn) propagation delays, the clock pulse width output transition times and the maximum clock pulse frequency.

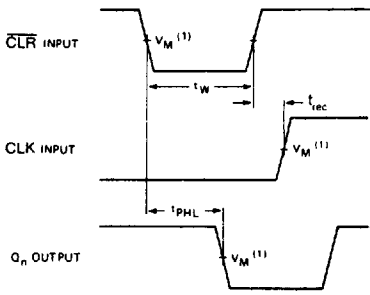


Fig. 4 Waveforms showing the master clear (CLR) pulse width, the master clear to output (Qn) propagation delays and the master clear to clock (CLK) recovery time.

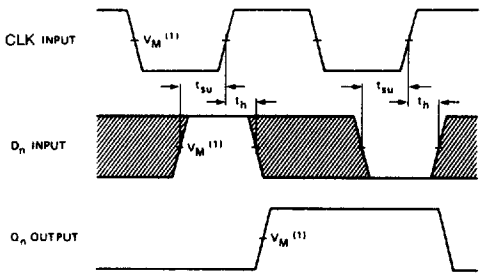


Fig. 5 Waveforms showing the data set-up and hold times for the data input (Dn).

Note to Fig. 5
The staded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms
(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$
HCT $V_M = 1.3V$, $V_I = \text{GND to } 3V$