GENERAL SEMICONDUCTOR®

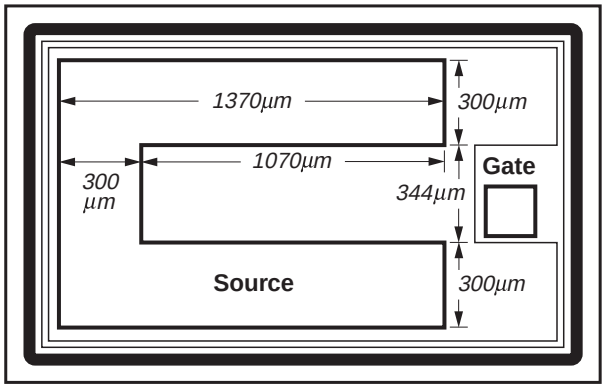
GF6968ED

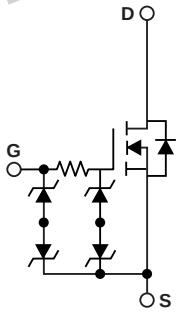
Battery Switch, ESD Protected N-Channel Enhancement-Mode MOSFET Die

V_{DS} 20V $R_{DS(ON)}$ 20mΩ I_D 6.8A

TRENCH GENFET™ New Product

Chip Geometry





Physical Characteristics

- Die size : 2000 x 1200µm (78.8 x 47.2 mils)
- Metalization:
  Top: Al/Si/Cu
  Back: Ti/Ni/Ag
- Metal Thickness:
  Top: 3.0µm
  Back: 1.4µm
- Die thickness: 9 –13 mils
- Bonding Area:
  Source: As shown
  Gate: 175 x 175µm
- Recommended Wire Bonding:
  Source: 2 mil ∅ Au wire (5 or more wires preferred)
  Gate: 2 mil ∅ Au wire

Note: More source wires can further improve performance

Features

- Advanced Trench process technology
- High density cell design for ultra-low on-resistance
- ESD protected
- Logic level
- Ideal for Li ion battery pack applications

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current(1)		I_D	6.8	A
Pulsed Drain Current		I_{DM}	30	
Maximum Power Dissipation(1)	T_A = 25°C T_A = 70°C	P_D	1.5 0.96	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Junction-to-Ambient Thermal Resistance(1)		$R_{\theta JA}$	83	°C/W

Note: (1) Maximum ratings are based on die packaged in a TSSOP-8 Dual Common Drain package. Actual rating can increase (or decrease), depending on actual assembly method used

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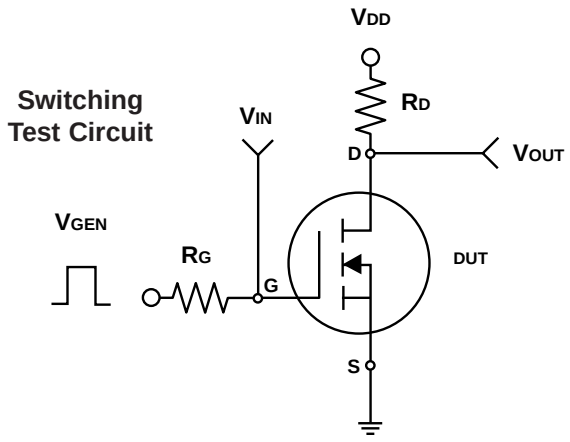
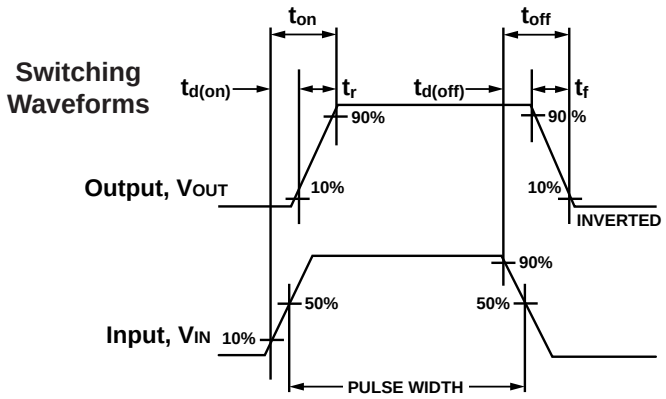
Electrical Characteristics (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	20	–	–	V
Drain-Source On-State Resistance(1)	$R_{DS(on)}$	V_{GS} = 3.5V, I_D = 3.0A	–	15	20	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1mA	0.5	0.85	1.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V	–	–	10	μA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±12V, V_{DS} = 0V	–	–	10	μA
On-State Drain Current(1)	$I_{D(on)}$	V_{DS} ≥ 5V, V_{GS} = 4.5V	20	–	–	A
Forward Transconductance(1)	g_{fs}	V_{DS} = 10V, I_D = 6.8A	–	20	–	S
Dynamic						
Total Gate Charge	Q_g	V_{DS} = 10V, V_{GS} = 4.5V I_D = 6.8A	–	16	30	nC
Gate-Source Charge	Q_{gs}		–	2		
Gate-Drain Charge	Q_{gd}		–	3.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10V, R_L = 10Ω I_D ≈ 1A, V_{GEN} = 4.5V R_G = 6Ω	–	450	600	ns
Turn-On Rise Time	t_r		–	650	850	
Turn-Off Delay Time	$t_{d(off)}$		–	4.5	6.0	μs
Turn-Off Fall Time	t_f		–	1.7	2.2	
Input Capacitance(2)	C_{iss}	V_{GS} = 0V V_{DS} = 10V f = 1.0MHz		1360		pF
Output Capacitance(2)	C_{oss}			220		
Reverse Transfer Capacitance(2)	C_{rss}			130		
Source-Drain Diode						
Max. Diode Forward Current	I_S				1.5	A
Diode Forward Voltage	V_{SD}	I_S = 1.5A, V_{GS} = 0V	–	–	1.2	V

Note: (1) Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%
(2) For MOSFET portion only





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Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 1 – Output Characteristics

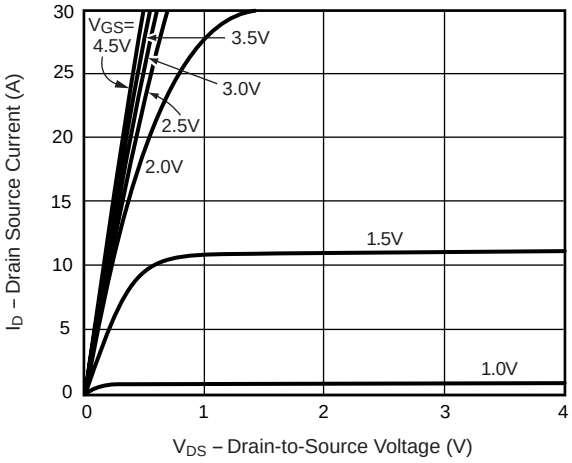

Fig. 2 – Transfer Characteristics

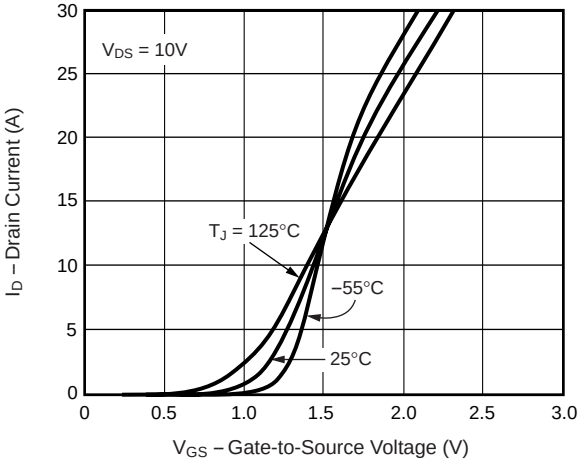

Fig. 3 – Threshold Voltage vs. Temperature

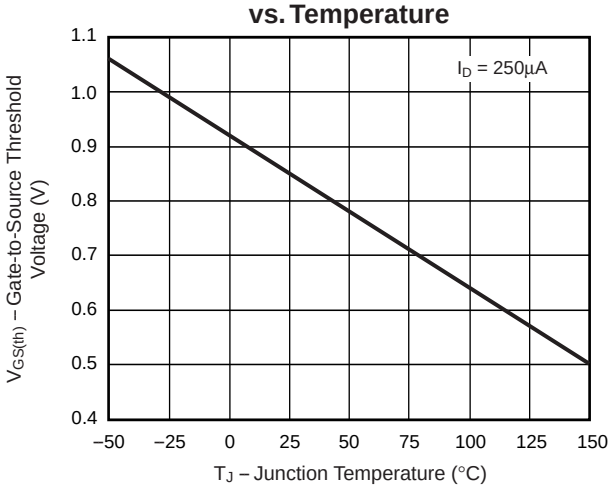

Fig. 4 – On-Resistance vs. Drain Current

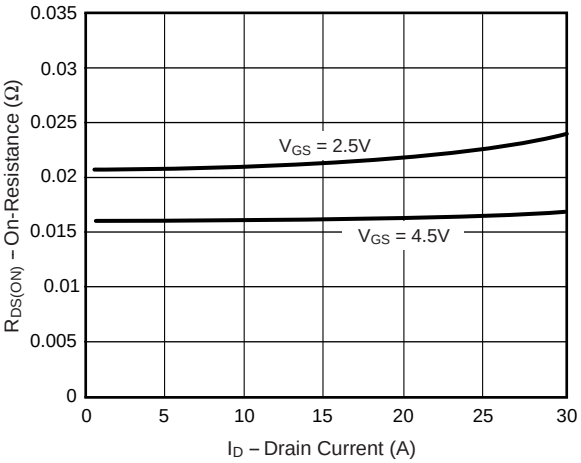

Fig. 5 – On-Resistance vs. Junction Temperature

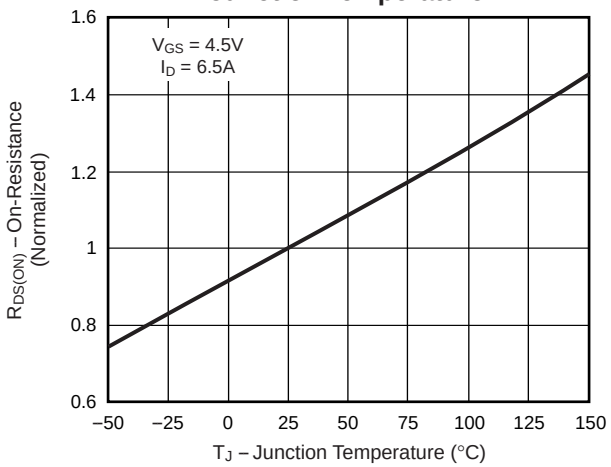

Fig. 6 – On-Resistance vs. Gate-to-Source Voltage

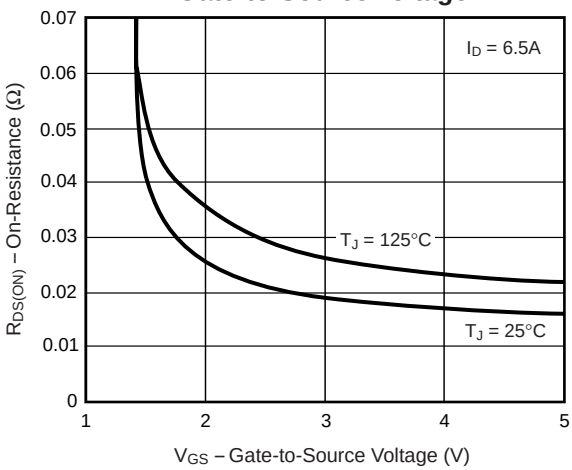

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Fig. 7 – Gate Charge

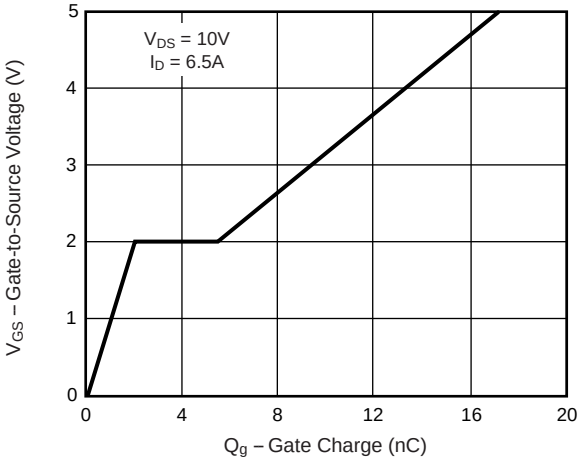

Fig. 8 – Source-Drain Diode Forward Voltage

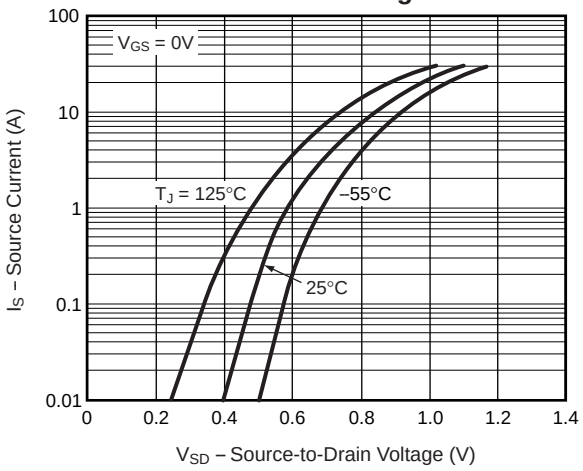

Fig. 9 – Power vs. Pulse Duration

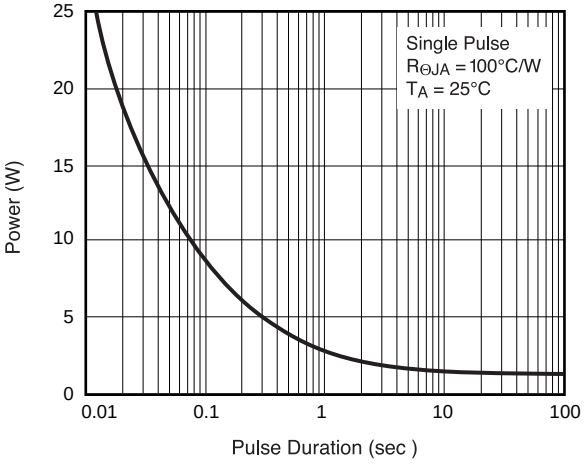

Fig. 10 – Maximum Safe Operating Area