Oki Semiconductor

GHDD4414

Decision Circuit with Phase Detectors

GENERAL DESCRIPTION

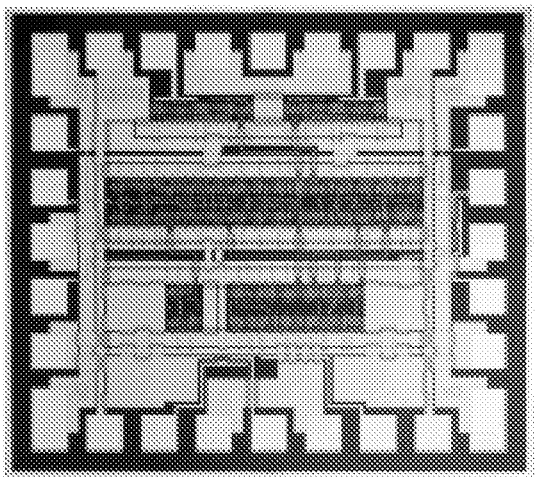
Oki's GHDD4414 is a 10-GHz decision circuit designed to strip data from high-speed serial bit streams in 10-Gbps communication links. Using a clock input at up to 10 GHz and using D-flip-flops, EX-ORs, and phase detectors, this circuit separates a 10-Gbps data stream into: clock output, data output, "phase" variation output, and data density output.

A 10-GHz master clock drives two D-flip-flops in this circuit. Buffered input data is clocked through the first flip-flop, then the second, "data out" is taken from the first flip-flop. The data input buffer is composed of a series of inverters to delay the signal and obtain a small decision ambiguity. A phase comparison is made of the buffered data and data from flip-flop one; a second phase comparison is made of the output of flip-flops one and two. The phase detectors are modified EX-OR circuits with resistor summing of the logic gates to permit analog measurement of their outputs. Any change in the timing relationships between the clock and data is seen at the output of the first phase detector. The second flip-flop operates as a 1-bit shift register with fixed 360-deg phase shift. The second phase detector output depends only upon the transition density (speed of rise and fall transitions) of the input data signal.

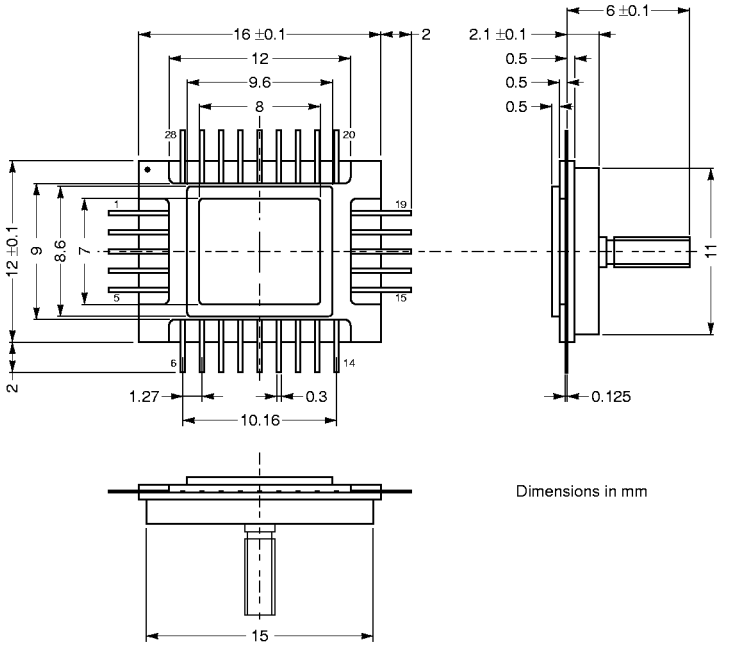
All signal interfaces are 50-Ω with all inputs internally terminated in 50 Ω. The 10-GHz clock and data inputs are AC capacitively-coupled for ease of interfacing at microwave speeds and reducing ground noise induced phase jitter. Data and phase outputs are DC-coupled.

FEATURES

- Phase detectors on chip: verifies data integrity
- Isolated 10-Gbps input pins: minimizes noise and impedance variation
- 1.5 V, 1 W: lowest power with 50-Ω interfaces
- 28-pin ceramic flat package with impedance controlling ground plane and flush mount heat sink



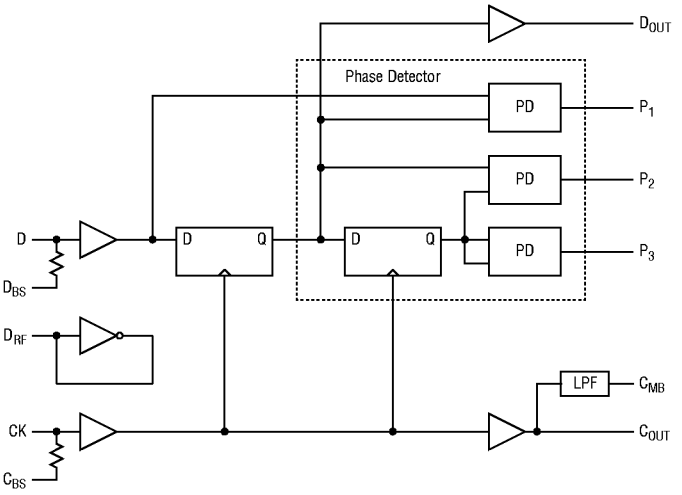
PIN CONFIGURATION



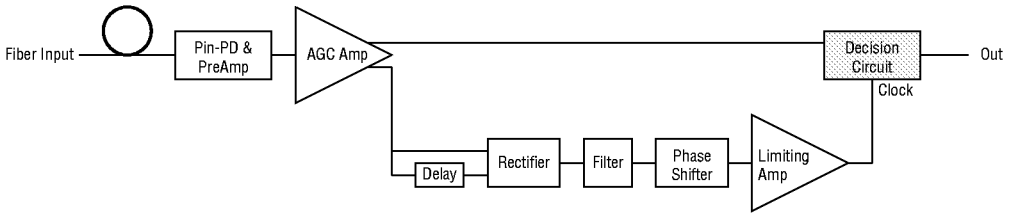
Dimensions in mm

Pin	Signal	Function	Pin	Signal	Function
1	C_{BS}	Clock bias input	15	V_B	Power supply (buffer)
2	NC		16	P1	Phase detector output
3	C_{MB}	Clock output duty monitor	17	P2	Phase detector ref. output 1
4	NC		18	P3	Phase detector ref. output 2
5	V_B	Powr supply (buffer)	19	V_D	Power supply (logic circuit)
6	GND		20	GND	
7	D_{OUT}	Data output	21	D_{IN}	Data input
8	GND		22	GND	
9	NC		23	D_{BS}	Data bias input
10	NC		24	D_{RF}	Data bias reference output
11	NC		25	V_D	Power supply (logic circuit)
12	GND		26	GND	
13	C_{OUT}	Clock output	27	CK	Clock input
14	GND		28	GND	

BLOCK DIAGRAM



APPLICATION BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

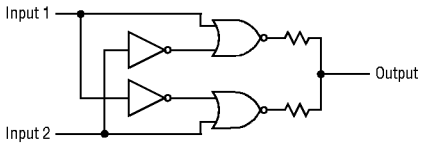
V_{DD} = 1.5 V ±0.1 V, V_B = 1.5 V ±0.1 V, T_S = 0° to 70°C

Parameter	Symbol	Condition	Min.	Max.	Unit
Power dissipation	P			1	W
Decision ambiguity	V_{IDEC}	10 Gbps PRBS: 2^{15} -1		0.05	V_{P-P}
Phase margin	$\Delta\theta$		250		degree
Data input voltage amplitude	V_{ID}	Capacitive coupling		0.8	V_{P-P}
Clock input voltage amplitude	V_{IC}		0.4	0.8	V_{P-P}
Data output voltage amplitude	V_{OD}	50Ω load capacitive coupling	0.7		V_{P-P}
Clock output voltage amplitude	V_{OC}		0.7		V_{P-P}
Clock output duty cycle	D_{TYC}		40	60	%
Clock to data delay	τ_{CD}		25	45	ps
Phase detection sensitivity	$\Delta V\theta$	10 Gbps PRBS: 2^{15} -1	0.28		mV/degree

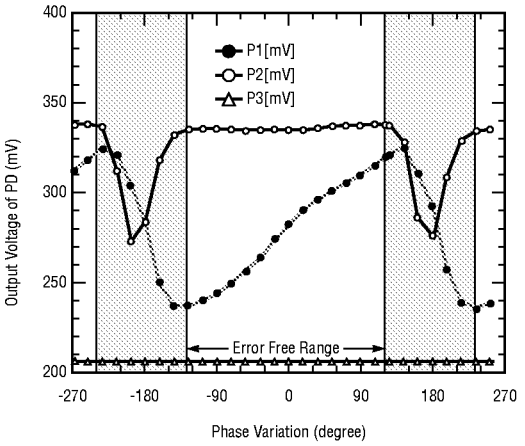
Phase Detection Characteristics (D_{IN} Amplitude = 0.7-V_{P-P})

CIN Delay (ps)	P1 (V)	P2 (V)	P3 (V)	Comments
+29	0.350	0.343	0.443	Maximum delay for ER <10^{-10}
0	0.383	0.340	0.443	Center of phase margin
-29	0.424	0.342	0.443	Minimum delay for ER <10^{-10}

PHASE DETECTOR CIRCUIT



PHASE DETECTION BETWEEN SIGNAL AND CLOCK AT 10 Gbps



TIMING