



FEATURES

- 100 μ A typical current drain
- low noise and distortion
- 1.0 to 5 VDC operating range
- DC coupled stages
- Class A output stage
- Schottky diodes for MPO control
- variable transducer current
- 4 k Ω microphone decoupling resistor

STANDARD PACKAGING

- 8 pin MICROpac
- 8 pin PLID[®]
- 8 pin SLT
- Chip (61 x 55 mils)

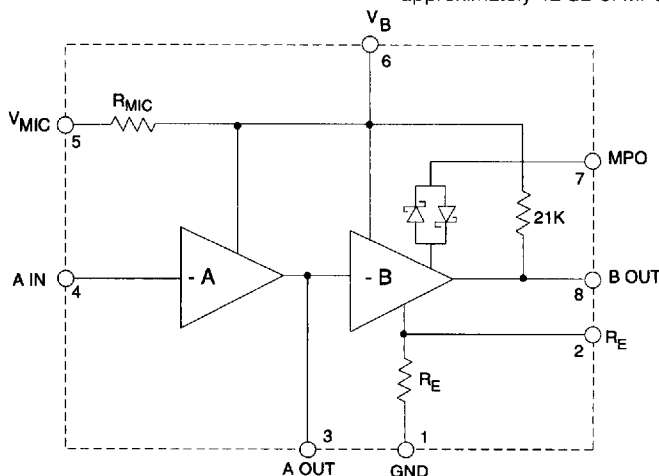
DESCRIPTION

The GK509 is a Class A amplifier utilizing Gennum's proprietary low voltage JFET technology. It consists of a single-ended, low noise inverting gain block, a Class A output stage, an on-chip microphone decoupling resistor, and a pair of Schottky diodes for symmetrical peak clipping.

Block A typically has an open loop voltage gain of 56 dB, with the closed loop gain set by the ratio of the feedback resistor to the source impedance. It is recommended that the maximum closed loop gain be 20 dB lower than the open loop gain. All blocks of the device are internally bias compensated, preventing any DC current flow via external feedback resistors. Without this compensation audible scratchiness would be present during changes in volume control settings.

The output stage of the GK509 is a Class A current drive. It has a fixed reference voltage of typically 30 mV at pin 2 of the device. The current that flows in the transducer is the ratio of the 30 mV reference voltage and the on-chip emitter resistor (R_E). To increase the bias current in the transducer, simply place an external R_E resistor from pin 2 to ground, thereby decreasing the equivalent emitter resistance and increasing the current.

The GK509 also contains a pair of Schottky diodes in the feedback configuration of the output stage, which provides approximately 12 dB of MPO control.



All resistors in ohms, all capacitors in farads unless otherwise stated

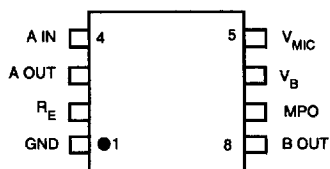
BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

PIN CONNECTION

PARAMETER	VALUE/UNITS
Supply Voltage	5 V DC
Operating Temperature Range	-10°C to 40°C
Storage Temperature Range	-20°C to 70°C

CAUTION
CLASS 1 ESD SENSITIVITY



ELECTRICAL CHARACTERISTICS

V_p - Pin voltage measured with conditions as shown in Test Circuit.

Positive current corresponds to current INTO the pin.

Negative current corresponds with current OUT of the pin.

Conditions: Frequency = 1 kHz, Temperature = 25°C, Supply Voltage $V_B = 1.3$ V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Amplifier Current	I_{AMP}		55	100	145	μA
Transducer Current	I_{TRANS}		170	230	290	μA
Maximum Transducer Current	$I_{TRANS (MAX)}$	$V_{P2} = 0$ V	2	-	-	mA
A Input Bias Voltage (pin 4)	$V_{BIAS A}$		500	570	650	mV
A Input Bias Current (pin 4)	$I_{BIAS A}$	$R_{FA} = 1$ M Ω , (Note 1)	-50	0	50	nA
A O/P Voltage Swing-Hi (pin 3)	$V_{OH A}$	$V_{IN} = 0.4$ V DC, $R_{FA} = \infty$, $I_{P3} = -10$ μA (Note 2)	200	580	-	mV
A Output Swing-Lo (pin 3)	$V_{OL A}$	$I_{IN} = +1$ μA , $R_{FA} = \infty$, $I_{P3} = +10$ μA (Note 3)	200	280	-	mV
A Open Loop Voltage Gain	A_{OL}		46	56	-	dB
B Output Sat. Voltage (pin 8)	$V_{SAT B}$	$R_L = 1$ k Ω , $V_{P2} = 0$ V	-	100	180	mV
A Output Current Capability	I_{OUT}		-	30	-	μA
Diode Voltage Drop	V_D	(S2 = b), $R_L = \infty$, (Note 4)	140	265	325	mV
Emitter Bias Voltage (pin 2)	V_{RE}		21.5	30	35.5	mV
On-chip Microphone Resistor	R_{MIC}		3	4	5	k Ω
On-chip Emitter Resistor	R_E		90	125	160	Ω
Input Referred Noise	IRN	NFB 0.2 to 10kHz at 12 dB/Oct	-	1	-	$\mu VRMS$
Harmonic Distortion	THD	500 mVRMS Output	-	1	-	%

All parameters and switches remain as shown in Test Circuit unless otherwise stated in CONDITIONS column.

NOTES: 1. $I_{BIAS A} = (V_{P4} - V_{P4(RFA = 1M)}) / 1M$

2. $V_{OH A} = (V_{P3} - V_{P3} [VIN = 0.4VDC, RFA = \infty, IP3 = -10 \mu A])$

3. $V_{OL A} = (V_{P3} - V_{P3} [IIN = +1 \mu A, RFA = \infty, IP3 = +10 \mu A])$

4. $V_D = (V_{P8} [Id = +(1.5 \times I_{TRANS})] - V_{P8} [Id = +(0.5 \times I_{TRANS})]) / 2$

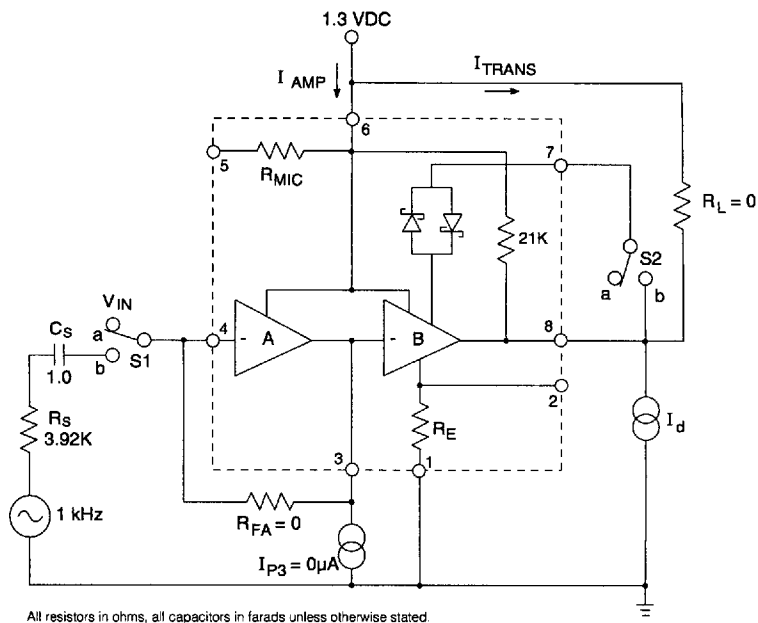


Fig. 1 Test Circuit

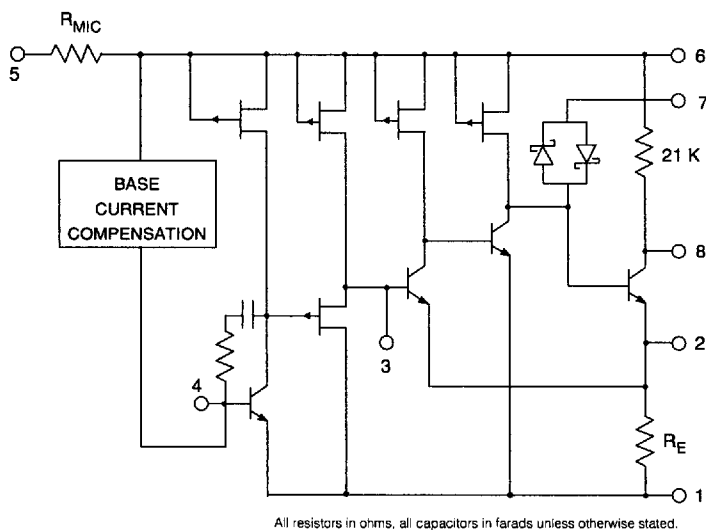
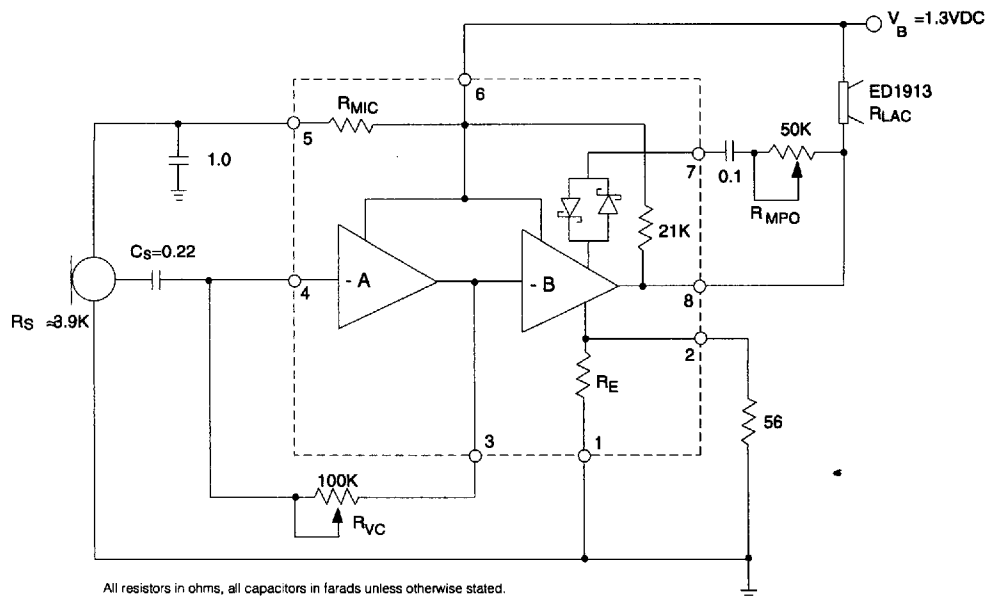


Fig. 2 Functional Schematic



$$\text{Gain of Stage A} = 20 \log \frac{R_{VC}}{R_S} \qquad \text{Gain of Stage B} = 20 \log \frac{R_{LAC} \parallel 21K}{56 \parallel R_F}$$

Fig. 3 Typical Hearing Aid Application

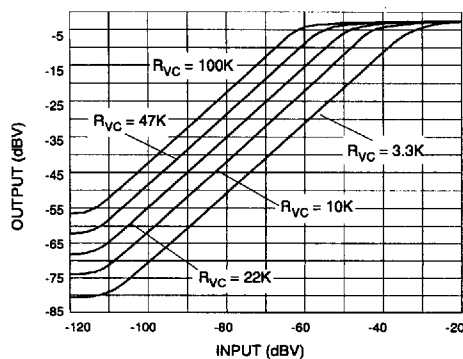


Fig. 4 I/O Curves at Various R_{VC} Settings

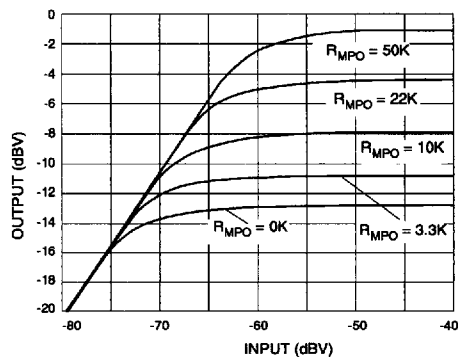


Fig. 5 I/O Curves at Various R_{MPO} Values

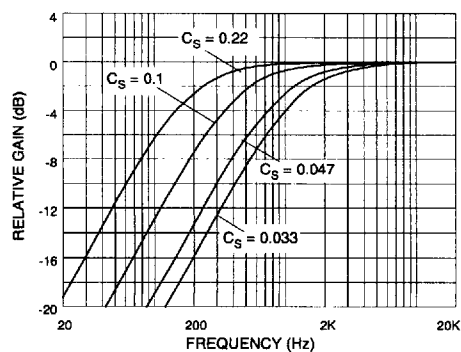


Fig. 6 Closed Loop Frequency Response with Various C_S Values

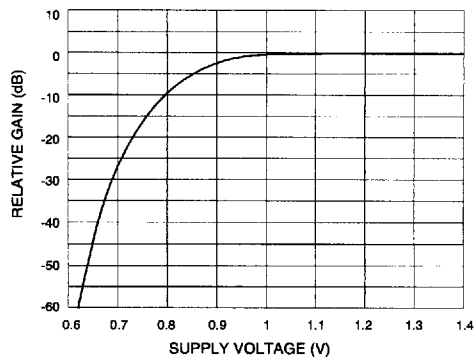


Fig. 7 Gain vs Supply Voltage

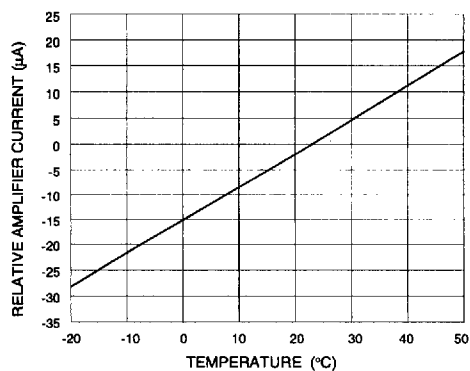


Fig. 8 Amplifier Current vs Temperature

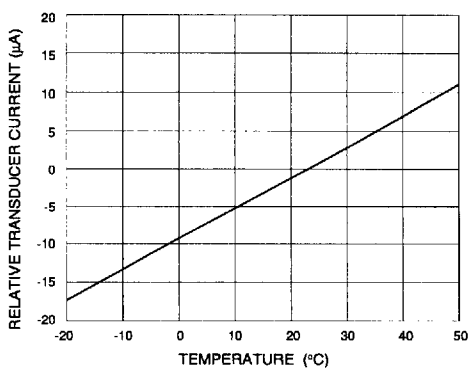


Fig. 9 Transducer Current vs Temperature

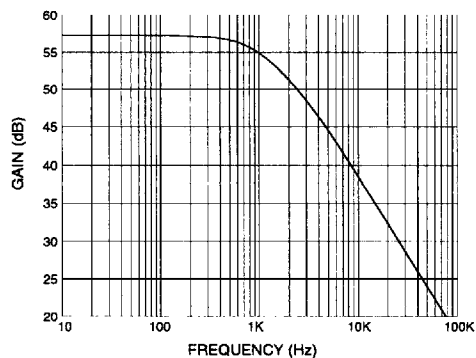


Fig. 10 Preamplifier Open Loop Frequency Response

REVISION NOTES

Au bump removed


GENNUM
CORPORATION

Assembly Methods for SLT Packaged Integrated Circuits

8 & 10 PIN SLT APPLICATION NOTE

T-90-20

INTRODUCTION

The SLT is a miniature fine pitch plastic encapsulation housing an integrated circuit. The packaging utilizes tape automated bonding (TAB) technology, and has leads folded on the side of the plastic capsule. The distance between the leads is 2.38mm (0.094") with overall height of 1.17mm (0.046") maximum. The outline dimensions of the packages are:

8 Pin 2.38 (0.094") x 2.40 (0.094") x 1.17 mm (0.046")

10 Pin 2.38 (0.094") x 2.91 (0.115") x 1.17 mm (0.046")

Why SLT? The name of this product is an acronym for Stub Lead Tab Pack. Gennum has developed the SLT brand packaging for its miniature integrated circuit audio amplifiers to satisfy two distinct market needs.

The first need is driven by market demands to supply circuits in smaller packages to meet dimensional requirements of an industry that is producing products of continually decreasing size and increasing complexity, utilizing smaller real estate than chip/wire.

The second need is to supply a miniature packaged circuit which can be tested prior to assembly into a hybrid circuit using alumina substrates, epoxy printed circuit boards or flex circuit boards and offers "reworkability", (i.e. aid's "manufacturability").

The purpose of what follows is to provide assistance to design and production personnel in the assembly of SLT packaged devices onto miniature printed circuit boards or ceramic substrates. The technical details encompassed in this note are based on Gennum's findings.

SUGGESTED PAD GEOMETRY FOR SLT PACKAGED DEVICES

The lands to which SLT terminals are to be soldered should be located in accordance with the SLT terminal pattern shown in Figures 1 and 2 and should carefully be placed and sized. The dimensions of the lands and adjacent conductors must be properly determined so that the solder will not run onto the conductors and will hold the SLT devices firmly in place. The lands should ideally be 0.05 mm (0.002 inch) per side larger than the SLT lead width, causing a fillet to be formed at the contact edges. If any conductor is wider than 0.254 mm (0.010 inch), it should be necked to 0.254 mm (0.010"), as shown in Figure 2. The purpose of necking down the conductors is to prevent solder back flow (this rule is applicable when no solder resist is used). Although it is strongly recommended that solder resist be used where possible.

Note: It is very important to ensure that the coplanarity of the solder pads on the circuit board substrate be maintained to very tight tolerances.

STENCIL DESIGN

Because of the fine pitch of the SLT, it is recommended that metal stencil be used instead of screen stencil. The stencil or mask should be 0.1 mm (0.004") thick, with the pattern obtained by an etching process. It is important that the stencil be etched simultaneously from both sides to reduce undercutting of the pattern, and the amount of under cutting should be compensated for during the manufacture of the stencil.

A suggested solder mask pattern is shown in Figure 3. The solder paste should be applied to all the lands on the substrate in one stroke through the stencil as shown in Figure 5. The metal stencil is stretched tight and cemented to a fixture as shown in Figure 6.

The fixture is attached to a hinged platform, so that it can be raised to permit loading of the substrate onto a vacuum chuck located directly below. Exact positioning of the substrate on the vacuum pedestal can be best achieved by a series of locating pins. Vacuum hold-down is required to hold the substrate fixed when the stencil is raised for "snap-off" from the solder paste pattern.

Note: All other devices which are to be surface mounted, should have their solder paste screened on at the same time, (i.e. stencil should be designed as such).

For high volume production, the pattern can be step and repeated "N" number of times, to correspond with the "N" number of circuit board patterns being assembled. The accuracy and consistency of solder paste application in this instance should be taken into account in the stencil design.

SCREEN PRINTING

To set up initially, the operator places the substrate on the vacuum chuck and lowers the stencil onto the substrate. Solder paste is applied using a teflon or polyurethane squeegee as shown in Fig. 7 (for high volume production, automated screen printers are usually available). This produces a uniform paste layer of a thickness equal to the metal stencil.

After the solder paste has been screened, the stencil must be raised vertically to provide a "snap-off". This motion is necessary to leave a well defined pattern on the substrate. Any horizontal movement will smear the pattern and increase the possibility of solder bridging of conductors on solder reflow.

The substrate is now ready for placement of surface mount components.

SOLDER REFLOW

The SLT can be easily soldered to the substrate using solder reflow techniques. Fig. 4 illustrates typically the solder temperature profile used to reflow SLTs.

For rigid substrates a 63 Sn/37 Pb solder cream (90% metal, -325 +500 mesh or type 3), containing the necessary flux is screened onto the land area. Kester Part #R-229-25 RMA or Alpha Part # RMA-390 DH3 performs well with no solder bridging evident. Excellent fillet formation at the land/device contact interface is apparent.

RECOMMENDED STEPS IN ASSEMBLY

Note: No precleaning of SLT devices is required prior to use.

STEP 1 SOLDER PASTE APPLICATION

Solder paste is screened onto the substrate using a squeegee as discussed under the heading "screen printing".

Important variables:

- age of solder paste
- time between solder paste application and reflow
- accuracy and consistency in placing solder paste

STEP 2 DEVICE PLACEMENT

The SLT is placed on the land area of the substrate with use of tweezers. A low power magnifier will assist the operator in easy, accurate location of the device over the circuit lands. It is best to bring the device above the application area, then descend vertically in one movement to avoid smearing the solder cream. It is important to precisely position the device over the contact lands.

For high volume production, the pick and place machine should have vision capability with two attributes:

1. Board error correction and
2. Component lead inspection (from under the device), or alternatively a dedicated pickup head with a recess shaped to the top section of SLT and vacuum for pickup can be used to center and square the device for placement.

The accurate placement of SLT devices is important in obtaining excellent soldering results, as the solder paste will not correct poor placement.

To prevent lead bending and maintain the pitch to pitch dimensions, the device should not be held or manipulated by the leads. Consistency and control of the placement force is also required.

STEP 3 SOLDER REFLOW

Heating the SLT and substrate for reflow soldering at 215°C (as measured at the lead/land interface) can be accompanied by any of the following techniques.

- A) Infra-red solder reflow oven.
- B) Vapor phase solder reflow.

Two versions are available:

- B1 Batch type (immersion)
- B2 Conveyor type

- C) Conduction / convection - this method is not preferred as the process is difficult to control.

Since Gennum believes that these techniques are well known to users of our circuits, no discussion of them is included in this note.

STEP 4 CLEANING

Cleaning the completed hybrid circuit is the final step in this assembly process. Ultrasonic cleaning is preferred to remove the flux residue which could corrode the solder joint in time.

STEP 5 INSPECTION/PROCESS MONITORING

The importance of process selection (for optimum yields) and control is very critical in the successful use of SLT devices. It is of utmost importance to ensure the any deviation from the "normally" expected soldering results, be analyzed and the cause be established, such that steps can be taken to bring the process back into control.

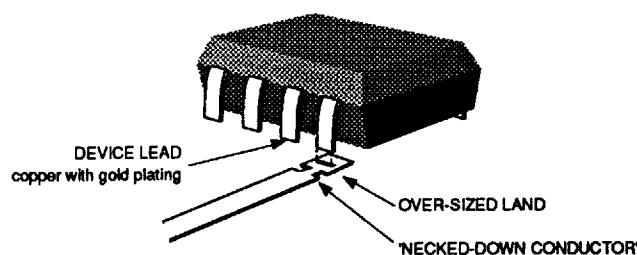
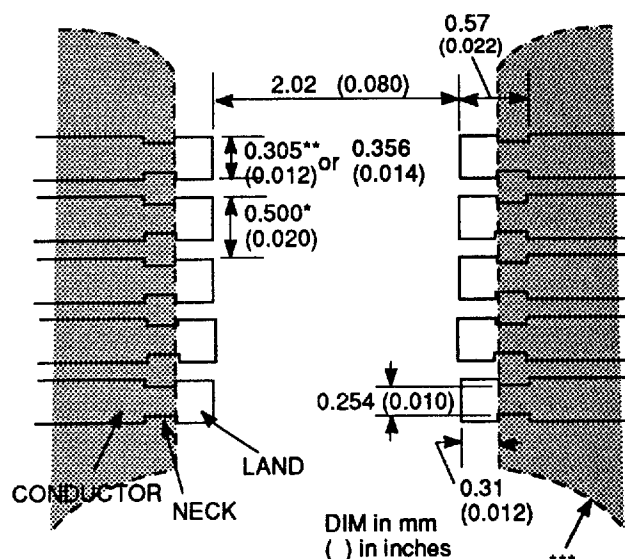


Fig. 1 Location of Conductor relative to Device Lead

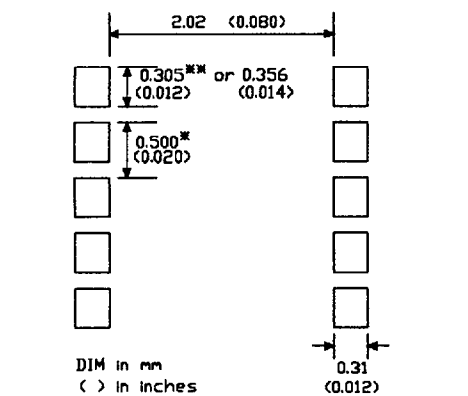


* 4 spaces at 0.5 ± 0.05 non-cumulative for 8 pin SLT
5 spaces at 0.5 ± 0.05 non-cumulative for 10 pin SLT

** Size should be established based on
• choice of interconnect medium
• assembly process capability

*** Extent of solder resist, in which case "necking" will not be required. It is of utmost importance to have symmetrical pads only.

Fig. 2 SLT Solder Pad Pattern



* 4 spaces at 0.5 ± 0.05 non-cumulative for 8 pin SLT
5 spaces at 0.5 ± 0.05 non-cumulative for 10 pin SLT

** Choice of size should correspond with size selected in Fig. 2.

Fig. 3 Solder Mask Pattern for SLT

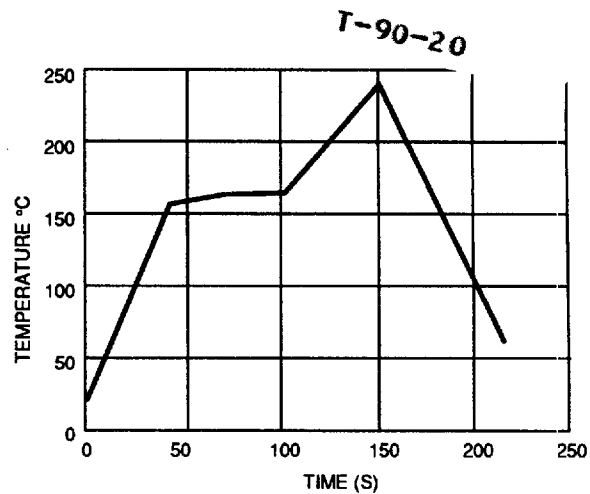


Fig. 4 SLT Solder Reflow Temperature Profile

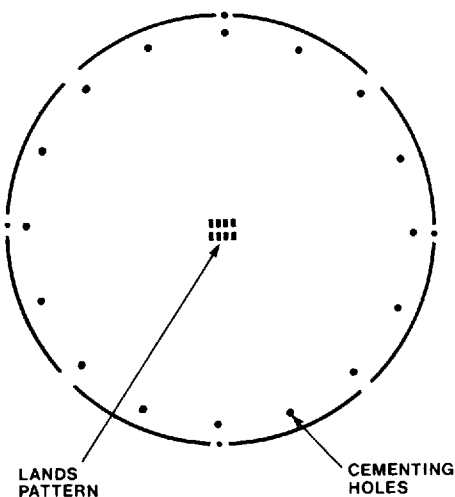


Fig. 5 Stencil for Solder Paste

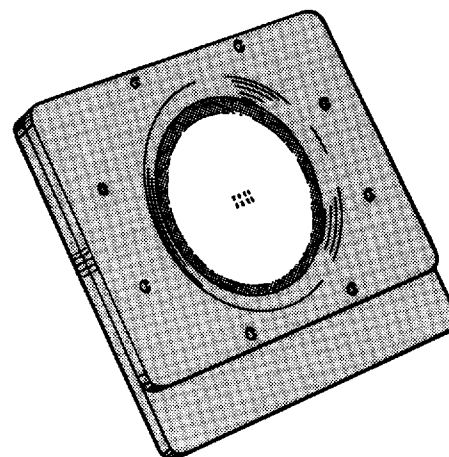


Fig. 6 Holding Plate for Stencil

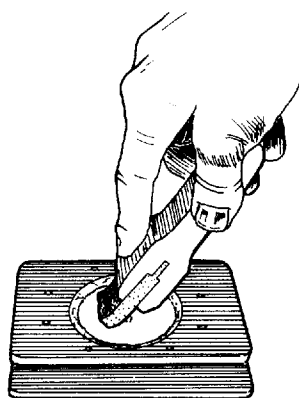


Fig. 7 Screen Printing of Paste with Squeegee