Description

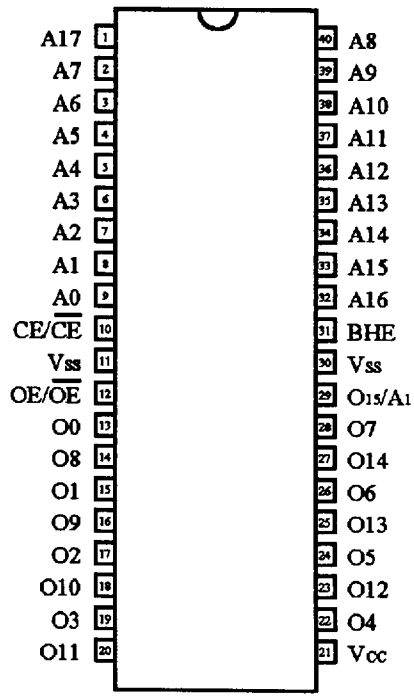
The GM23C4100B high performance read only memory is organized either as 524,288 x 8 bits (byte mode) or 262,144 x 16 bits (word mode) followed by BHE mode select. The GM23C4100B offers automatic power down controlled by the make programmed CE or $\overline{CE}$ input. The low power feature allows the battery operation. The large size of 4M bit memory density is ideal for character generator, data or program memory in microprocessor application. The GM23C4100B is packaged in 40 pin DIP or 40pin SOP.

Features

- Switchable Organization
  Byte Mode : 524,288 x 8 bit
  Word Mode : 262,144 x 16 bit
- Single + 5V Supply
- Access Time : 100/120 / 150 ns (Max)
- Operating current : 50mA (Max)
- Standby current : 50μA (Max)
- TTL-compatible inputs and outputs
- Polarity programmable chip enable and out enable pin
- Byte or Word switchable by BHE pin
  (BHE can be switched on the fly or a DC signal)
- 3-State outputs for wired-OR expansion
- Fully static operation
- Package : GM23C4100BFW : 40 Pin Plastic SOP (525 mil)
  GM23C4100B : 40 Pin Plastic DIP (600 mil)

Pin Configuration

40 SOP/DIP



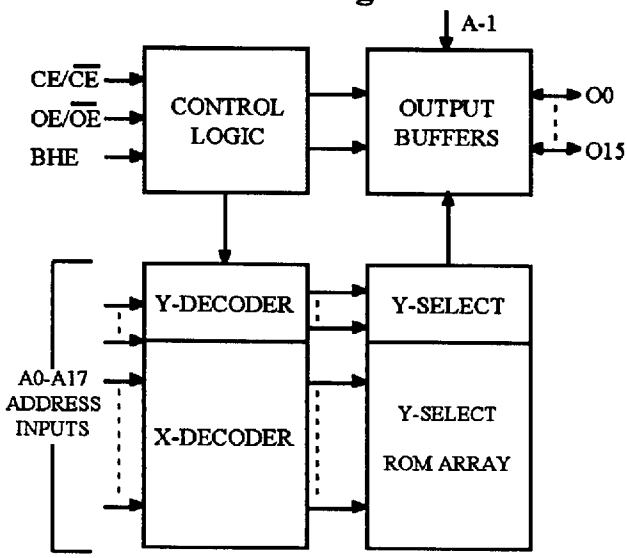
(Top View)

Pin Description

Pin	Function
A0-A17	Address Inputs
O0-O14	Data Outputs
O15/A-1	Output O15 (Word Mode)/ LSB Address (Byte Mode)
BHE	Word/Byte Selection
$\overline{CE}$/CE*	Chip Enable Input
$\overline{OE}$/OE*	Output Enable Input
Vcc	Power Supply (+5V)
Vss	Ground

*User Selectable Polarity.

Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Operating Temperature	-10 ~ 80	℃
T_{STG}	Storage Temperature	-65 ~ 150	℃
V_{CC}	Supply Voltage to Ground Potential	-0.5 ~ V_{CC} + 0.5	V
V_{OUT}	Output Voltage	-0.5 ~ V_{CC} + 0.5	V
V_{IN}	Input Voltage	-0.5 ~ 7.0	V

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratinge only functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (V_{CC} = 5.0V ± 10%, T_A = 0 ~ 70℃)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

DC Electrical Characteristics (V_{CC} = 5.0V ± 10%, T_A = 0 ~ 70℃)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = -1mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			0.4	V
$I_{I(L)}$	Input Leakage Current	V_{IN} = 0V to V_{CC}			±10	μA
$I_{O(L)}$	Output Leakage Current	V_{OUT} = 0V to V_{CC}			±10	μA
I_{CC}	Operating Supply Current (f = 6.7 MHz) Io=0 uA	$\overline{CE}$ = V_{IL}, CE = V_{IH}			50	mA
I_{SB1}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}, all Output Open			1	mA
I_{SB2}	Standby Current (CMOS)	$\overline{CE}$ = Vcc, all Output Open			50	μA

Capacitance (T_A = 25℃, f = 1.0 MHz)

Symbol	Parameter	Condition	Min	Max	Unit
C_I	Input Capacitance	V_{IN} = 0V		10	pF
C_O	Output Capacitance	V_{OUT} = 0V		10	pF

Note : Capacitance is periodically sampled and not 100% tested.

Mode Selection

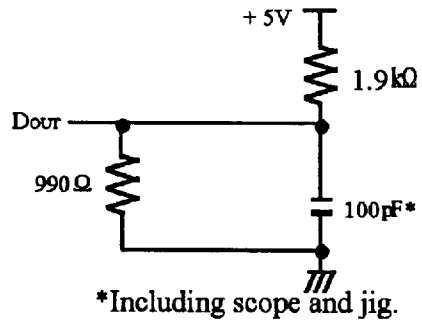
Mode	CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	O0~07	O8~014	O15/A-1	Power
Standby	L/H	X	X	High-Z			Standby
16 Bit Operating	H/L	H/L	H	Data Out			Active
8 Bit Operating			L	Data Out (Lower 8 Bit)	High-Z	L	
				Data Out (Upper 8 Bit)		H	
Output Disable		L/H	X	High-Z		X	

AC Operating Characteristics ($V_{CC} = 5.0V \pm 10\%$, $T_A = 0 \sim 70℃$)

Symbol	Parameter	GM23C4100B-10		GM23C4100B-12		GM23C4100B-15		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	100		120		150		ns
t_{ACE}	Chip Enable Access Time		100		120		150	ns
t_{AA}	Address Access Time		100		120		150	ns
t_{AOE}	Output Enable Access Time		50		60		70	ns
t_{OH}	Output Hold From Address Change	0		0		0		ns
t_{OHZ} t_{CHZ}	Output or Chip Disable to Output High-Z		40		50		60	ns
t_{OLZ} t_{CLZ}	Output or Chip Enable to Output Low-Z	10		10		10		ns

AC Test Condition

Input Pulse Level	0.4V to 2.4V
Input Rise and Fall Time	10ns
Input and Output Timming Level	0.8V to 2.0V
Output Load	See Fig. 1



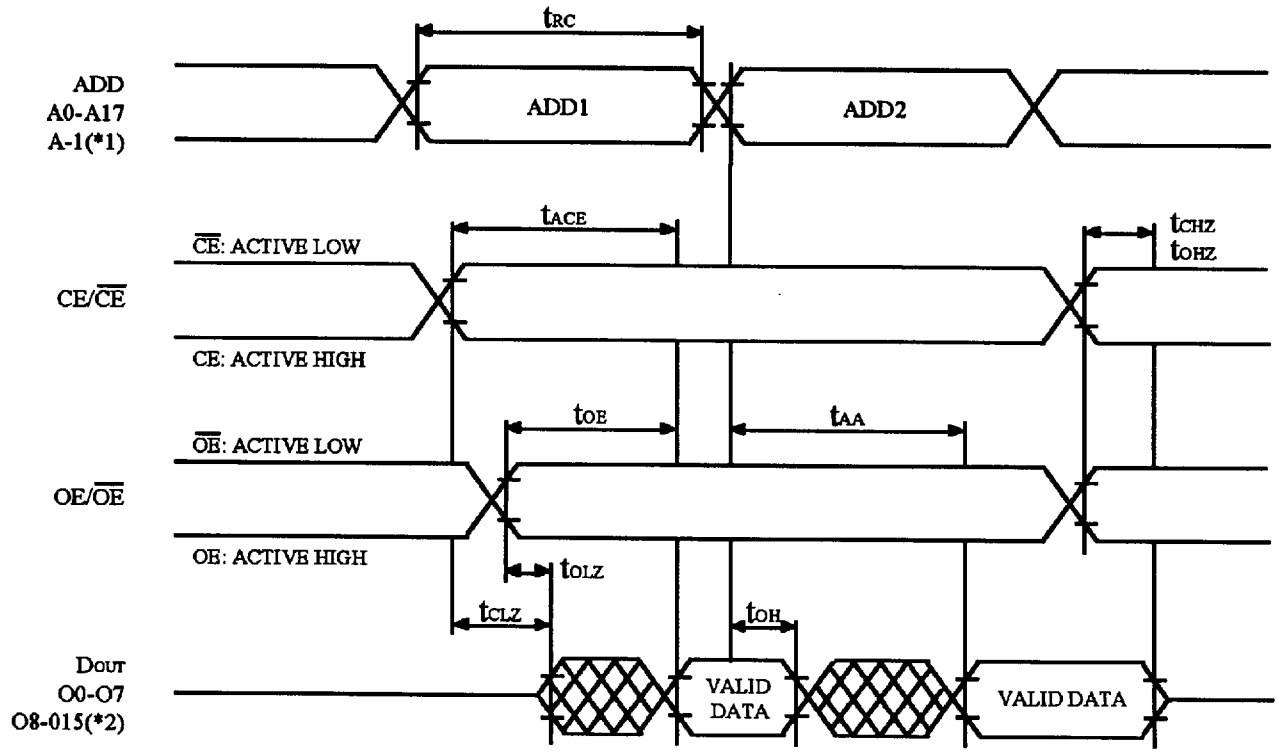
*Including scope and jig.

Fig. 1 Output Load Circuit

Timing Waveforms

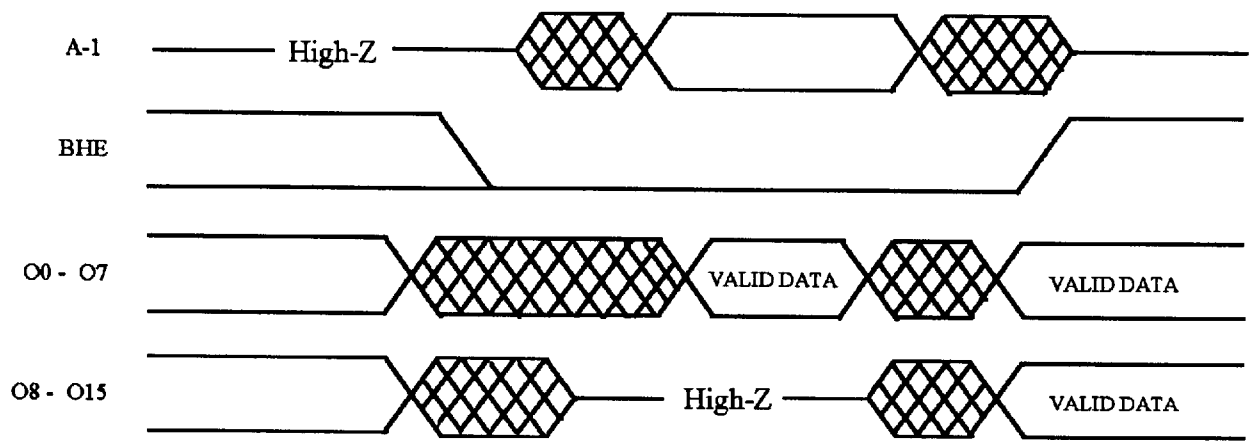
Read

Word Mode (BHE=V_{IH}) / Byte Mode (BHE=V_{IL})



(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})
(*2) Word Mode only. (BHE = V_{IH})

Word Mode / Byte Mode Switch

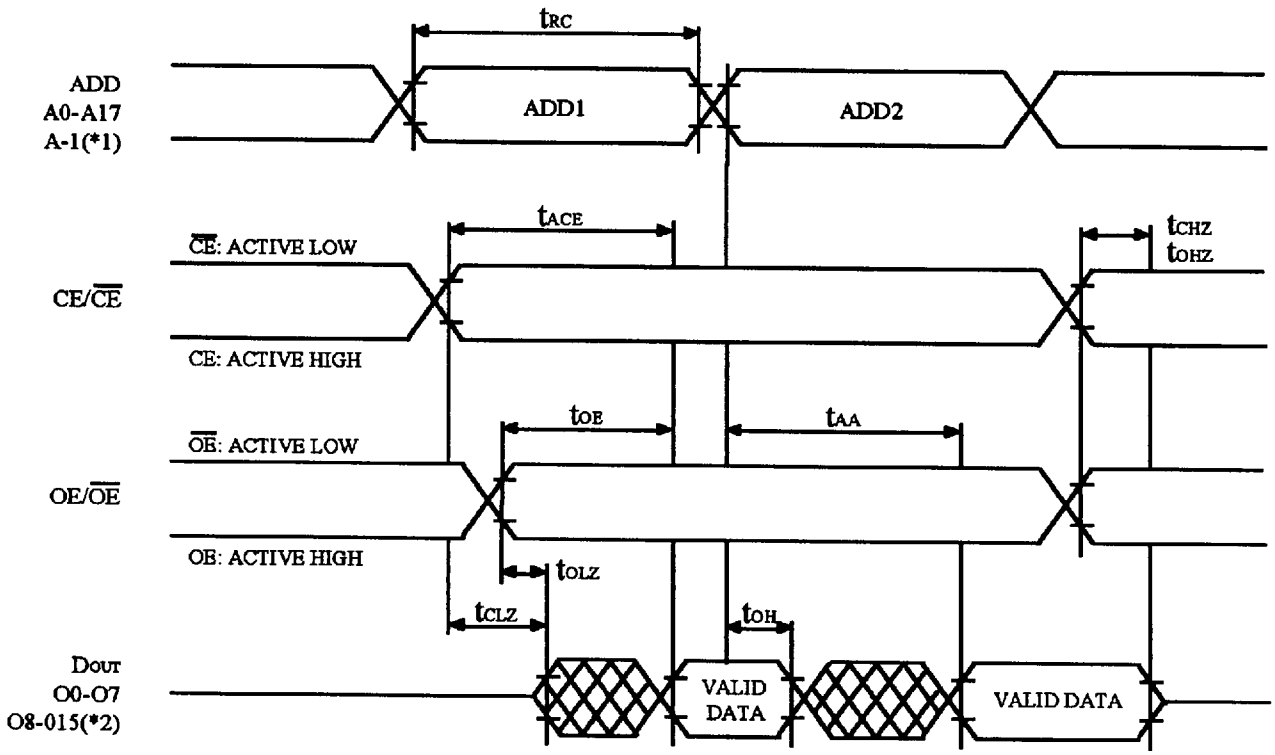


Notes : 1. CE/$\overline{CE}$, OE/$\overline{OE}$ are enable A0 - A17 are Valid.
2. If BHE is high and CE, OE is enable O15/A-1 pin is the output state.
3. Therefore the input signals of opposite phase to the outputs must not be applied to them.

Timing Waveforms

Read

Word Mode (BHE=V_{IH}) / Byte Mode (BHE=V_{IL})



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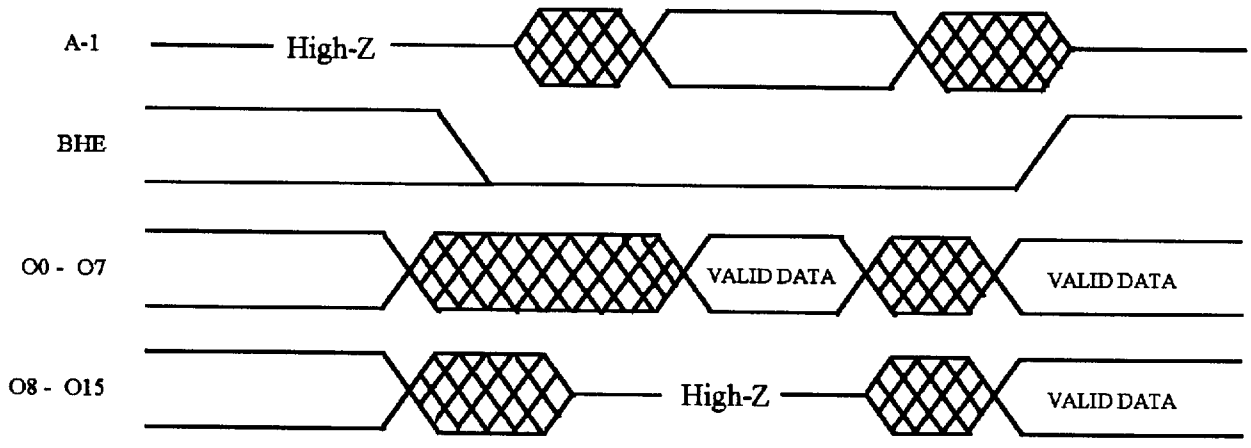
Word Mode / Byte Mode Switch



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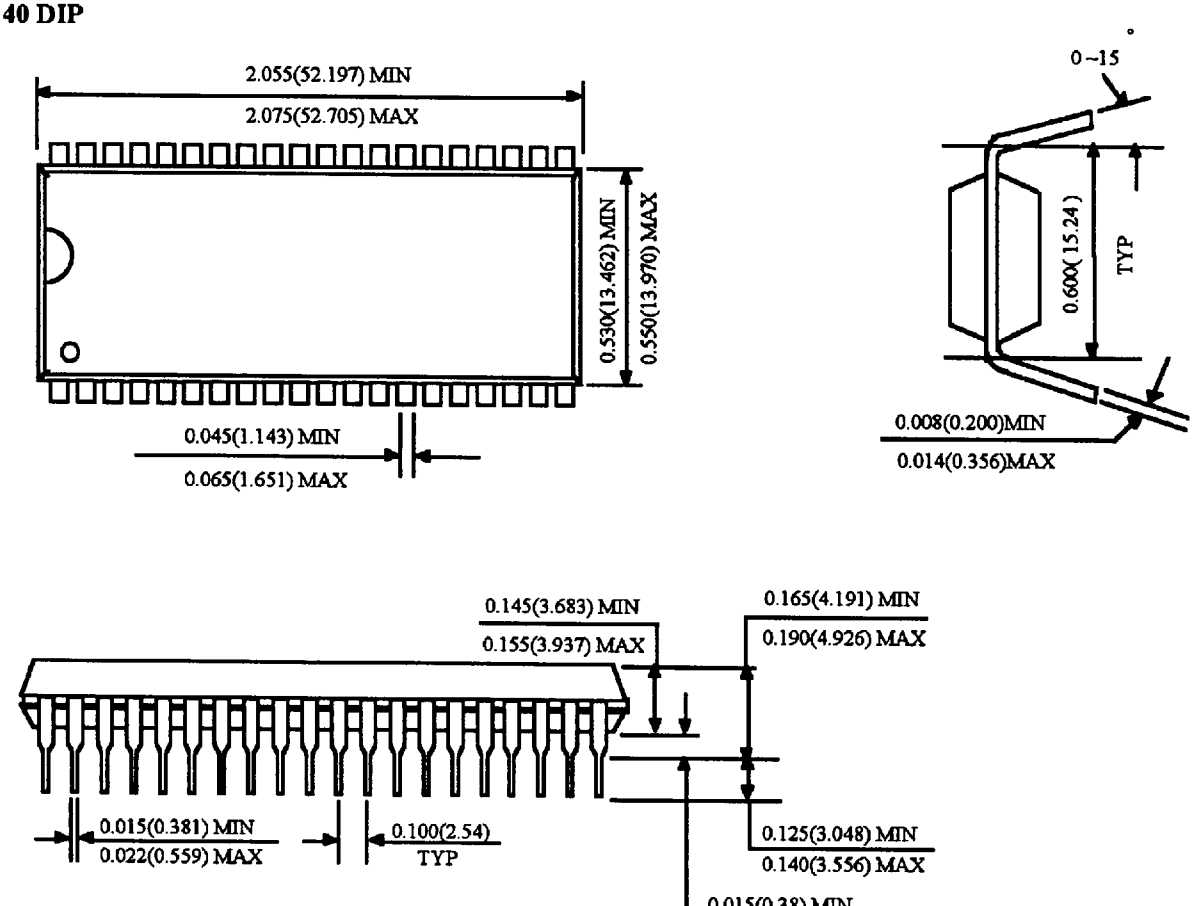
Package Dimensions

Unit: Inches (mm)

40 DIP



40 SOP