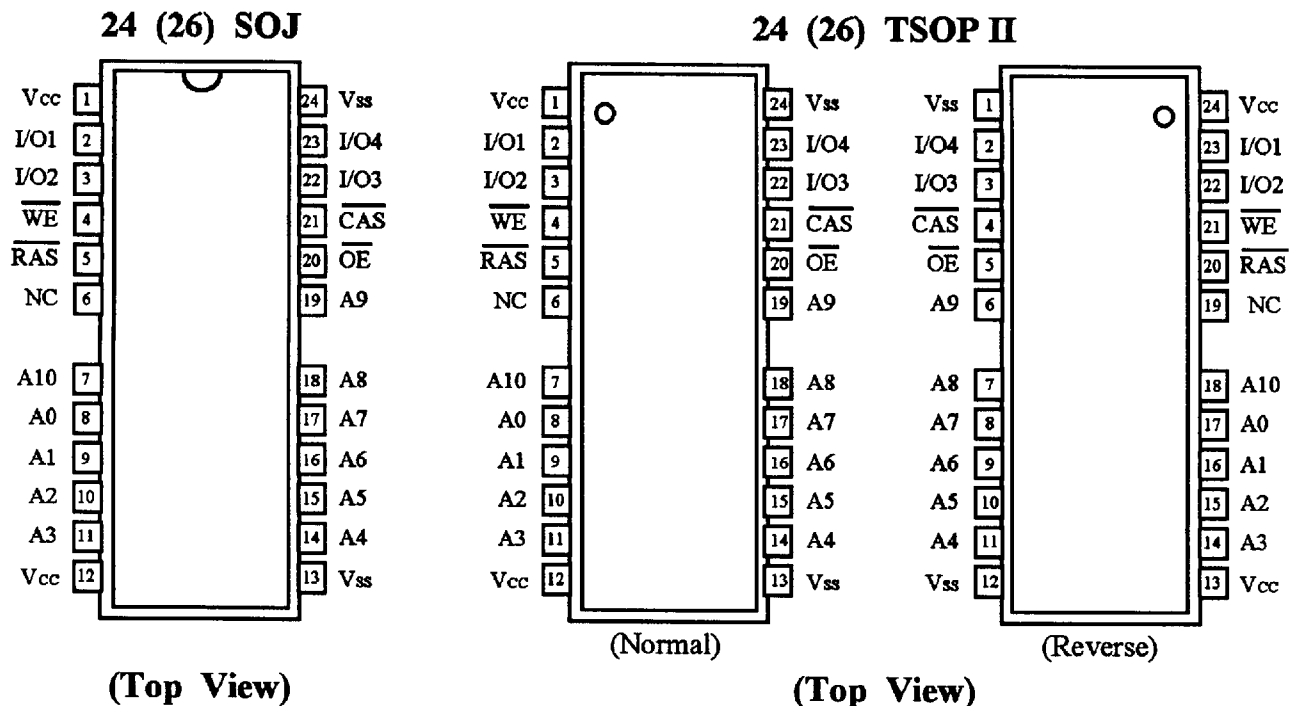




## Description

The GM71C17400B/BL is the new generation dynamic RAM organized 4,194,304 words x 4 Bit. GM71C17400B/BL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C17400B/BL offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71C17400B/BL to be packaged in a standard 300 mil 24 (26) pin SOJ and standard 300mil 24(26)pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply  $5V \pm 10\%$  tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

## Pin Configuration



## Features

- 4,194,304 Words x 4 Bit
- Fast Page Mode Capability
- Single Power Supply ( $5V \pm 10\%$ )
- Fast Access Time & Cycle Time (Unit: ns)

|                  | t <sub>rac</sub> | t <sub>cac</sub> | t <sub>rc</sub> | t <sub>pc</sub> |
|------------------|------------------|------------------|-----------------|-----------------|
| GM71C17400B/BL-6 | 60               | 15               | 110             | 40              |
| GM71C17400B/BL-7 | 70               | 18               | 130             | 45              |
| GM71C17400B/BL-8 | 80               | 20               | 150             | 50              |

- Low Power
  - Active : 605/550/495mW (MAX)
  - Standby : 5.5mW (CMOS level : MAX)
  - 0.83mW (L-version : MAX)
- $\overline{\text{RAS}}$  Only Refresh,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 2048 Refresh Cycles/32ms
- 2048 Refresh Cycles/128ms (L-version)
- Battery Back Up Operation (L-version)
- Test function : 16-bit parallel test mode

### Pin Description

| Pin              | Function               | Pin             | Function          |
|------------------|------------------------|-----------------|-------------------|
| A0-A10           | Address Inputs         | $\overline{WE}$ | Read/Write Enable |
| A0-A10           | Refresh Address Inputs | $\overline{OE}$ | Output Enable     |
| I/O1-I/O4        | Data Input/Data Output | V <sub>CC</sub> | Power (+5V)       |
| $\overline{RAS}$ | Row Address Strobe     | V <sub>SS</sub> | Ground            |
| $\overline{CAS}$ | Column Address Strobe  | NC              | No Connection     |

### Ordering Information

| Type No.                                                       | Access Time             | Package                                                     |
|----------------------------------------------------------------|-------------------------|-------------------------------------------------------------|
| GM71C17400BJ/BLJ-6<br>GM71C17400BJ/BLJ-7<br>GM71C17400BJ/BLJ-8 | 60 ns<br>70 ns<br>80 ns | 300 Mil<br>24 (26) Pin<br>Plastic SOJ                       |
| GM71C17400BT/BLT-6<br>GM71C17400BT/BLT-7<br>GM71C17400BT/BLT-8 | 60 ns<br>70 ns<br>80 ns | 300 Mil<br>24 (26) Pin<br>Plastic TSOP II<br>(Normal Type)  |
| GM71C17400BR/BLR-6<br>GM71C17400BR/BLR-7<br>GM71C17400BR/BLR-8 | 60 ns<br>70 ns<br>80 ns | 300 Mil<br>24 (26) Pin<br>Plastic TSOP II<br>(Reverse Type) |

### Absolute Maximum Ratings\*

| Symbol                            | Parameter                                              | Rating     | Unit |
|-----------------------------------|--------------------------------------------------------|------------|------|
| T <sub>A</sub>                    | Ambient Temperature under Bias                         | 0 ~ 70     | °C   |
| T <sub>STG</sub>                  | Storage Temperature (Plastic)                          | -55 ~ 125  | °C   |
| V <sub>IN</sub> /V <sub>OUT</sub> | Voltage on any Pin Relative to V <sub>SS</sub>         | -1.0 ~ 7.0 | V    |
| V <sub>CC</sub>                   | Voltage on V <sub>CC</sub> Relative to V <sub>SS</sub> | -1.0 ~ 7.0 | V    |
| I <sub>OUT</sub>                  | Short Circuit Output Current                           | 50         | mA   |
| P <sub>D</sub>                    | Power Dissipation                                      | 1.0        | W    |

\*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

### Recommended DC Operating Conditions (T<sub>A</sub> = 0 ~ 70°C)

| Symbol          | Parameter          | Min  | Typ | Max | Unit |
|-----------------|--------------------|------|-----|-----|------|
| V <sub>CC</sub> | Supply Voltage     | 4.5  | 5.0 | 5.5 | V    |
| V <sub>IH</sub> | Input High Voltage | 2.4  | -   | 6.5 | V    |
| V <sub>IL</sub> | Input Low Voltage  | -1.0 | -   | 0.8 | V    |

**DC Electrical Characteristics** ( $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $T_A = 0 \sim 70^\circ C$ )

| Symbol    | Parameter                                                                                                                                              | Min   | Max      | Unit    | Note       |
|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------|-------|----------|---------|------------|
| $V_{OH}$  | Output Level<br>Output "H" Level Voltage ( $I_{OUT} = -2mA$ )                                                                                          | 2.4   | $V_{CC}$ | V       |            |
| $V_{OL}$  | Output Level<br>Output "L" Level Voltage ( $I_{OUT} = 2mA$ )                                                                                           | 0     | 0.4      | V       |            |
| $I_{CC1}$ | Operating Current<br>Average Power Supply Operating Current<br>( $\overline{RAS}$ , $\overline{CAS}$ Cycling: $t_{RC} = t_{RC} \text{ min}$ )          | 60 ns | -        | 110     | mA<br>1, 2 |
|           |                                                                                                                                                        | 70 ns | -        | 100     |            |
|           |                                                                                                                                                        | 80 ns | -        | 90      |            |
| $I_{CC2}$ | Standby Current (TTL)<br>Power Supply Standby Current<br>( $\overline{RAS}$ , $\overline{CAS} = V_{IH}$ , $D_{OUT} = \text{High-Z}$ )                  | -     | 2        | mA      |            |
| $I_{CC3}$ | $\overline{RAS}$ Only Refresh Current<br>Average Power Supply Current<br>$\overline{RAS}$ Only Refresh Mode<br>( $t_{RC} = t_{RC} \text{ min}$ )       | 60 ns | -        | 110     | mA<br>2    |
|           |                                                                                                                                                        | 70 ns | -        | 100     |            |
|           |                                                                                                                                                        | 80 ns | -        | 90      |            |
| $I_{CC4}$ | Fast Page Mode Current<br>Average Power Supply Current<br>Fast Page Mode<br>( $t_{RC} = t_{RC} \text{ min}$ )                                          | 60 ns | -        | 80      | mA<br>1, 3 |
|           |                                                                                                                                                        | 70 ns | -        | 70      |            |
|           |                                                                                                                                                        | 80 ns | -        | 65      |            |
| $I_{CC5}$ | Standby Current (CMOS)<br>Power Supply Standby Current<br>( $\overline{RAS}$ , $\overline{CAS} \geq V_{CC} - 0.2V$ , $D_{OUT} = \text{High-Z}$ )       | -     | 1        | mA      | 5          |
|           |                                                                                                                                                        | -     | 150      | $\mu A$ |            |
| $I_{CC6}$ | $\overline{CAS}$ -before- $\overline{RAS}$ Refresh Current<br>( $t_{RC} = t_{RC} \text{ min}$ )                                                        | 60 ns | -        | 110     | mA         |
|           |                                                                                                                                                        | 70 ns | -        | 100     |            |
|           |                                                                                                                                                        | 80 ns | -        | 90      |            |
| $I_{CC7}$ | Standby Current $\overline{RAS} = V_{IH}$<br>$\overline{CAS} = V_{IL}$<br>$D_{OUT} = \text{Enable}$                                                    | -     | 5        | mA      | 1          |
| $I_{CC8}$ | Battery Back Up Operating Current(C-MOS)<br>(Standby with CBR Refresh)<br>( $t_{RC}=62.5 \mu s$ , $t_{RAS} \leq 0.3 \mu s$ , $D_{OUT}=\text{High-Z}$ ) | -     | 350      | $\mu A$ | 4,5        |
| $I_{LQ}$  | Input Leakage Current<br>Any Input ( $0V \leq V_{IN} \leq 7V$ )                                                                                        | -10   | 10       | $\mu A$ |            |
| $I_{LQ}$  | Output Leakage Current<br>( $D_{OUT}$ is Disabled, $0V \leq V_{OUT} \leq 7V$ )                                                                         | -10   | 10       | $\mu A$ |            |

Note: 1.  $I_{CC}$  depends on output load condition when the device is selected.  $I_{CC}(\text{max})$  is specified at the output open condition.

2. Address can be changed once or less while  $\overline{RAS} = V_{IL}$ .

3. Address can be changed once or less while  $\overline{CAS} = V_{IH}$ .

4.  $\overline{CAS} = L$  ( $\leq 0.2V$ ) while  $\overline{RAS} = L$  ( $\leq 0.2V$ ).

5. L-version.

**Capacitance** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 25^\circ C$ )

| Symbol    | Parameter                        | Min | Max | Unit | Note |
|-----------|----------------------------------|-----|-----|------|------|
| $C_{I1}$  | Input Capacitance (Address)      | -   | 5   | pF   | 1    |
| $C_{I2}$  | Input Capacitance (Clocks)       | -   | 7   | pF   | 1    |
| $C_{I/O}$ | Output Capacitance (Data-In/Out) | -   | 7   | pF   | 1, 2 |

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.  
 2.  $\overline{CAS} = V_{IH}$  to disable Dour.

**AC Characteristics** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0 \sim 70^\circ C$ , Notes 1, 2, 18, 19)

**Test Conditions**

Input rise and fall times : 2 ns

Input timing reference levels : 0.8V, 2.4V

Output timing reference levels : 0.4V, 2.4V

Output load : 2 TTL gate + CL (100 pF)

(Including scope and jig)

**Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)**

| Symbol    | Parameter                                           | GM71C17400<br>B/BL-6 |        | GM71C17400<br>B/BL-7 |        | GM71C17400<br>B/BL-8 |        | Unit | Note |
|-----------|-----------------------------------------------------|----------------------|--------|----------------------|--------|----------------------|--------|------|------|
|           |                                                     | Min                  | Max    | Min                  | Max    | Min                  | Max    |      |      |
| $t_{RC}$  | Random Read or Write Cycle Time                     | 110                  | -      | 130                  | -      | 150                  | -      | ns   |      |
| $t_{RP}$  | $\overline{RAS}$ Precharge Time                     | 40                   | -      | 50                   | -      | 60                   | -      | ns   |      |
| $t_{CP}$  | $\overline{CAS}$ Precharge Time                     | 10                   | -      | 10                   | -      | 10                   | -      | ns   |      |
| $t_{RAS}$ | $\overline{RAS}$ Pulse Width                        | 60                   | 10,000 | 70                   | 10,000 | 80                   | 10,000 | ns   |      |
| $t_{CAS}$ | $\overline{CAS}$ Pulse Width                        | 15                   | 10,000 | 18                   | 10,000 | 20                   | 10,000 | ns   |      |
| $t_{ASR}$ | Row Address Setup Time                              | 0                    | -      | 0                    | -      | 0                    | -      | ns   |      |
| $t_{RAH}$ | Row Address Hold Time                               | 10                   | -      | 10                   | -      | 10                   | -      | ns   |      |
| $t_{ASC}$ | Column Address Setup Time                           | 0                    | -      | 0                    | -      | 0                    | -      | ns   |      |
| $t_{CAH}$ | Column Address Hold Time                            | 10                   | -      | 15                   | -      | 15                   | -      | ns   |      |
| $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay Time     | 20                   | 45     | 20                   | 52     | 20                   | 60     | ns   | 3    |
| $t_{RAD}$ | $\overline{RAS}$ to Column Address Delay Time       | 15                   | 30     | 15                   | 35     | 15                   | 40     | ns   | 4    |
| $t_{RSH}$ | $\overline{RAS}$ Hold Time                          | 15                   | -      | 18                   | -      | 20                   | -      | ns   |      |
| $t_{CSH}$ | $\overline{CAS}$ Hold Time                          | 60                   | -      | 70                   | -      | 80                   | -      | ns   |      |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 5                    | -      | 5                    | -      | 5                    | -      | ns   |      |
| $t_{ODD}$ | $\overline{OE}$ to $D_{IN}$ Delay Time              | 15                   | -      | 18                   | -      | 20                   | -      | ns   | 5    |
| $t_{DZO}$ | $\overline{OE}$ Delay Time from $D_{IN}$            | 0                    | -      | 0                    | -      | 0                    | -      | ns   | 6    |
| $t_{DZC}$ | $\overline{CAS}$ Set-up Time from $D_{IN}$          | 0                    | -      | 0                    | -      | 0                    | -      | ns   | 6    |
| $t_T$     | Transition Time (Rise and Fall)                     | 3                    | 50     | 3                    | 50     | 3                    | 50     | ns   | 7    |
| $t_{REF}$ | Refresh Period                                      | -                    | 32     | -                    | 32     | -                    | 32     | ms   |      |
|           | Refresh Period (L-version)                          | -                    | 128    | -                    | 128    | -                    | 128    | ms   |      |

### Read Cycle

| Symbol           | Parameter                                             | GM71C17400<br>B/BL-6 |     | GM71C17400<br>B/BL-7 |     | GM71C17400<br>B/BL-8 |     | Unit | Note           |
|------------------|-------------------------------------------------------|----------------------|-----|----------------------|-----|----------------------|-----|------|----------------|
|                  |                                                       | Min                  | Max | Min                  | Max | Min                  | Max |      |                |
| t <sub>RAC</sub> | Access Time from $\overline{\text{RAS}}$              | -                    | 60  | -                    | 70  | -                    | 80  | ns   | 8.9.20         |
| t <sub>CAC</sub> | Access Time from $\overline{\text{CAS}}$              | -                    | 15  | -                    | 18  | -                    | 20  | ns   | 9,10,<br>17,20 |
| t <sub>AA</sub>  | Access Time from Column Address                       | -                    | 30  | -                    | 35  | -                    | 40  | ns   | 9,11,<br>17,20 |
| t <sub>OAC</sub> | Access Time from $\overline{\text{OE}}$               | -                    | 15  | -                    | 18  | -                    | 20  | ns   | 9,20           |
| t <sub>RCS</sub> | Read Command Setup Time                               | 0                    | -   | 0                    | -   | 0                    | -   | ns   |                |
| t <sub>RCH</sub> | Read Command Hold Time to $\overline{\text{CAS}}$     | 0                    | -   | 0                    | -   | 0                    | -   | ns   | 12             |
| t <sub>RRH</sub> | Read Command Hold Time to $\overline{\text{RAS}}$     | 0                    | -   | 0                    | -   | 0                    | -   | ns   | 12             |
| t <sub>RAL</sub> | Column Address to $\overline{\text{RAS}}$ Lead Time   | 30                   | -   | 35                   | -   | 40                   | -   | ns   |                |
| t <sub>CAL</sub> | Column Address to $\overline{\text{CAS}}$ Lead Time   | 30                   | -   | 35                   | -   | 40                   | -   | ns   |                |
| t <sub>CLZ</sub> | $\overline{\text{CAS}}$ to Output in low-Z            | 0                    | -   | 0                    | -   | 0                    | -   | ns   |                |
| t <sub>OH</sub>  | Output Data Hold Time                                 | 3                    | -   | 3                    | -   | 3                    | -   | ns   |                |
| t <sub>OH0</sub> | Output Data Hold Time from $\overline{\text{OE}}$     | 3                    | -   | 3                    | -   | 3                    | -   | ns   |                |
| t <sub>OEZ</sub> | Output Buffer Turn-off Time to $\overline{\text{OE}}$ | -                    | 15  | -                    | 18  | -                    | 20  | ns   | 13             |
| t <sub>OFF</sub> | Output Buffer Turn-off Time                           | -                    | 15  | -                    | 15  | -                    | 15  | ns   | 13             |
| t <sub>CDD</sub> | $\overline{\text{CAS}}$ to D <sub>IN</sub> Delay Time | 15                   | -   | 18                   | -   | 20                   | -   | ns   | 5              |

### Write Cycle

| Symbol           | Parameter                                          | GM71C17400<br>B/BL-6 |     | GM71C17400<br>B/BL-7 |     | GM71C17400<br>B/BL-8 |     | Unit | Note |
|------------------|----------------------------------------------------|----------------------|-----|----------------------|-----|----------------------|-----|------|------|
|                  |                                                    | Min                  | Max | Min                  | Max | Min                  | Max |      |      |
| t <sub>WCS</sub> | Write Command Setup Time                           | 0                    | -   | 0                    | -   | 0                    | -   | ns   | 14   |
| t <sub>WCH</sub> | Write Command Hold Time                            | 10                   | -   | 15                   | -   | 15                   | -   | ns   |      |
| t <sub>WP</sub>  | Write Command Pulse Width                          | 10                   | -   | 10                   | -   | 10                   | -   | ns   |      |
| t <sub>RWL</sub> | Write Command to $\overline{\text{RAS}}$ Lead Time | 15                   | -   | 18                   | -   | 20                   | -   | ns   |      |
| t <sub>CWL</sub> | Write Command to $\overline{\text{CAS}}$ Lead Time | 15                   | -   | 18                   | -   | 20                   | -   | ns   |      |
| t <sub>DS</sub>  | Data-in Setup Time                                 | 0                    | -   | 0                    | -   | 0                    | -   | ns   | 15   |
| t <sub>DH</sub>  | Data-in Hold Time                                  | 10                   | -   | 15                   | -   | 15                   | -   | ns   | 15   |

### Read-Modify-Write Cycle

| Symbol           | Parameter                                                    | GM71C17400<br>B/BL-6 |     | GM71C17400<br>B/BL-7 |     | GM71C17400<br>B/BL-8 |     | Unit | Note |
|------------------|--------------------------------------------------------------|----------------------|-----|----------------------|-----|----------------------|-----|------|------|
|                  |                                                              | Min                  | Max | Min                  | Max | Min                  | Max |      |      |
| t <sub>RWC</sub> | Read-Modify-Write Cycle Time                                 | 155                  | -   | 181                  | -   | 205                  | -   | ns   |      |
| t <sub>RWD</sub> | $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time | 85                   | -   | 98                   | -   | 110                  | -   | ns   | 14   |
| t <sub>CWD</sub> | $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time | 40                   | -   | 46                   | -   | 50                   | -   | ns   | 14   |
| t <sub>AWD</sub> | Column Address to $\overline{\text{WE}}$ Delay Time          | 55                   | -   | 63                   | -   | 70                   | -   | ns   | 14   |
| t <sub>OEH</sub> | $\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$ | 15                   | -   | 18                   | -   | 20                   | -   | ns   |      |

### Refresh Cycle

| Symbol           | Parameter                                                                                                        | GM71C17400<br>B/BL-6 |     | GM71C17400<br>B/BL-7 |     | GM71C17400<br>B/BL-8 |     | Unit | Note |
|------------------|------------------------------------------------------------------------------------------------------------------|----------------------|-----|----------------------|-----|----------------------|-----|------|------|
|                  |                                                                                                                  | Min                  | Max | Min                  | Max | Min                  | Max |      |      |
| t <sub>CSR</sub> | $\overline{\text{CAS}}$ Set-up Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle) | 5                    | -   | 5                    | -   | 5                    | -   | ns   |      |
| t <sub>CHR</sub> | $\overline{\text{CAS}}$ Hold Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)   | 10                   | -   | 10                   | -   | 10                   | -   | ns   |      |
| t <sub>RPC</sub> | $\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time                                           | 0                    | -   | 0                    | -   | 0                    | -   | ns   |      |
| t <sub>WRP</sub> | $\overline{\text{WE}}$ Set-up Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)  | 0                    | -   | 0                    | -   | 0                    | -   | ns   |      |
| t <sub>WRH</sub> | $\overline{\text{WE}}$ Hold Time<br>( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)    | 10                   | -   | 10                   | -   | 10                   | -   | ns   |      |

### Fast Page Mode Cycle

| Symbol            | Parameter                                                                | GM71C17400<br>B/BL-6 |         | GM71C17400<br>B/BL-7 |         | GM71C17400<br>B/BL-8 |         | Unit | Note    |
|-------------------|--------------------------------------------------------------------------|----------------------|---------|----------------------|---------|----------------------|---------|------|---------|
|                   |                                                                          | Min                  | Max     | Min                  | Max     | Min                  | Max     |      |         |
| t <sub>PC</sub>   | Fast Page Mode Cycle Time                                                | 40                   | -       | 45                   | -       | 50                   | -       | ns   |         |
| t <sub>RASP</sub> | Fast Page Mode $\overline{\text{RAS}}$ Pulse Width                       | -                    | 100,000 | -                    | 100,000 | -                    | 100,000 | ns   | 16      |
| t <sub>ACP</sub>  | Access Time from $\overline{\text{CAS}}$ Precharge                       | -                    | 35      | -                    | 40      | -                    | 45      | ns   | 9,17,20 |
| t <sub>RHCP</sub> | $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge | 35                   | -       | 40                   | -       | 45                   | -       | ns   |         |
| t <sub>CPW</sub>  | $\overline{\text{WE}}$ Delay Time from $\overline{\text{CAS}}$ Precharge | 60                   | -       | 68                   | -       | 75                   | -       | ns   | 14      |
| t <sub>PRWC</sub> | Fast Page Mode Read-Modify-Write Cycle Time                              | 85                   | -       | 96                   | -       | 105                  | -       | ns   |         |

**Test Mode Cycle**<sup>\*20</sup>

| Symbol           | Parameter                                   | GM71C17400<br>B/BL-6 |     | GM71C17400<br>B/BL-7 |     | GM71C17400<br>B/BL-8 |     | Unit | Note |
|------------------|---------------------------------------------|----------------------|-----|----------------------|-----|----------------------|-----|------|------|
|                  |                                             | Min                  | Max | Min                  | Max | Min                  | Max |      |      |
| t <sub>WTS</sub> | Test Mode $\overline{\text{WE}}$ Setup Time | 0                    | -   | 0                    | -   | 0                    | -   | ns   |      |
| t <sub>WTH</sub> | Test Mode $\overline{\text{WE}}$ Hold Time  | 10                   | -   | 10                   | -   | 10                   | -   | ns   |      |

**Counter Test Cycle**

| Symbol           | Parameter                                                    | GM71C17400<br>B/BL-6 |     | GM71C17400<br>B/BL-7 |     | GM71C17400<br>B/BL-8 |     | Unit | Note |
|------------------|--------------------------------------------------------------|----------------------|-----|----------------------|-----|----------------------|-----|------|------|
|                  |                                                              | Min                  | Max | Min                  | Max | Min                  | Max |      |      |
| t <sub>CPT</sub> | $\overline{\text{CAS}}$ Precharge Time in Counter Test Cycle | 20                   | -   | 30                   | -   | 30                   | -   | ns   |      |

**Notes:**

1. AC Measurements assume  $t_r = 5\text{ ns}$ .
2. An initial pause of  $200\mu\text{s}$  is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing  $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh). If the internal refresh counter is used, a minimum of eight  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles are required.
3. Operation with the  $t_{\text{RCD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met,  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only; if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{CAC}}$ .
4. Operation with the  $t_{\text{RAD}}(\text{max})$  limit insures that  $t_{\text{RAC}}(\text{max})$  can be met,  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, then access time is controlled exclusively by  $t_{\text{AA}}$ .
5. Either  $t_{\text{ODD}}$  or  $t_{\text{CDD}}$  must be satisfied.
6. Either  $t_{\text{DZO}}$  or  $t_{\text{DZC}}$  must be satisfied.
7.  $V_{\text{IH}}(\text{min})$  and  $V_{\text{IL}}(\text{max})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{\text{IH}}(\text{min})$  and  $V_{\text{IL}}(\text{max})$ .
8. Assume that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$ . If  $t_{\text{RCD}}$  or  $t_{\text{RAD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  exceeds the value shown.
9. Measured with a load circuit equivalent to 2 TTL loads and  $100\text{pF}$ .
10. Assume that  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$ .
11. Assume that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$  and  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ .
12. Either  $t_{\text{RCH}}$  or  $t_{\text{RRH}}$  must be satisfied for a read cycles.
13.  $t_{\text{OFF}}(\text{max})$  and  $t_{\text{OEZ}}(\text{max})$  define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
14.  $t_{\text{WCS}}$ ,  $t_{\text{RWD}}$ ,  $t_{\text{CWD}}$ ,  $t_{\text{AWD}}$  and  $t_{\text{CPW}}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if  $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ , the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$ , the  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ , and  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ , or  $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ ,  $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$  and  $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$ , the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in delayed write or read-modify-write cycles.
16.  $t_{\text{RASC}}$  defines  $\overline{\text{RAS}}$  pulse width in fast page mode cycles.
17. Access time is determined by the longer of  $t_{\text{AA}}$  or  $t_{\text{CAC}}$  or  $t_{\text{ACP}}$



18. In delayed write or read-modify-write cycles,  $\overline{OE}$  must disable output buffer prior to applying data to the device. After  $\overline{RAS}$  is reset, if  $t_{OE} \geq t_{CWL}$ , the I/O pin will remain open circuit (high impedance); if  $t_{OE} \leq t_{CWL}$ , invalid data will be out at each I/O.
19. The 16M DRAM offers a 16-bit time saving parallel test mode. Address CA0 and CA1 for the 4M x 4 are don't care during test mode. Test mode is set by performing a  $\overline{WE}$ -and- $\overline{CAS}$ -before- $\overline{RAS}$  (WCBR) cycle. In 16-bit parallel test mode, data is written into 4 bits in parallel at each I/O (I/O1 to I/O4) and read out from each I/O. If 4 bits of each I/O are equal (all 1s or 0s), data output pin is high state during test mode read cycle, then the device has passed. If they are not equal, data output pin is a low state, then the device has failed. Refresh during test mode operation can be performed by normal read cycles or by WCBR refresh cycles. To get out of test mode and enter a normal operation mode, perform either a regular  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycle or  $\overline{RAS}$ -only refresh cycle.
20. In a test mode read cycle, the value of  $t_{RAC}$ ,  $t_{AA}$ ,  $t_{CAC}$  and  $t_{ACP}$  is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.



## Timing Waveforms

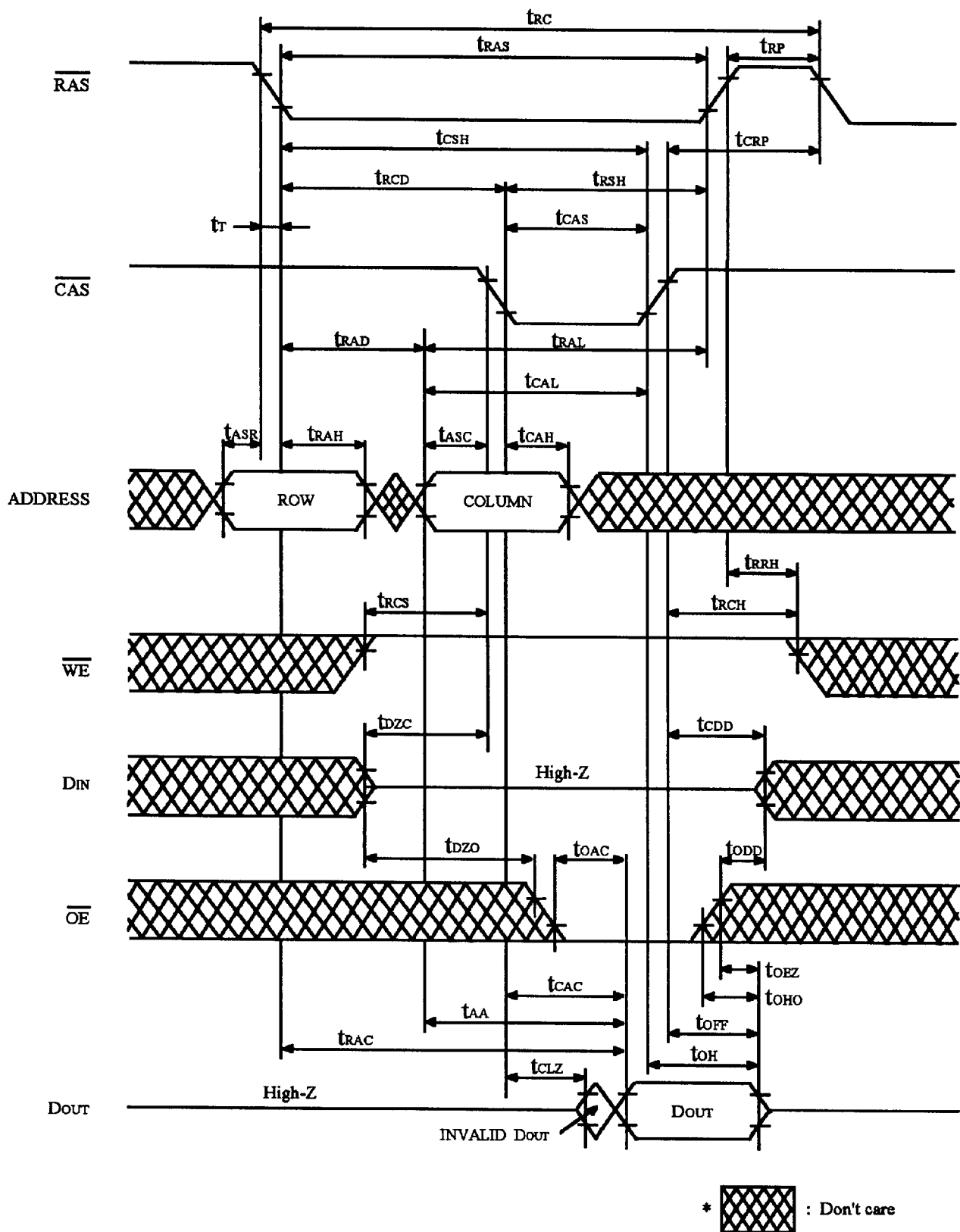
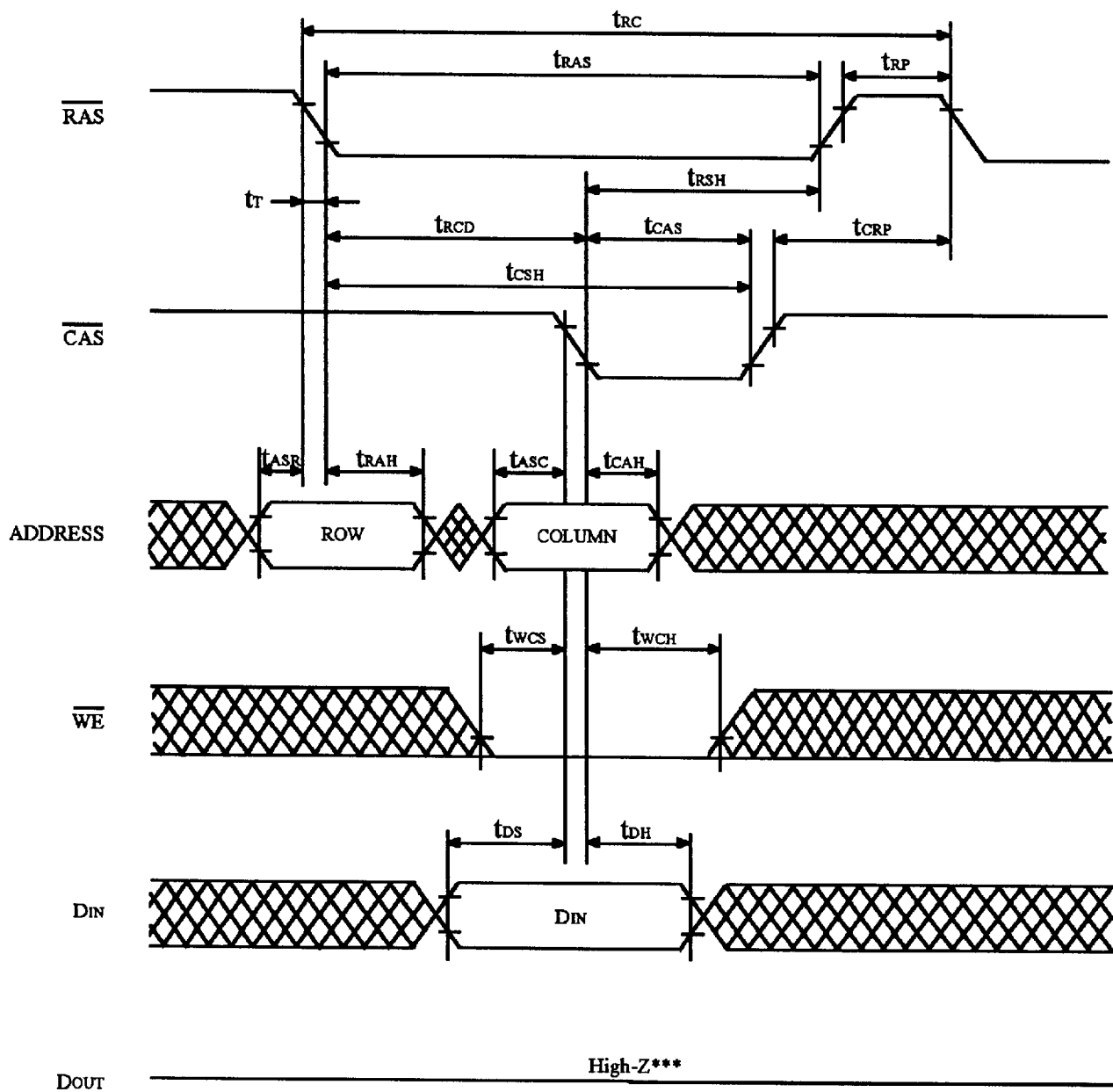


FIGURE 1. READ CYCLE



\*  : Don't care

\*\*  $\overline{OE}$  : Don't care

\*\*\*  $t_{WCS} \geq t_{WCS}(\min)$

FIGURE 2. EARLY WRITE CYCLE

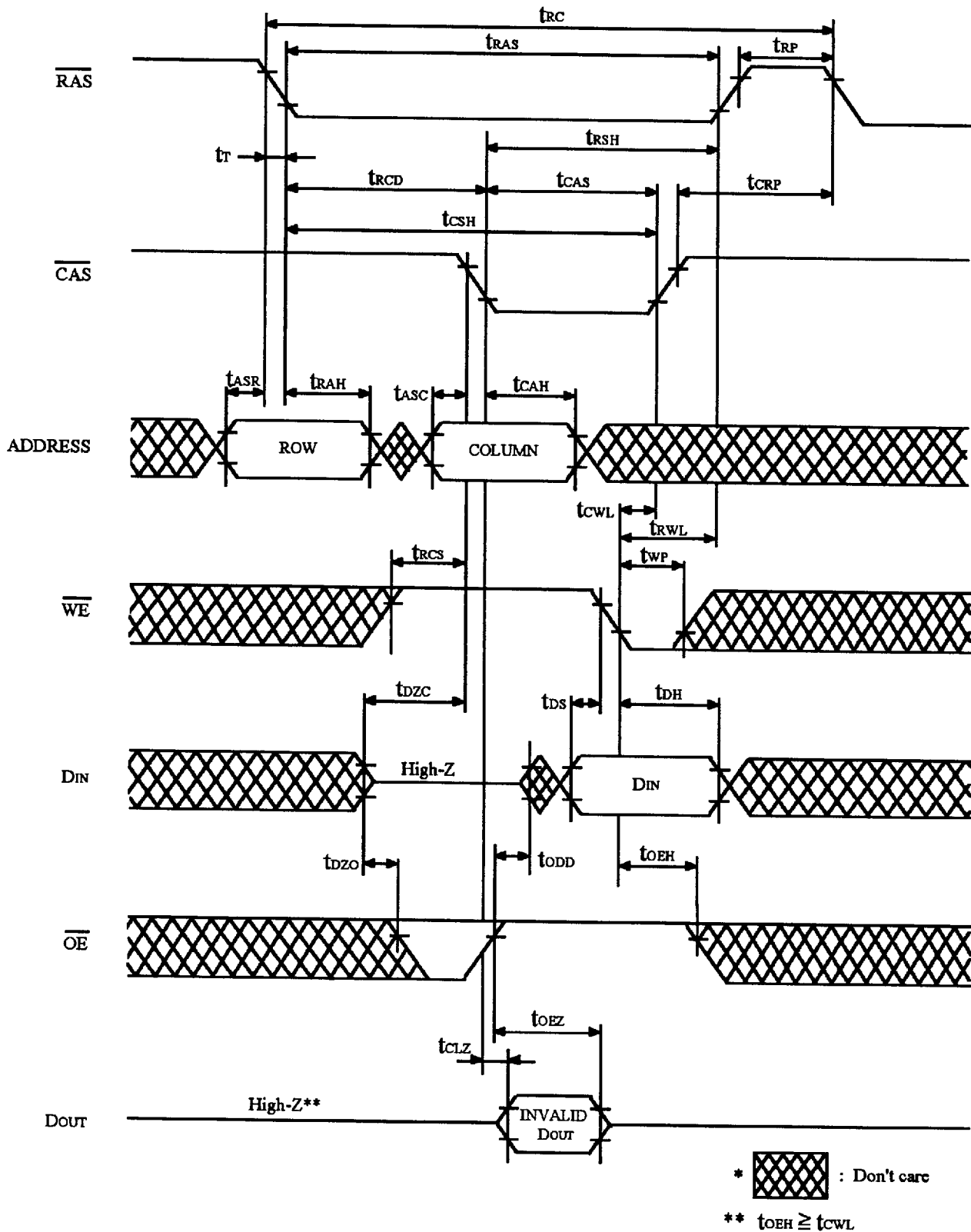


FIGURE 3. DELAYED WRITE CYCLE <sup>\*18</sup>

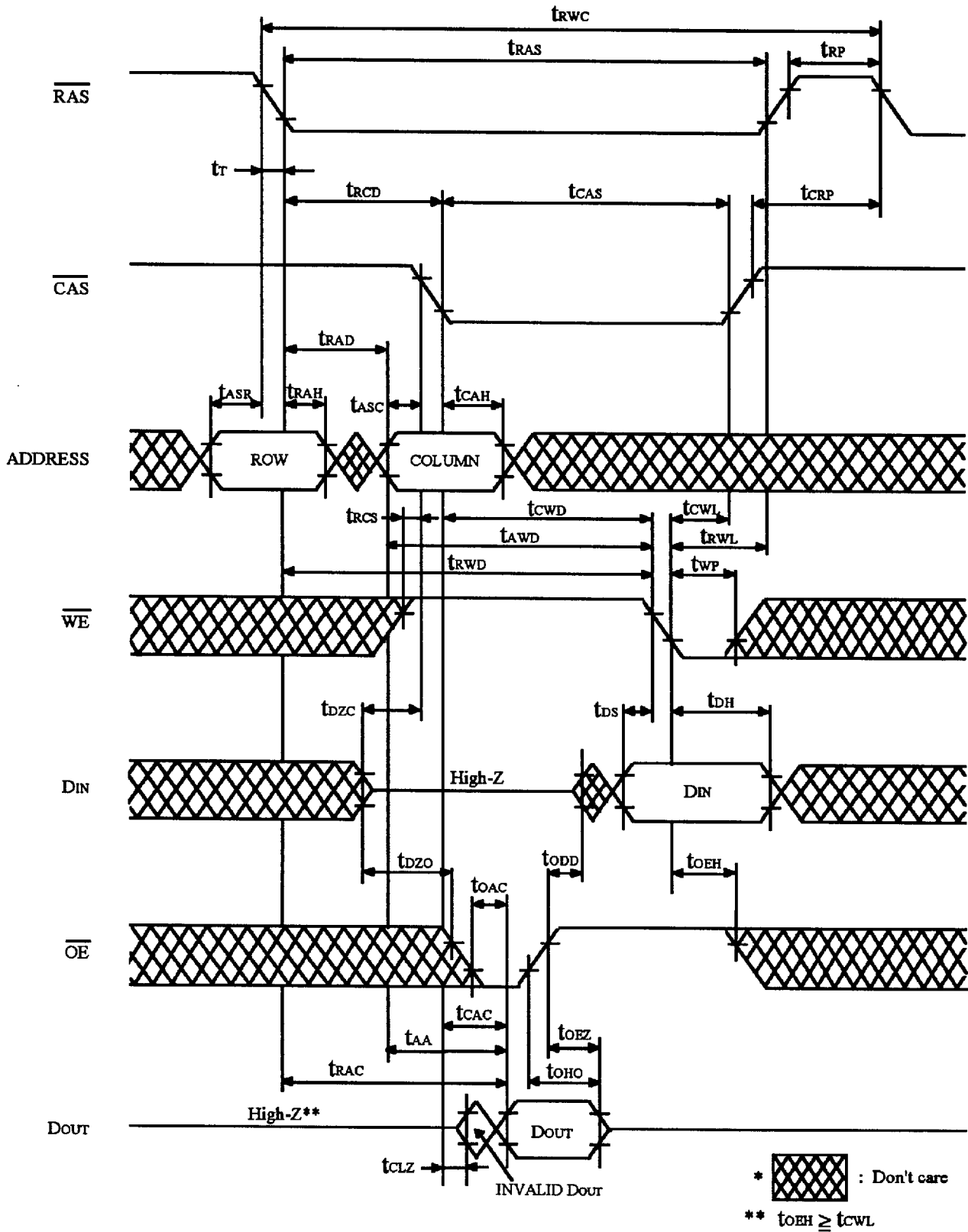
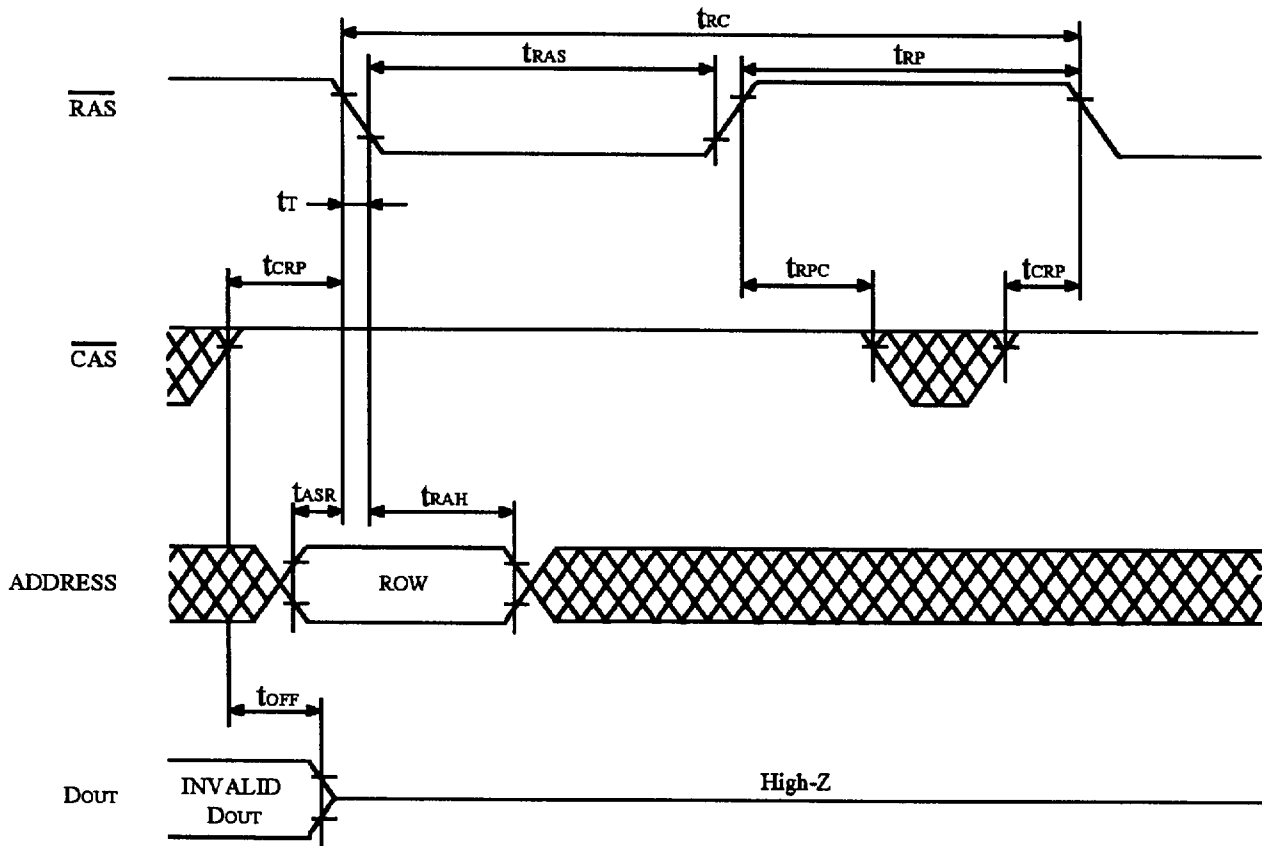


FIGURE 4. READ MODIFY WRITE CYCLE<sup>\*18</sup>



\*  : Don't care

\*\*  $\overline{OE}$ ,  $\overline{WE}$  : Don't care

\*\*\* Refresh Address :  
A0 - A10 (RA0 - RA10)

**FIGURE 5.  $\overline{RAS}$  ONLY REFRESH CYCLE**

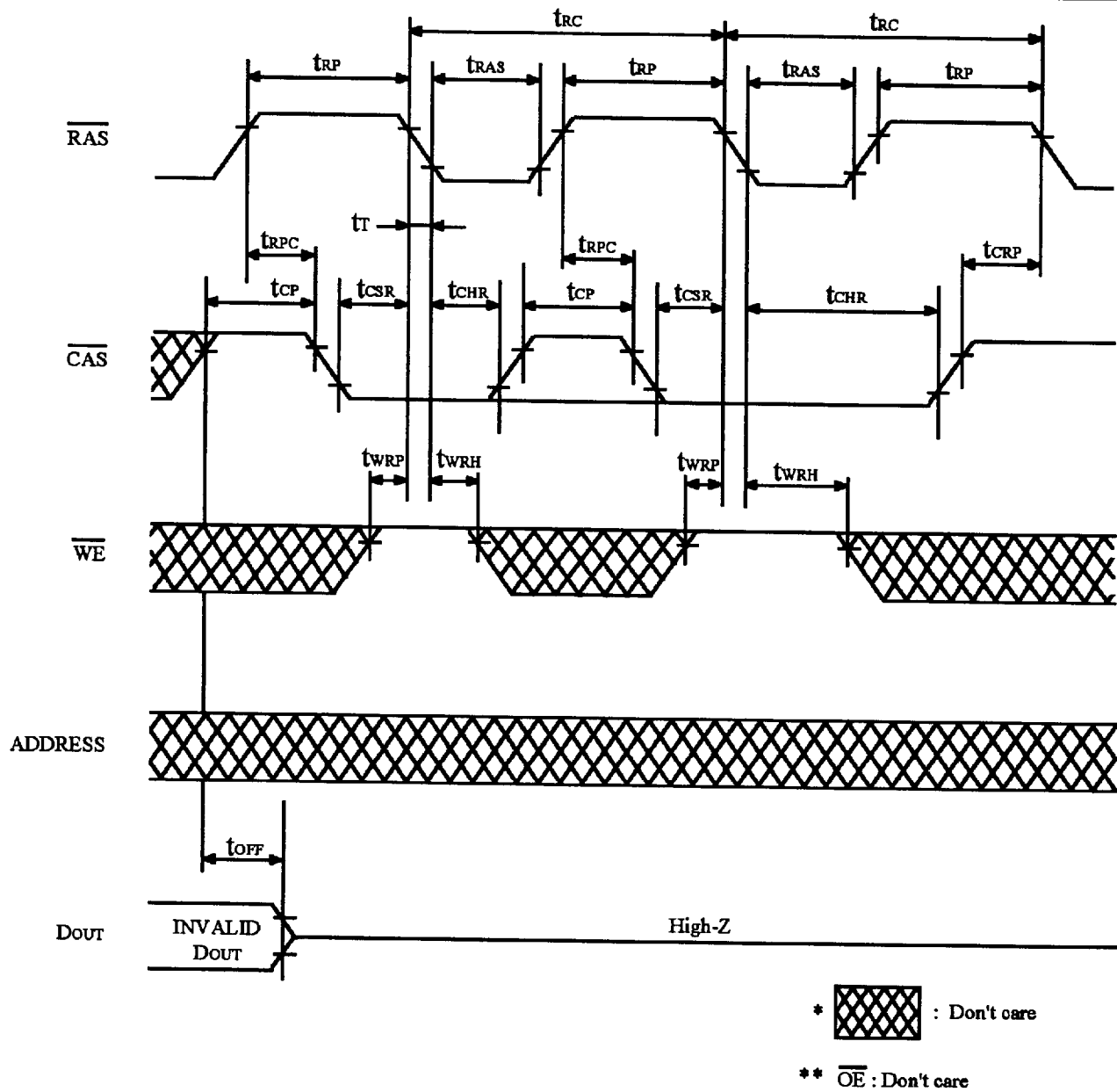
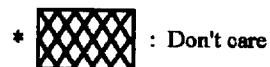
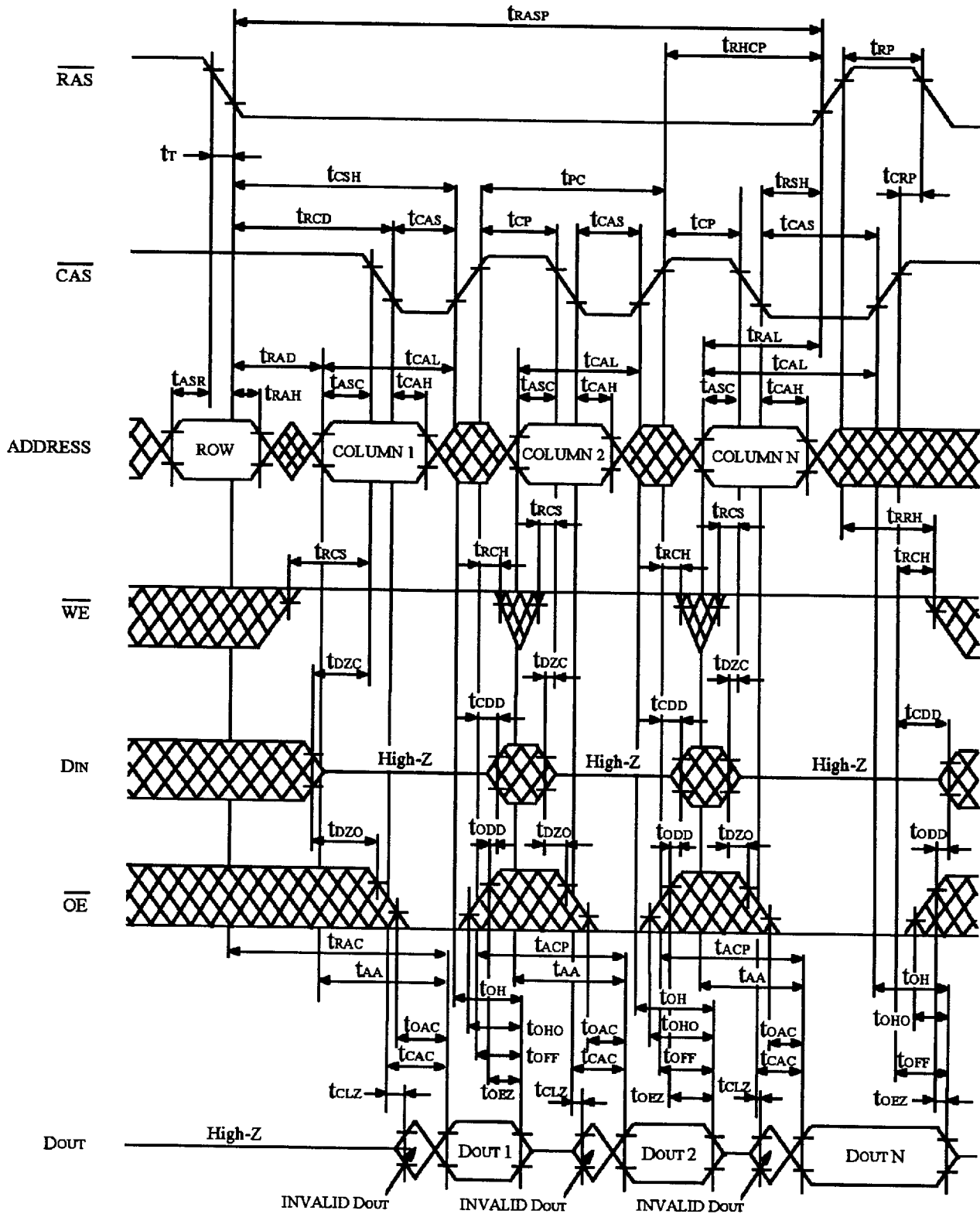


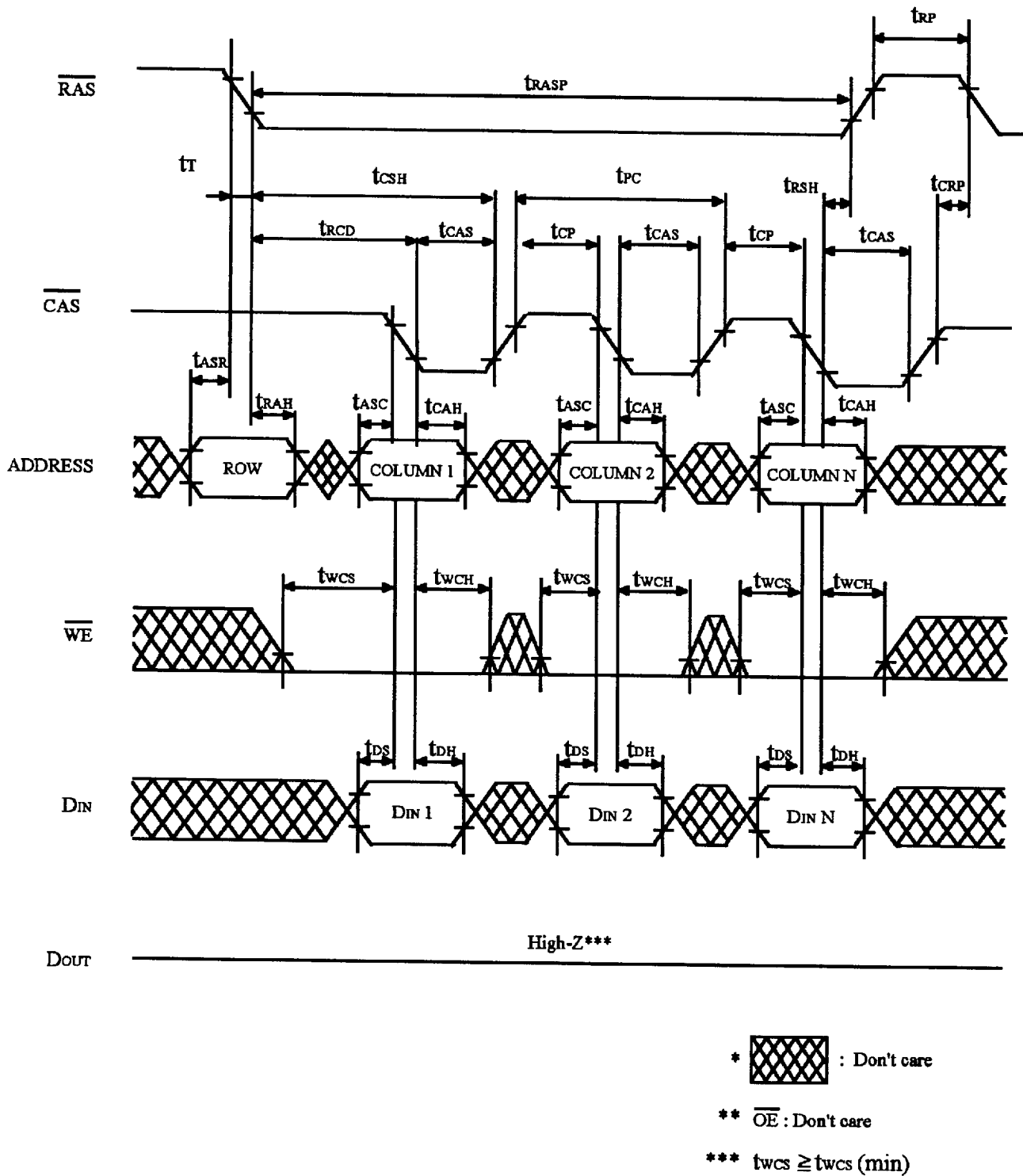
FIGURE 6.  $\overline{CAS}$  BEFORE  $\overline{RAS}$  REFRESH CYCLE



### FIGURE 7. HIDDEN REFRESH CYCLE



**FIGURE 8. FAST PAGE MODE READ CYCLE**



**FIGURE 9. FAST PAGE MODE EARLY WRITE CYCLE**



**FIGURE 10. FAST PAGE MODE DELAYED WRITE CYCLE<sup>\*18</sup>**



•18

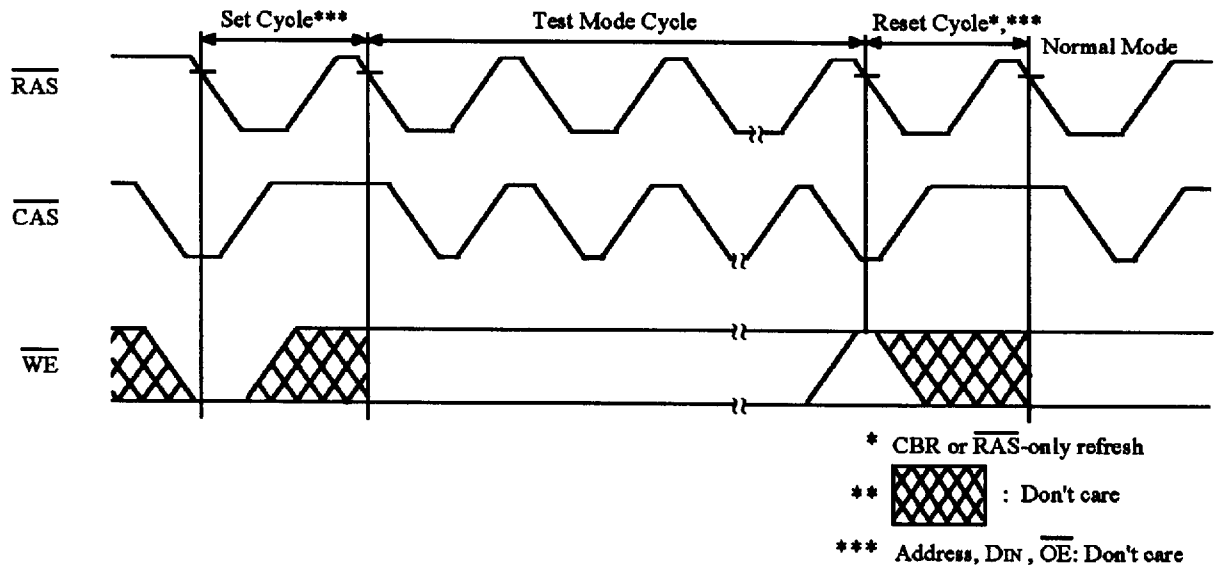


FIGURE 12. TEST MODE CYCLE \*19

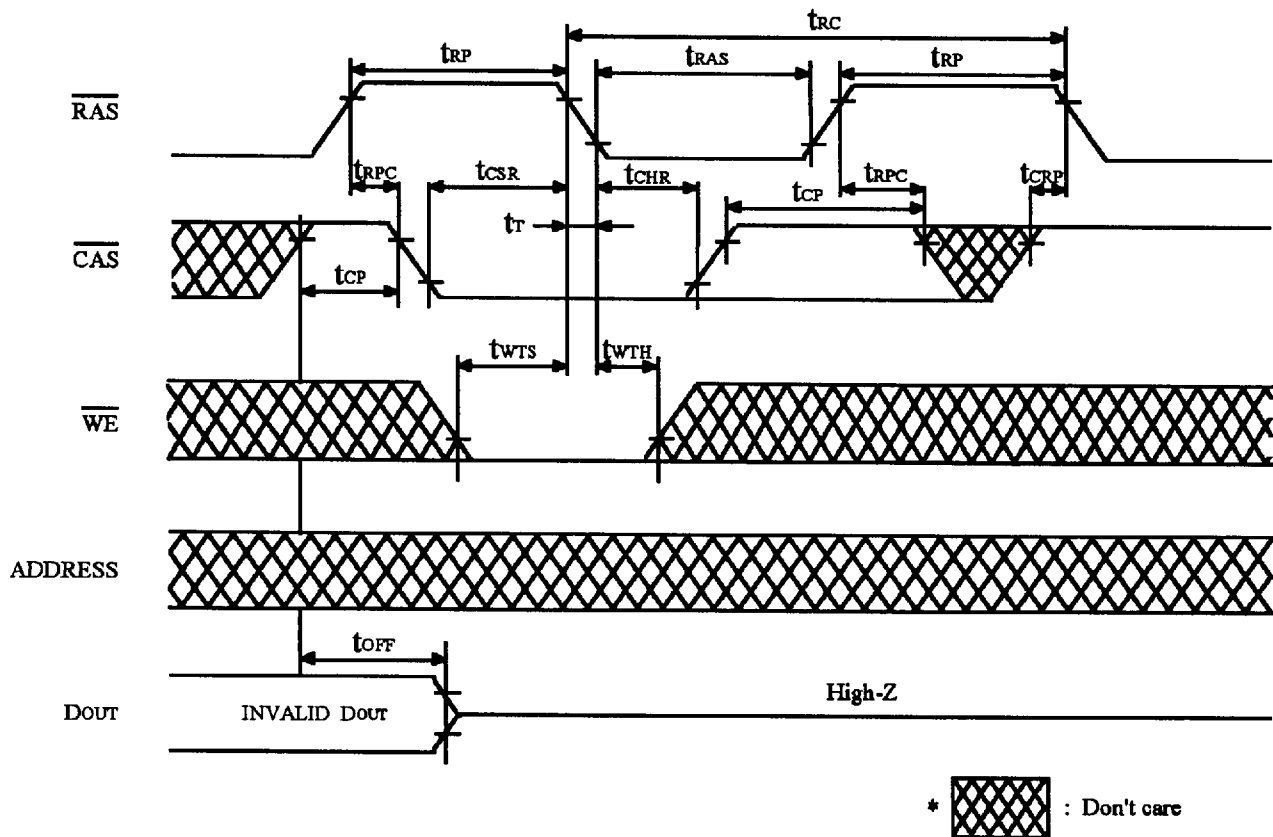


FIGURE 13. TEST MODE SET CYCLE



Test Mode Reset Cycle

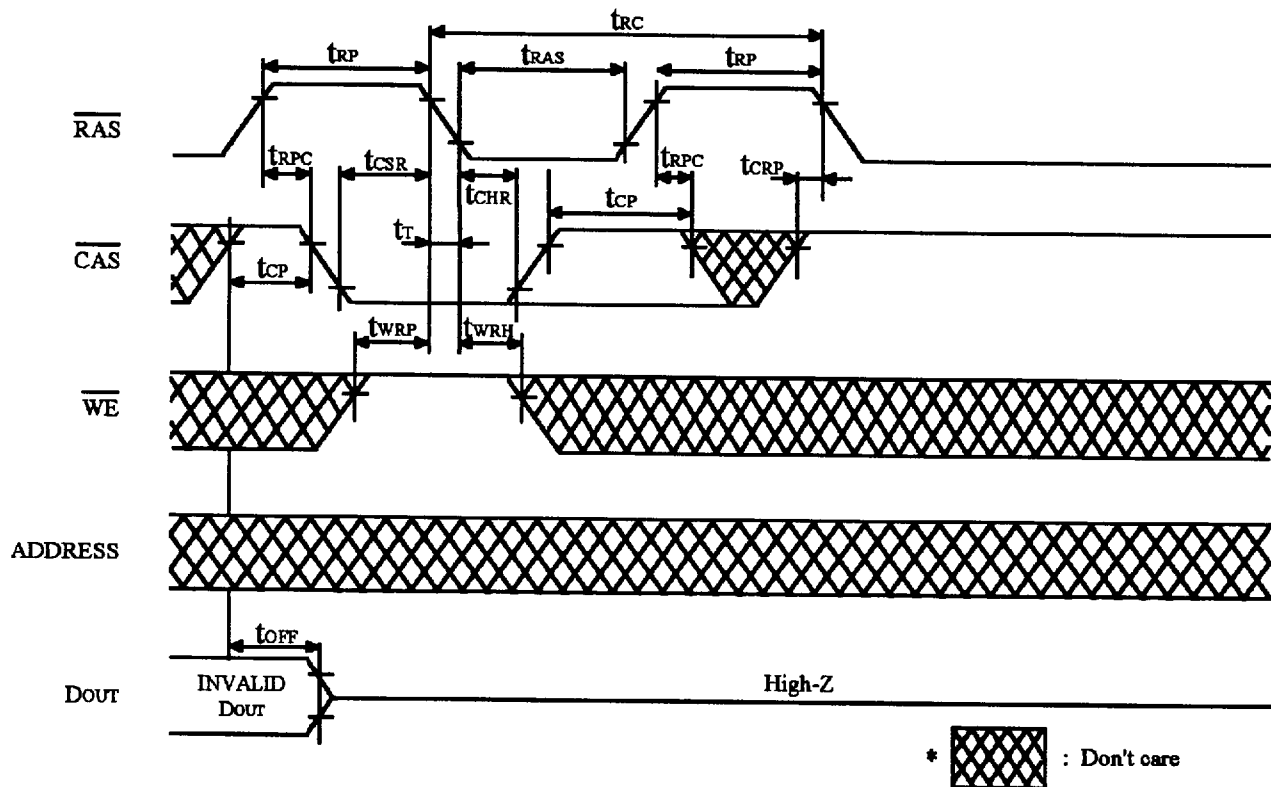


FIGURE 14.  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH CYCLE

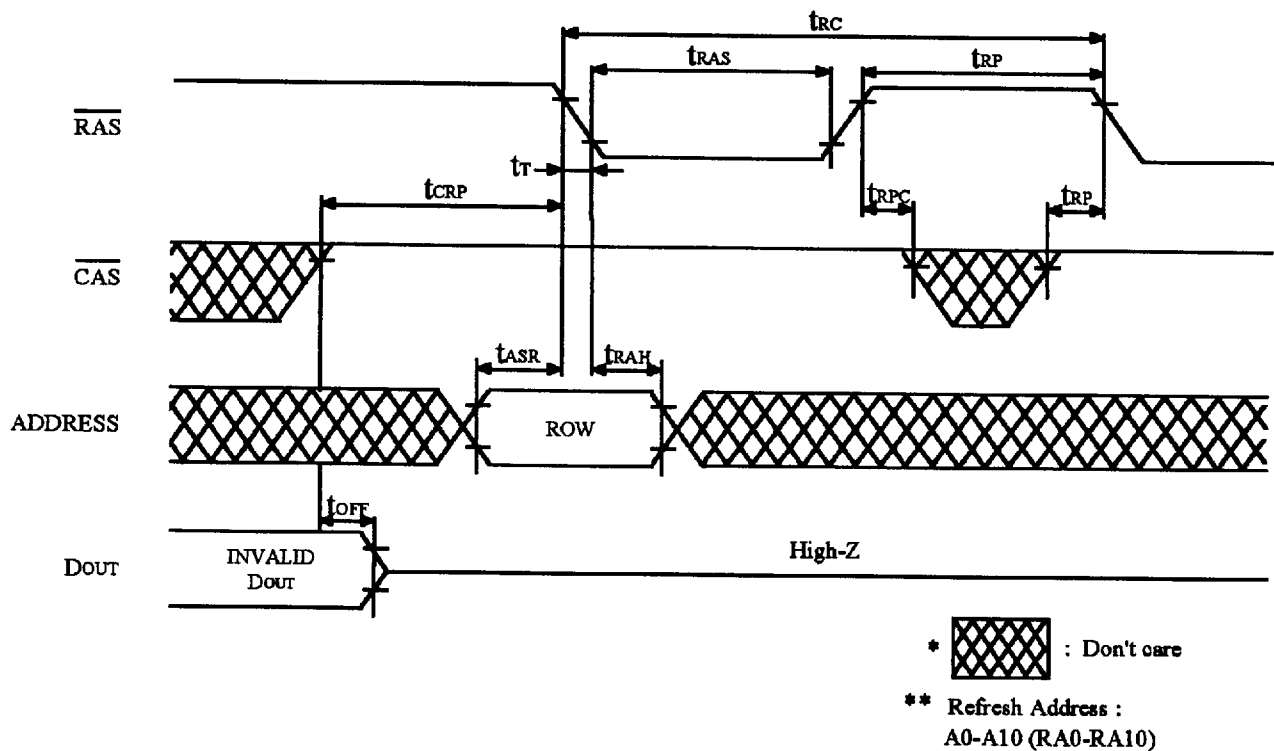


FIGURE 15.  $\overline{\text{RAS}}$  ONLY REFRESH CYCLE



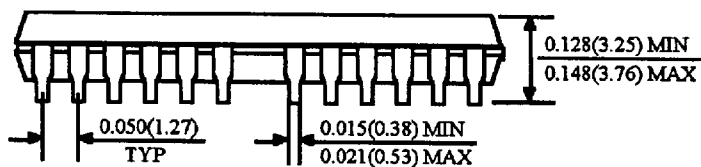
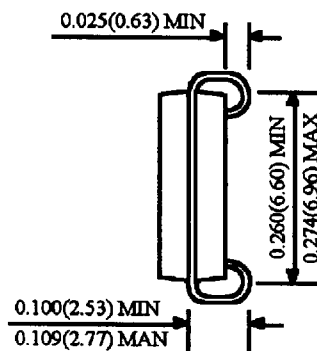
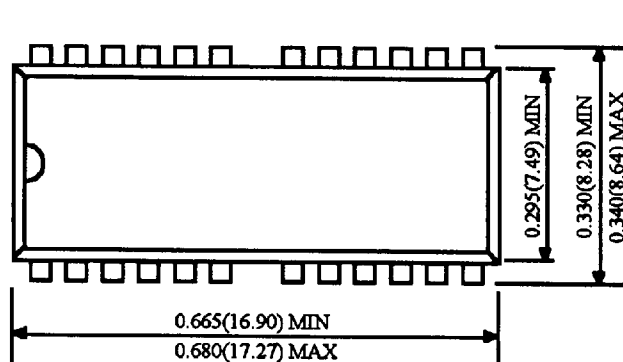
**FIGURE 16.  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER CHECK CYCLE (READ)**



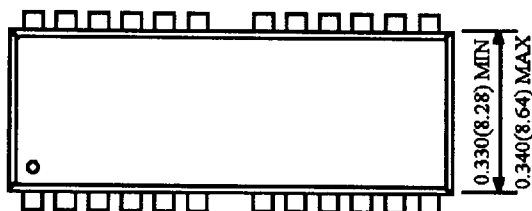
**FIGURE 17.  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  REFRESH COUNTER CHECK CYCLE (WRITE)**



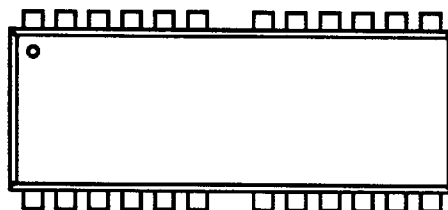
### 24 (26) SOJ



### 24 (26) TSOP(TYPE II)



NORMAL TYPE



REVERSE TYPE

