PRELIMINARY

SINGLE CHIP DIGITAL DELAY IC

■ GENERAL DESCRIPTION

NJU9701 is a single chip digital delay LSI designed for Dolby® Pro-logic or other types surround processor.

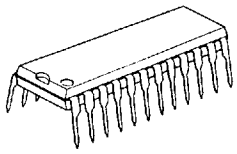
It consists of 16k SRAM, input/output filter, A/D D/A converters and control logic.

The A/D and DA converter is using a ADM (Adaptive Delta Modulation) method. Consequently, it is realized low noise and low distortion.

The delay time can select from 64 mode of 0.5ms to 32.8ms in 0.5ms step, according to the application.

Furthermore, the NJU9701 has a sleep mode, mute function, and power on initiarization function which perform low current consumption in the sleep mode, muting on/off control and power on initialization.

■ PACKAGE OUTLINE

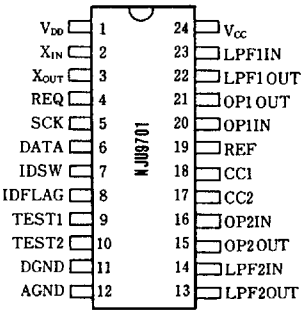


NJU9701D

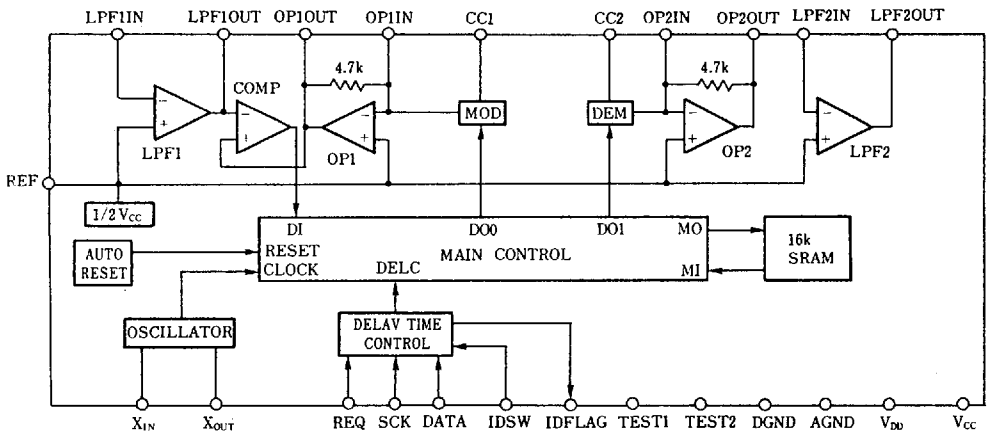
■ FEATURES

- ADM (Adaptive Delta Modulation) Method
  A/D and D/A Converter
- Low Noise and Low Distortion
  (No=95[dBV] TYP., THD=0.2[%] TYP.)
- 64 Delay Time Modes From 0.5ms To 32.8ms
  In 0.5ms step
- Low Current Consumption In Sleep Mode
- Input/Output Filter Built-in (Required External CR)
- A/D, D/A Converter Built-in (Required External CR)
- 16K SRAM (Internal)
- Power on initialization
- Oscillation Circuit
- Package Outline --------- DIP24
- C-MOS Technology

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	FUNCTIONS		
1	V_{DD}	Voltage Supply for Digital Block V_{DD} =5[V]		
11	DGND	Digital GND DGND=0[V]		
24	V_{CC}	Voltage supply for Analog Block V_{CC} =5[V]		
12	AGND	Analog GND AGND=0[V]		
19	REF	Analog Refernece Voltage REF =1/2·V_{CC}		
2	X_{IN}	Oscillator Input Terminal	Connects to 2MHz ceramic Oscillaor	
3	X_{OUT}	Oscillator Output Terminal		
4	REQ	Data Request Input Terminal		
5	SCK	Serial Data Shift Clock Input Terminal		
6	DATA	Serial Data Input Terminal		
7	IDSW	ID Switch (ID Code When Connect to the Common Bus)		
8	IDFLAG	ID Flag (Data Input Confirmation and Serial Data Output)		
18	CC1	Current Control 1 Modulator	ADM Controller	
17	CC2	Current Control 2 Demodulator		
9,10	TEST1,2	Test Terminal (Normally Connects to the GND)		
23	LPF1IN	Lowpass Filter 1 Input	Input Side	Constitute a Lowpass Filter with external C and R.
22	LPF1OUT	Lowpass Filter 1 Output		
14	LPF2IN	Lowpass Filter 2 Input	Output Side	
13	LPF2OUT	Lowpass Filter 2 Output		
20	OP1IN	OP-AMP 1 Input	Input Side	Constitute a Integrator with external C.
21	OP1OUT	OP-AMP 1 Output		
16	OP2IN	OP=AMP 2 Input	Output Side	
15	OP2OUT	OP-AMP 2 Output		

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■ FUNCTION DESCRIPTION

The sampling frequency (fs) is 500KHz when master clock frequency is 2MHz.

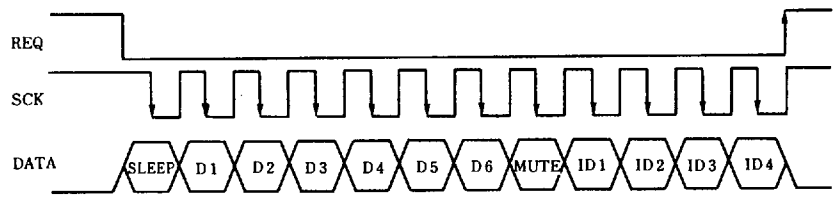
1) Data Format and Setting

The delay time is set by serial data.

The serial data is written into the NJU9701 sincronized by falling edge of shift clock(SCK) and the last 12 bit is effective before the data request(REQ) rising edge.

The time chart of serial data input is shown as follows.

In order to avoid the shock noise output at the delay time setting, mute function using is recommended.



2) Sleep Mode Setting

The sleep mode can be set by writing the code "1"(H level) to the Sleep bit of the serial data.

The sleep mode performs ① output muting, ② stop the internal clock, ③ stop the memory operation and put a low current consumption mode. Normally, this Sleep bit must be "0" (L level).

In order to avoid the shock noise output when the sleep mode released, mute function using is recommended.

SLEEP	MODE	F U N C T I O N S
0	NORMAL	Normal operation
1	SLEEP	① Output Muting ② Stop the Internal Clock ③ Stop the Memory Operation

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3) Delay Time Setting

64 kind of delay time from 0.5ms to 32.8ms in 0.5ms is set by D1 to D6 of the serial data.

D6	D5	D4	D3	D2	D1	Delay T.
0	0	0	0	0	0	0.5
					1	1.0
				1	0	1.5
					1	2.0
			1	0	0	2.6
					1	3.1
				1	0	3.6
					1	4.1
		1	0	0	0	4.6
					1	5.1
				1	0	5.6
					1	6.1
			1	0	0	6.7
					1	7.2
				1	0	7.7
					1	8.2
	1	0	0	0	0	8.7
					1	9.2
				1	0	9.7
					1	10.2
			1	0	0	10.8
					1	11.3
				1	0	11.8
					1	12.3
		1	0	0	0	12.8
					1	13.3
				1	0	13.8
					1	14.3
			1	0	0	14.8
					1	15.4
				1	0	15.9
					1	16.4

D6	D5	D4	D3	D2	D1	Delay T.
1	0	0	0	0	0	16.9
					1	17.4
				1	0	17.9
					1	18.4
			1	0	0	18.9
					1	19.5
				1	0	20.0
					1	20.5
		1	0	0	0	21.0
					1	21.5
				1	0	22.0
					1	22.5
			1	0	0	23.0
					1	23.6
				1	0	24.1
					1	24.6
	1	0	0	0	0	25.1
					1	25.6
				1	0	26.1
					1	26.6
			1	0	0	27.1
					1	27.6
				1	0	28.2
					1	28.7
		1	0	0	0	29.2
					1	29.7
				1	0	30.2
					1	30.7
			1	0	0	31.2
					1	31.7
				1	0	32.3
					1	32.8

UNIT (ms)

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4) Mute Setting

The mute mode can be set by writing the code "1"(H level) to the Mute bit of the serial data. Normally, this Mute bit must be "0" (L level).

MUTE	MODE	F U N C T I O N S
0	NORMAL	Normal Operation
1	MUTE	Output Muting

5) ID Code Setting

The access from the controller(CPU) is recognized by the ID code input. It is useful when the NJU9701 connect the common bus togather with other LSI(s). The IDSW can select the prefixed ID code. If the other LSI using the ID code system and setting the same code already, please select other code by using this SW(IDSW).

ID Code Table

CONDITIONS	Code Selection Term.	ID Code			
	IDSW	ID1	ID2	ID3	ID4
1	0	0	0	1	0
2	1	0	0	1	1

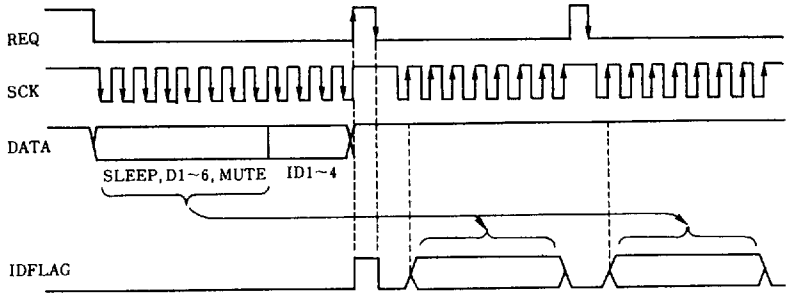
Note) ID code input except mentiond above, the NJU9701 can not be receive any data. In this case, the NJU9701 stil keeping the condition input before.

6) IDFLAG

IDFLAG is a terminal to check the setting of delay time and the setting conditions.

When the serial data is received by the NJU9701, the IDFLAG terminal output "H" level for controller(CPU)'s confermation.

After serial data writting, except the ID code (Sleep, D1 to D6, and Mute) can read out for checking. When the read out, ① set the "L" level of the request signal(REQ), ②input the clock signal are required. The data is output syncronized by the rising edge of the clock signal. The ID code can not read out even if over 8 clock input.



7) Reset Function

NJU9701 performs power-on-initialization when turn on the power. After 120ms pased the turn on at the condition of V_{CC}=5V, Capacitor connecting to the REF terminal=47μF, it is released automatically. The 20.0ms delay time is set by the power-on-initialization.

■ ABSOLUTE MAXIMUN RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	6.5	V
	V_{CC}	6.5	
Operating Current	I_{CC}	100	mA
Power Dissipation	P_D	500	mW
Operating Temperature Range	Topr	-20 ~ + 75	℃
Storage Temperature Range	Tstg	-40 ~ +125	℃

Note) V_{DD} should be rise up before V_{CC} or same time. Otherwise power-on-initialization may not be operate corectly.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage	V_{DD}		4.5	5.0	5.5	V
	V_{CC}		4.5	5.0	5.5	V
Clock Frequency	f_{ck}			2.0		MHz
Input Voltage "H"	V_{IH}		$0.7V_{DD}$	—	V_{DD}	V
Input Voltage "L"	V_{IL}		0	—	$0.3V_{DD}$	V

■ ELECTRICAL CHARACTERISTICS

(V_{DD}=V_{CC}=5V, f=1kHz, Vo=200mVrms, Ta=25℃)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current	I_{CC}	No Signal		30		mA
Voltage Gain	Gv	R_L=47kΩ		-0.5		dB
Max. Output Voltage	Vo_{max}	THD=10%		1		Vrms
Output Distortion	THD	30kHz LPF		0.2		%
Output Noise Voltage	No	DIN-AUDIO		-95		dBV
Supply Voltage Rejc. Ratio	SVRR	V_{CC}=-20dBV, f=100Hz		-40		dB
Frequency Characteristics	f	-3dB, Vo=100mVrms		7		kHz

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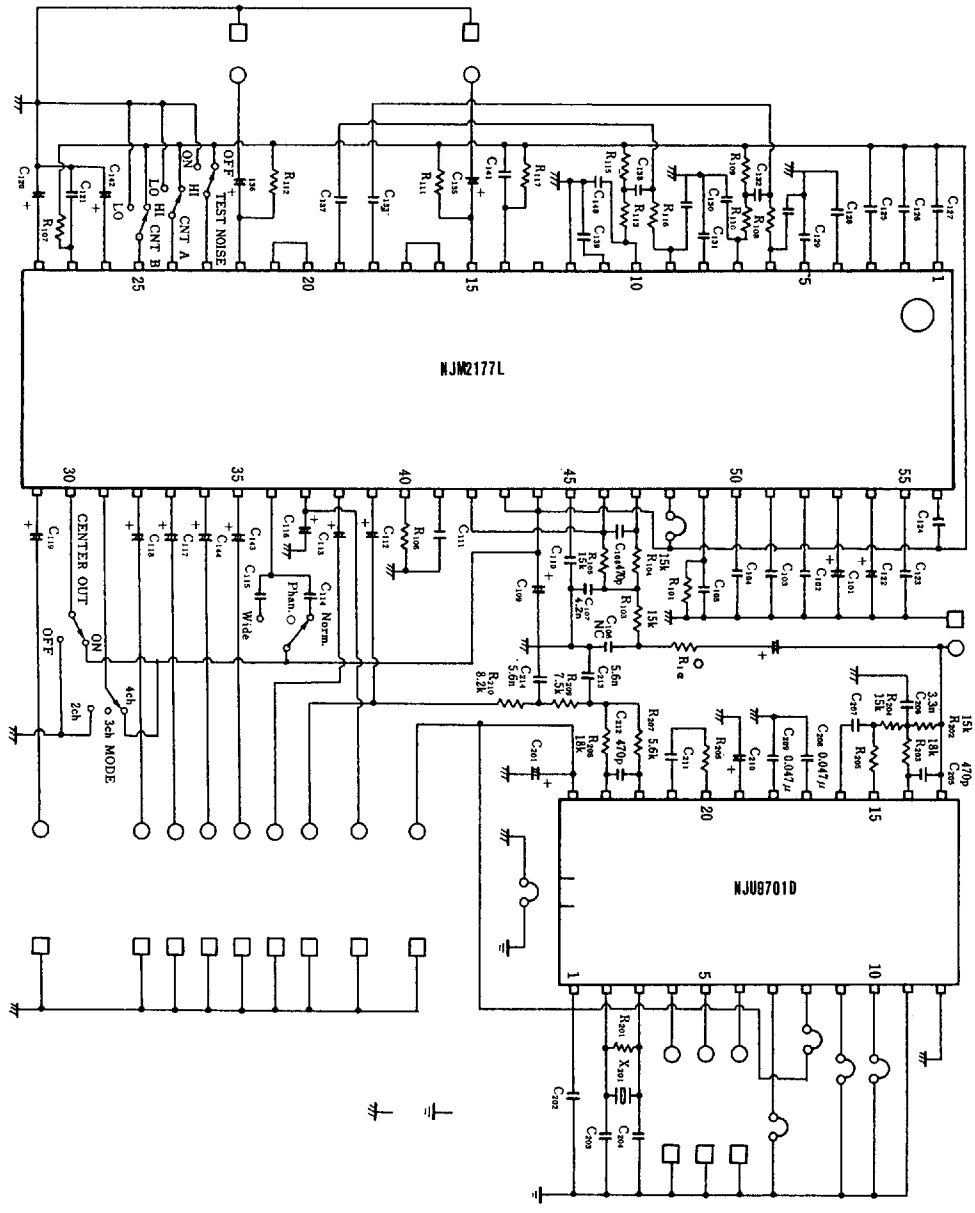
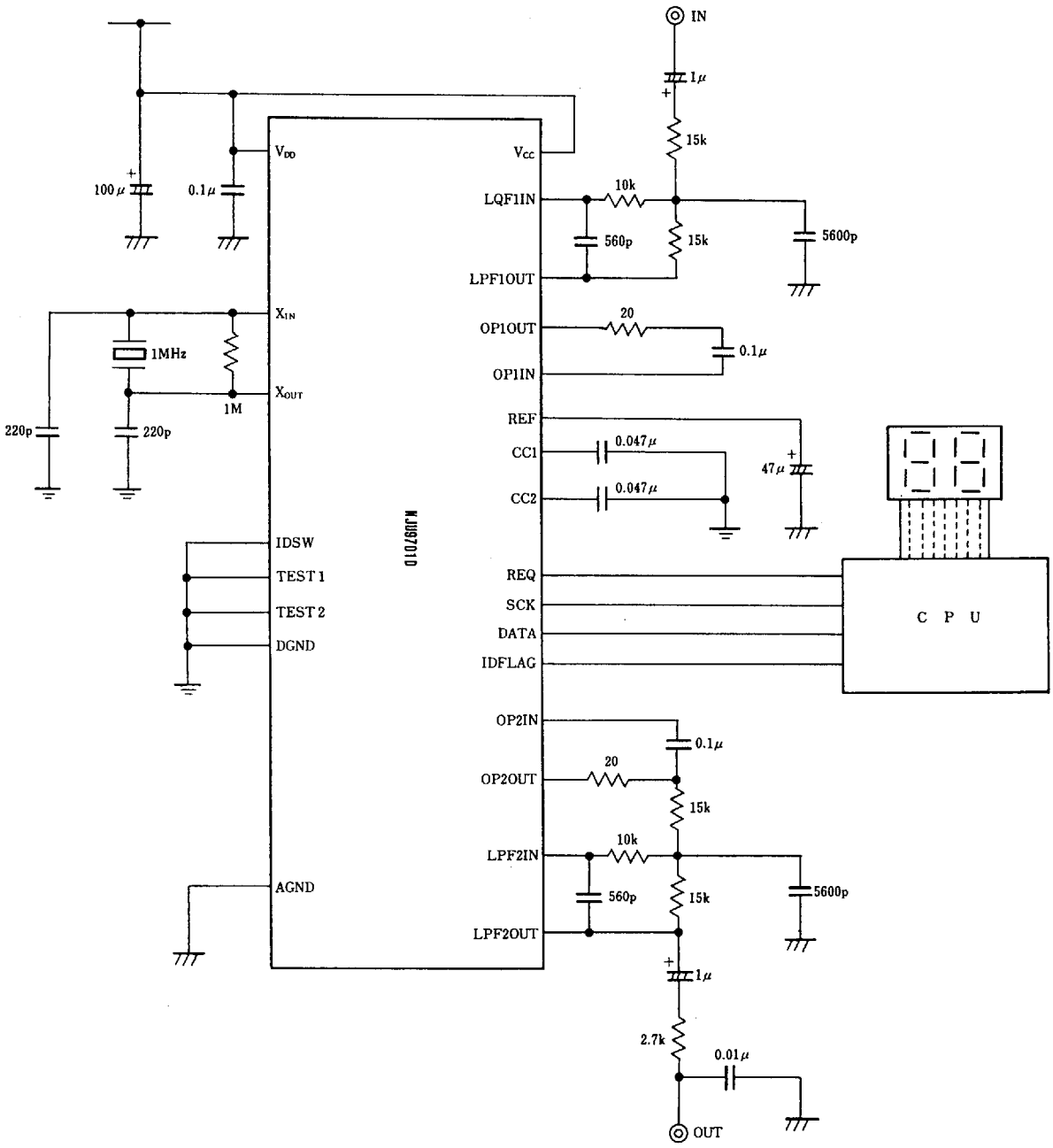
■ APPLICATION CIRCUIT(1) (Combined with NJM2177)



■ APPLICATION CIRCUIT(2)



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