

NLB6222

NEL
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Dual T Flip-flop with Set and Reset

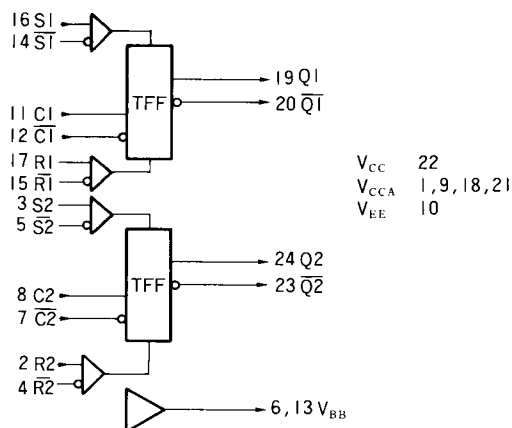
Description

The NLB6222 is an ultra high-speed monolithic dual T Flip-Flop with separate direct compliment set (S) and reset (R).

Features

- Typical : clock rate up to 4GHz.
- Internal pull down resisters on input pins (S_n, R_n, C_n) to maintain logic LOW level with the pins left open
- Internal pull down resisters on input pins ($\overline{S}_n, \overline{R}_n, \overline{C}_n$) to maintain logic HIGH level with the pins left open
- ELC100K compatible I/O levels
- Differential output

Logic Symbol

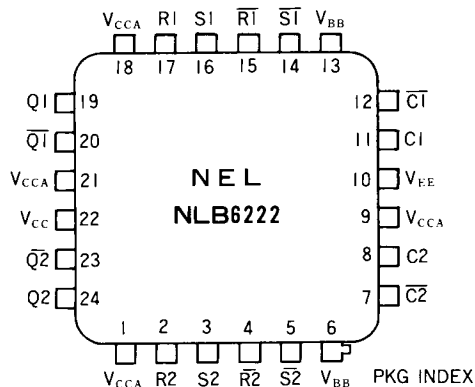


Truth table

Input				Output	
S	R	C	$\overline{C}$	Q	$\overline{Q}$
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	X	X
L	L	J	L	$\overline{Q}_{n-1}$	Q_{n-1}

H : High voltage level
L : Low voltage level
X : Arbitrary
J : L to H transition
L : H to L transition

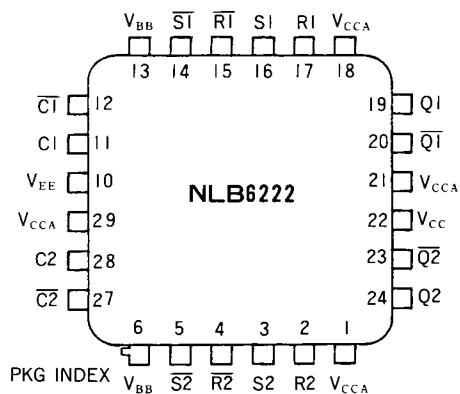
Pin Assignment Top View (Ceramic)



Pin Name

$S_n, \overline{S}_n$ Direct set inputs
 $R_n, \overline{R}_n$ Direct reset inputs
 $C_n, \overline{C}_n$ Clock inputs
(Positive edge trigger)
 V_{BB} Reference voltage outputs
 V_{CC} Circuit GND
 V_{CCA} Circuit GND for outputs
 V_{EE} -4.5V

Back View (Metal Cap)



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DC Characteristics

$V_{EE} = -4.5V \pm 0.3V$, $V_{CC} = GND$, $V_{TT} = -2V$
 $T_C = 0^\circ C$ to $+85^\circ C$

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Power supply current	I_{EE}	80	115	155	mA

AC Characteristics

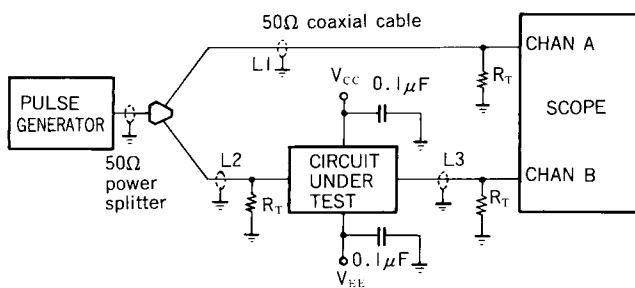
$V_{EE} = -4.5V \pm 0.3V$, $V_{CC} = GND$, $V_{TT} = -2V$
 $T_C = 0^\circ C$ to $+85^\circ C$, $R_T = 50\Omega$ to V_{TT}

Characteristics	Symbol	Input	Output	Measuring condition	Min.	Typ.	Max.	Unit
Propagation delay time	t _{PLH}	Cn	Qn			600	790	ps
	t _{PHL}					600	790	
	t _{PLH}	Sn				660	870	
	t _{PHL}					660	870	
	t _{PLH}	Rn				680	900	
	t _{PHL}					680	900	
Release time	t _R	Sn, Cn			230	170		
		Rn, Cn			230	170		
Minimum pulse width	t _{PW}	Sn			330	250		
		Rn			330	250		
Maximum operating frequency	f _{max}	Cn					2.8	4.0
Rise time	t _r	Cn	Qn	20 to 80 %		150	200	ps
Fall time	t _f					140	190	

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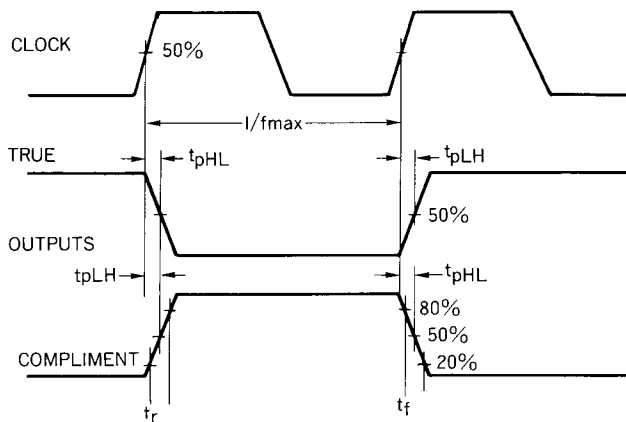
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AC Test Circuit



Notes) $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$.
 $L1 = L2 + L3$
 $R_T = 50\Omega$ terminator.
 Unused complement output is loaded with 50Ω to GND.
 C_L = Fixture and stray capacitance ≤ 2 pF.

Propagation Delay and Transition Times



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Dual T Flip-Flop with Set and Reset

Propagation Delay (Set/Reset) and Release Times

