National Semiconductor

PRELIMINARY

NM100492/NM4492 2k x 9 Advanced Self-Timed SRAM

Features

- Extremely fast access time
  - 5 ns Max (NM4492)
  - 7 ns Max (NM100492)
- Power supply: −5.2V ± 5% (NM4492)
- Power supply: −4.2V to −4.8V (NM100492)
- Completely self-timed read and write cycle
- On-chip input and output registers
- Modest power consumption—2W at 7 ns, <1.5W at 100 MHz
- On-chip parity checking—with odd address parity mode pin
- Clock enable input simplifies pipeline control
- Scan diagnostics supported by on-chip scan registers
- High speed ceramic flatpak
- High speed TapePak™ package under development
- I/O compatible with F100k standard

General Description

The NM100492/NM4492 is an extremely high performance 2k x 9 SRAM. It is the first of a family of similar 9-bit wide SRAMs designed specifically for very high speed ECL computer applications such as register files, writable control stores, cache RAMs, cache tag RAMs, and address translation lookaside buffers. The NM100492/NM4492 offers several features which are very desirable in such applications.

ADVANCED SELF-TIMED ARCHITECTURE

This advanced self-timed RAM simplifies the system design of extremely fast memory arrays by minimizing the impact of timing skews on the cycle time of the memory array. All input signals (address, data and control signals) are registered on-chip by a transition of the clock. By registering all inputs with minimal setup and hold times (setup + hold = 2 ns) the troublesome skews inherent with traditional static RAM timing requirements are significantly reduced. With skew problems minimized, very short cycle times become practical. Output registers (self-timed on-chip) hold output data valid for an extended portion of the cycle easing system read timing requirements.

HIDDEN WRITE CYCLE MODE

The hidden write cycle timing allows relaxed data bus timing. This will often ease system setup and hold requirements for the data output bus. Hidden write timing is essentially a technique for interleaving reads and writes. This advanced self-timed SRAM supports hidden write timing more conveniently in the system than first generation self-timed SRAM's, due to the unique control signal functions defined for write enable ($\overline{W}$) and chip select ($\overline{S}$). By keeping the output register active (with the last read data) during a write cycle, this device greatly simplifies the timing of interleaved memory architectures. This mode may be very useful in cache and register file applications, where multiple sources and/or destinations may be interleaved within each machine cycle.

PARITY CHECKING

The device also offers several convenient features which may be useful in specific applications. One such feature is the on-chip parity checking function. For systems where parity checking is desirable this device will check for odd parity on the 9-bit data input field, and will check for either even or odd parity (depending on the polarity of the parity mode pin −PM) on the 11-bit address field combined with the address parity input. Odd parity is met when the number of highs in the field is odd. Address parity checking can be conveniently disabled if desired, allowing data field only parity checking. If either the data or address demonstrates a parity error, then the parity error output flag is set. The polarity of the error output flag facilitates emitter dot ORing several error outputs for minimal delay. The parity checking feature is benign in the sense that if parity checking is not desired, the output can simply be ignored without detrimental effects to normal operation.

SERIAL SCAN DIAGNOSTICS REGISTERS

Another convenient feature provided on-chip is the scan diagnostics register. For system designs where scan diagnostics are included, this device allows observing the state of the input registers (scan out) and forcing the state of the input and output registers (scan in). For writable control store applications the control store can be loaded via the serial channel (scan in), simplifying circuit board layout by eliminating the wide parallel data input bus structure. For systems where scan diagnostics are not desired, the scan enable input can simply be left open allowing the on-chip pulldown device to disable scan functions and provide normal SRAM functionality.

PIPELINE CONTROL

Yet a third convenient feature is the clock enable input. This control simplifies starting and stopping pipeline operations in pipelined systems. It reduces, and may eliminate, the need to gate the clock signal external to the RAM. This feature is also benign since the on-chip pulldown device will ensure normal operation if the clock enable is not used.

MODEST POWER CONSUMPTION

Modest power consumption is achieved without compromising device speed through very unique and innovative circuit design techniques (patents applied for). Power consumption is predominately dependent on clock frequency (1/cycle time) allowing a reduction in power at lower operating frequency.

F100K COMPATIBLE I/O

The device is I/O compatible with standard temperature compensated F100K ECL logic, allowing trouble free interfacing in high performance ECL systems.