National Semiconductor

NM100504/NM5104 256k BiCMOS SRAM 64k x 4

General Description

The NM5104 and NM100504 are 262,144-bit fully static, asynchronous, random access memories organized as 65,536 words by 4 bits. The devices are based on National's advanced one micron BiCMOS III process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of high performance technology and speed optimized circuit designs results in a very high speed memory device.

The NM5104 operates with a supply voltage of −5.2V ±5%, yet the input and output voltage levels are temperature compensated 100K ECL compatible. The NM100504 operates with a −4.2V to −4.8V supply voltage.

Reading the memory is accomplished by pulling the chip select ($\overline{S}$) pin LOW while the write enable ($\overline{W}$) pin remains HIGH allowing the memory contents to be displayed on the output pins (Q0–Q3). The output pins will remain inactive (LOW) if either the chip select ($\overline{S}$) pin is HIGH or the write enable ($\overline{W}$) pin is LOW.

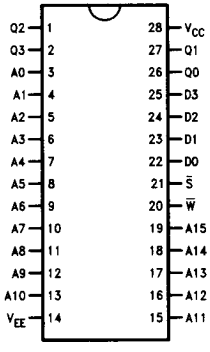
Writing to the device is accomplished by having the chip select ($\overline{S}$) and the write enable ($\overline{W}$) pins LOW. Data on the input pins will then be written into the memory address specified on the address pins (A0–A15).

Features

- Speed Grades: 12 ns/15 ns (NM5104)
- Speed Grades: 15 ns/18 ns (NM100504)
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skews
- Temperature compensated F100K ECL I/O
- Power supply −5.2V to ±5% (NM5104)
- Power supply −4.2V to −4.8V (NM100504)
- Low power dissipation <1.4W @ 50 MHz
- Soft error rate less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS III process technology
- Over 200 mA latch-up immunity
- Low inductance, high density 28-pin flatpak and 28-pin ceramic DIP

Connection Diagrams

28-Pin Ceramic DIP



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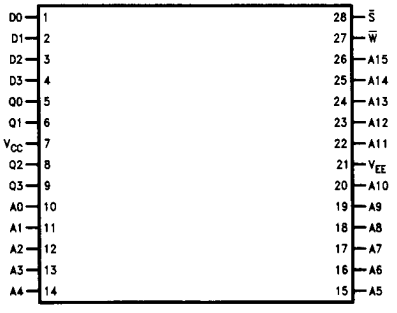
Top View

28-Pin Ceramic Flatpak (30 Mil Lead Pitch)



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Top View

Pin Names

A0–A15	Address Inputs
$\overline{S}$	Chip Select
$\overline{W}$	Write Enable
Q0–Q3	Data Out
D0–D3	Data In
V_{CC}	Ground
V_{EE}	Power

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Absolute Maximum Ratings

above which useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Static Discharge Voltage (Per MIL-STD 883)	>2001V
Maximum Junction Temperature (T_J)	+150°C
Output Current (DC Output HIGH)	−50 mA
Latch-Up Current	>200 mA

These devices contain circuitry to protect the inputs against damage to due to high static voltages or electric fields however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit.

AC Test Conditions

Input Pulse Levels	*Figure 1*
Input Rise and Fall times	0.7 ns
Output Timing Reference Levels	50% of Input
AC Test Circuit	*Figure 2*

Capacitance Tested by Sample Basis

Symbol	Parameter	Max	Units
C_{IN}	Input Pin Capacitance	5.0	pF
C_{OUT}	Output Pin Capacitance	8.0	pF

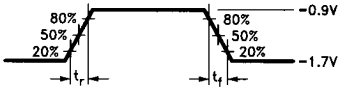
Operating Voltage

Device	Voltage
NM5104	V_{EE} = −5.2V ±5%
NM100504	V_{EE} = −4.2V to −4.8V

DC Electrical Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output HIGH Voltage	Loading with 50Ω to −2.0V	−1025	−880	mV
V_{OL}	Output LOW Voltage		−1810	−1620	mV
V_{IH}	Input HIGH Voltage		−1165	−880	mV
V_{IL}	Input LOW Voltage		−1810	−1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IH(Min)}$		50	μA
I_{IL}	Input LOW Current	$V_{IN} = V_{IL(Max)}$	−50	50	μA
I_{EE}	Power Supply Current	f_o = 50 MHz	−250		mA

All voltages are referenced to V_{CC} pin = 0V.



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t_R = Rise Time
t_F = Fall Time
50% = Timing Reference Levels

FIGURE 1. Input Levels

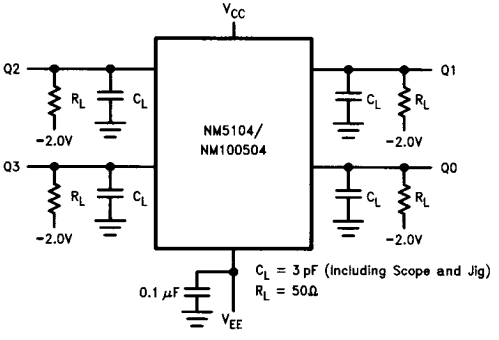

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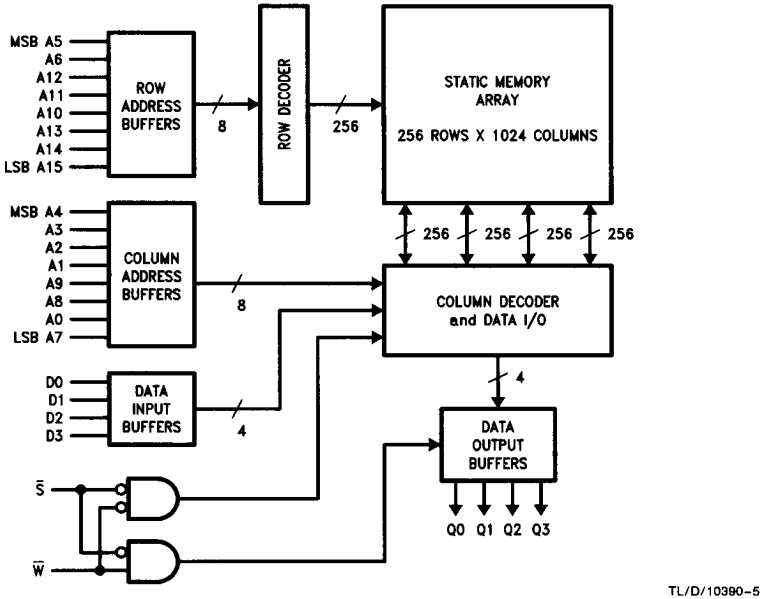
FIGURE 2. AC Test Circuit

Truth Table

$\overline{S}$	$\overline{W}$	D	Q	Mode
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Q	Read

Logic Diagram



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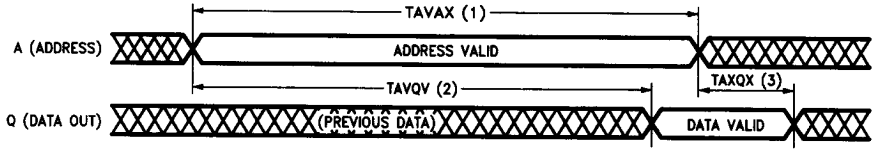
Read Cycles

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	12 ns Device		15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	Min	Max	
1	TAVAX	TRC	Address Valid to Address Invalid	12		15		18		ns
2	TAVQV	TAA	Address Valid to Output Valid		12		15		18	ns
3	TAXQX	TOH	Address Invalid to Output Invalid	3		3		3		ns
4	TSLSH	TRC	Chip Select LOW to Chip Select HIGH	7		7		7		ns
5	TSLQV	TACS	Chip Select LOW to Output Valid		5		5		5	ns
6	TSHQL	TRCS	Chip Select HIGH to Output LOW		4		4		4	ns

Read Cycle 1

Where $\overline{S}$ is active prior to within TAVQV-TSLQV after address valid.



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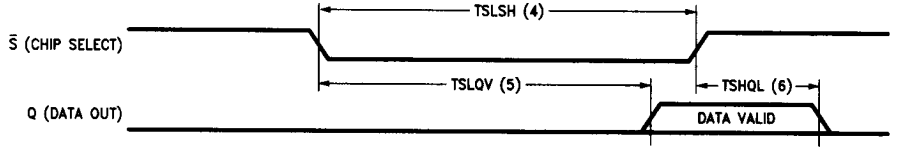
Read Cycle 2

Where address is valid a minimum of TAVQV-TSLQV prior to $\overline{S}$ becoming active.



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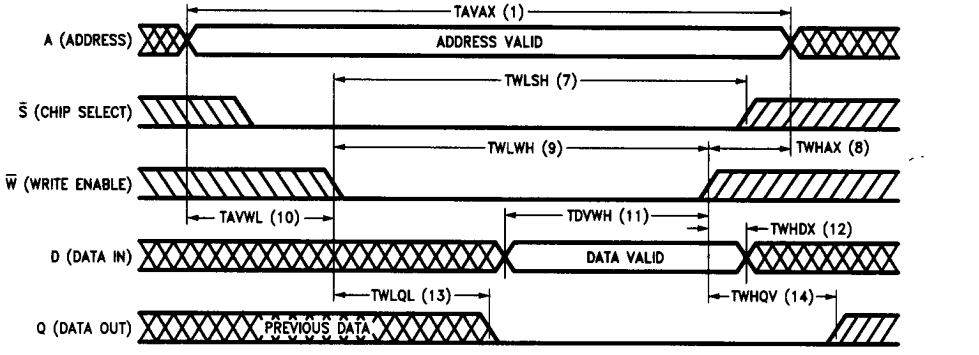
Write Cycle 1

This write cycle is $\overline{W}$ controlled, where $\overline{S}$ is active (LOW) prior to $\overline{W}$ becoming active (LOW). In this write cycle the data out (Q) may become active and requires observance of TWLQL to avoid data bus contention in common I/O applications. At the end of the write cycle the data out may become active if $\overline{W}$ becomes inactive (HIGH) prior to $\overline{S}$ becoming inactive (HIGH).

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	12 ns Device		15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	Min	Max	
1	TAVAX	TWC	Address Valid to Address Invalid	12		15		18		ns
7	TWLSH		Write Enable LOW to Chip Select HIGH	9		10		12		ns
8	TWHAX	TWHA	Write HIGH to Address Don't Care	0		0		3		ns
9	TWLWH	TW	Write LOW to Write HIGH	9		10		12		ns
10	TAVWL	TWSA	Address Valid to Write LOW	0		0		2		ns
11	TDVWH		Data Valid to Write HIGH	9		10		14		ns
12	TWHDX	TWHD	Write HIGH to Data Don't Care	0		0		3		ns
13	TWLQL	TWS	Write LOW to Output LOW		5		5		5	ns
14	TWHQV	TWR	Write HIGH to Output Valid		12		15		18	ns



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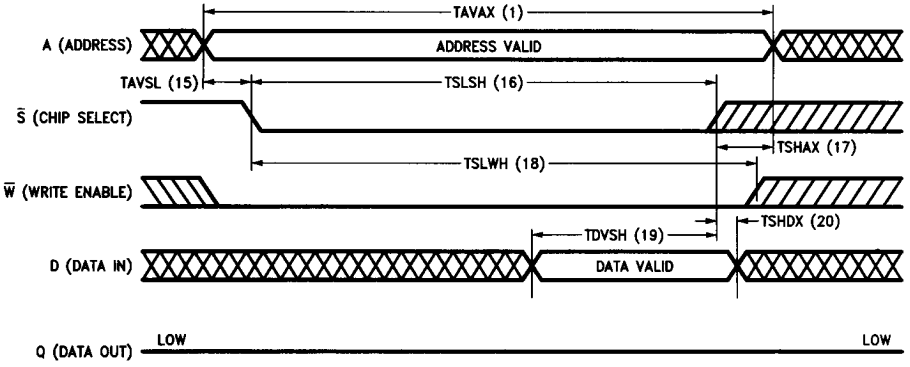
Write Cycle 2

This write cycle is $\overline{S}$ controlled, where $\overline{W}$ is active prior to, or coincident with, $\overline{S}$ becoming active (LOW). Write cycle 2 has indentical specifications to write cycle 1 with the exceptions of $\overline{W}$ and $\overline{S}$ being interchanged. This write cycle may be more convenient for common I/O applications because data bus restrictions are alleviated.

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	12 ns Device		15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	Min	Max	
15	TAVSL	TWSA	Address Valid to Chip Select LOW	0		0		2		ns
16	TSLSH		Chip Select LOW to Chip Select HIGH	9		10		12		ns
17	TSHAX	TWHA	Chip Select HIGH to Address Don't Care	0		0		3		ns
18	TSLWH		Chip Select LOW to Write Enable HIGH	9		10		12		ns
19	TDVSH		Data Valid to Chip Select HIGH	9		10		14		ns
20	TSHDX	TWHD	Chip Select HIGH to Data Don't Care	0		0		3		ns



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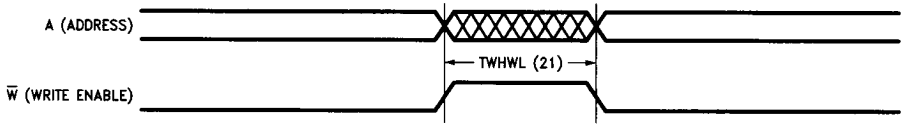
Consecutive Write Cycles

AC Timing Characteristics V_{CC} = Ground, T_C = 0°C to +85°C

No.	Symbol		Parameter	12 ns Device		15 ns Device		18 ns Device		Units
	Std.	Alt.		Min	Max	Min	Max	Min	Max	
21	TWHWL	$\overline{TWP}$	Write Enable HIGH to Write Enable LOW	3		4		4		ns
22	TSHSL	$\overline{TSP}$	Chip Select HIGH to Chip Select LOW	3		4		4		ns

Minimum Write Pulse Disable



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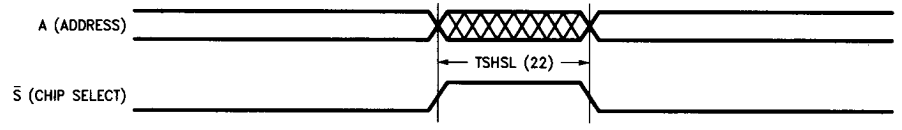
Minimum Select Pulse Disable



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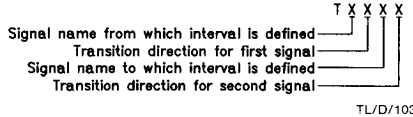
Standard Timing Parameter Abbreviations



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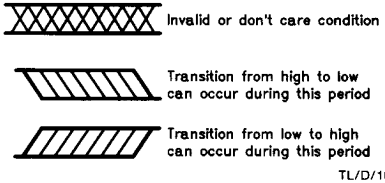
The transition definitions used in this data sheet are:

H = Transition to HIGH State
L = Transition to LOW State
V = Transition to Valid State
X = Transition to Invalid or Don't Care Condition

TIMING EXPLANATIONS

The AC Operating Conditions and Characteristics tables typically show either a minimum or maximum limit for a device parameter. Those timing parameters which show a minimum value do so because the system must supply at least that much time, even though most devices do not need the full amount. Thus, input requirements are specified from the external point of view. In contrast, responses from the memory devices (i.e., access times) are specified as a maximum time because the device will never provide the data later than this stated value, and usually, much sooner.



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Ordering Information

Part Number	Temperature Range	Package Type	Ordering Code
NM5104	0°C to +85°C	28-Pin Ceramic DIP	NM5104D12/15
NM5104	0°C to +85°C	28-Pin Flatpak	NM5104F12/15
NM100504	0°C to +85°C	28-Pin Ceramic DIP	NM100504D15/18
NM100504	0°C to +85°C	28-Pin Flatpak	NM100504F15/18