National Semiconductor

May 1996

NM24Cxx—Standard 2-Wire Bus Interface Serial EEPROM Family

General Description

The NM24Cxx devices are 2048/4096/8192/16,834 bits of CMOS nonvolatile electrically erasable memory. These devices conform to all specifications in the I²C™ 2-wire protocol and are designed to minimize device pin count and simplify PC board layout requirements.

The upper half of the memory of the 03/05/09/17 can be disabled (Write Protected) by connecting the WP pin to V_{CC}. This section of memory then becomes unalterable unless WP is switched to V_{SS}.

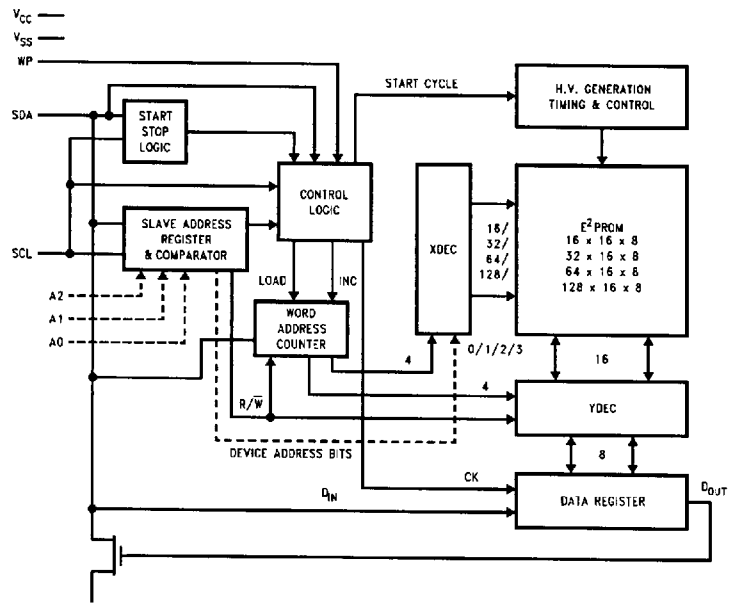
This communications protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). This bus structure allows for a maximum of 16k of EEPROM memory, which is supported by the NSC family in 2k, 4k, 8k, and 16k devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16k).

National EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Extended operating voltage 2.7V–5.5V
- 400 kHz clock frequency (F)
- 500 μA active current typical
  10 μA standby current typical
  1 μA standby typical (L)
  0.1 μA standby typical (LZ)
- I²C compatible interface
  — Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  — Minimizes total write time per byte
- Self timed write cycle
  Typical write cycle time of 6 ms
- Hardwire write protect for upper block (03/05/09/17) only
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8-pin mini-DIP, 8-pin SO, and 8-pin TSSOP (2k, 4k) only

Block Diagram



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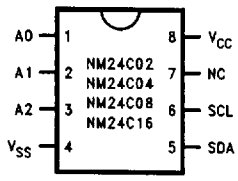
I²C™ is a trademark of Philips Corporation.

Connection Diagrams

Dual-In-Line Package (N)



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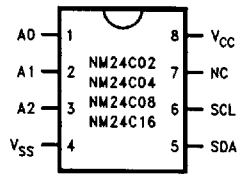
Top View

See NS Package Number N08E (N)

SO Package (M8)



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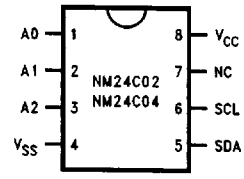
Top View

See NS Package Number M08A (M8)

TSSOP Package (MT8)



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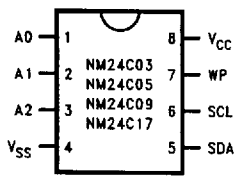
Top View

See NS Package Number MTC08 (MT8)

Pin Names

A0, A1, A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
NC	No Connection
V_{CC}	Power Supply

Dual-In-Line Package (N)



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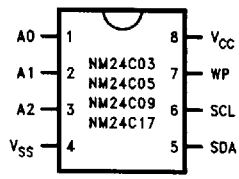
Top View

See NS Package Number N08E (N)

SO Package (M8)



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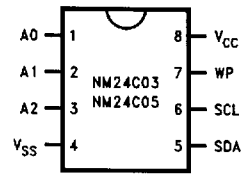
Top View

See NS Package Number M08A (M8)

TSSOP Package (MT8)



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Top View

See NS Package Number MTC08 (MT8)

Pin Names

A0, A1, A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
WP	Write Protect
V_{CC}	Power Supply

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM24CxxN
NM24CxxLN
NM24CxxM8
NM24CxxLM8
NM24C02MT8/NM24C04MT8
NM24C03MT8/NM24C05MT8
NM24C02LMT8/NM24C04LMT8
NM24C03LMT8/NM24C05LMT8
NM24CxxFN
NM24CxxFLN
NM24CxxFM8
NM24CxxFLM8
NM24C02FMT8/NM24C04FMT8
NM24C03FMT8/NM24C05FMT8
NM24C02FLMT8/NM24C04FLMT8
NM24C03FLMT8/NM24C05FLMT8

Extended Temperature Range (−40°C to +85°C)

Order Number
NM24CxxEN
NM24CxxLEN
NM24CxxEM8
NM24CxxLEM8
NM24C02EMT8/NM24C04EMT8
NM24C03EMT8/NM24C05EMT8
NM24C02LEMT8/NM24C04LEMT8
NM24C03LEMT8/NM24C05LEMT8
NM24CxxFEN
NM24CxxFLEN
NM24CxxFEM8
NM24CxxFLEM8
NM24C02FEMT8/NM24C04FEMT8
NM24C03FEMT8/NM24C05FEMT8
NM24C02FLEMT8/NM24C04FLEMT8
NM24C03FLEMT8/NM24C05FLEMT8

Product Specifications

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

Operating Conditions

Ambient Operating Temperature	
NM24Cxx	0°C to +70°C
NM24CxxE	−40°C to +85°C
Positive Power Supply	
NM24Cxx	4.5V to 5.5V
NM24CxxL	2.7V to 5.5V
NM24CxxLZ	2.7V to 5.5V

Standard V_{CC} DC and AC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.5	1.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		10	50	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Low V_{CC} DC and AC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		0.5	1.0	mA
I_{SB} (Note 2)	Standby Current	V_{IN} = GND or V_{CC}		1	10	µA
	Standby Current for LZ	V_{IN} = GND or V_{CC}		0.1	1	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = +25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and C_L = 100 pF

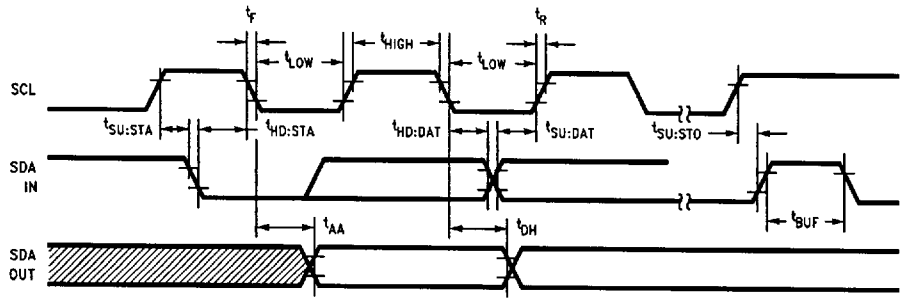
Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Read and Write Cycle Limits (Standard and Low V_{CC} Range—2.7V–5.5V)

Symbol	Parameter	100 kHz		400 kHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse Width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	1.4	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		μs
t_{LOW}	Clock Low Period	4.7		1.5		μs
t_{HIGH}	Clock High Period	4.0		0.6		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		μs
$t_{HD:DAT}$	Data in Hold Time	0		0		μs
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	μs
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		μs
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time—NM24Cxx —NM24CxxL/xxLZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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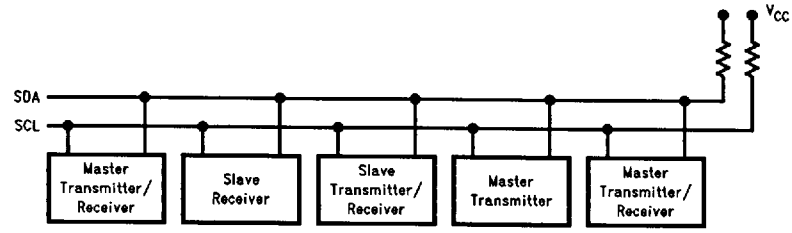
System Layout



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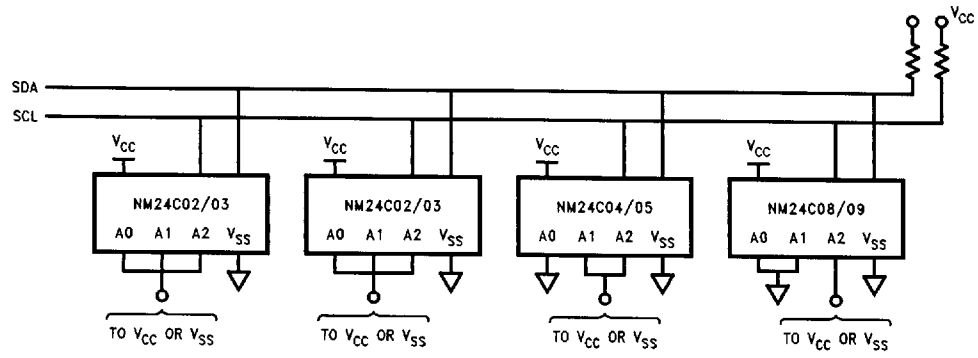
Note: Due to open drain configuration of SDA, a bus-level pull-up resistor is called for (typical value = 4.7 kΩ).

FIGURE 1. Typical System Configuration

Example of 16k (Maximum Size) of Memory on 2-Wire Bus



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Note: The SDA pull-up resistor is required due to the open-drain/open collector output of I²C bus devices.
The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.
It is recommended that the total line capacitance be less than 400 pF.

System Layout (Continued)

Device	Address Pins			Memory Size	# of Page Blocks
	A0	A1	A2		
NM24C02/03	ADR	ADR	ADR	2048 Bits	1
NM24C04/05	No Connect	ADR	ADR	4096 Bits	2
NM24C08/09	No Connect	No Connect	ADR	8192 Bits	4
NM24C16/17	No Connect	No Connect	No Connect	16,384 Bits	8

ADR is the hardware address (V_{CC}/1 or V_{SS}/0) of the device(s) used.

Device Operation Inputs (A0, A1, A2)

Device address pins A0, A1, and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM chip address. Table I shows the active pins across the NM24Cxx device family.

TABLE I

Device	A0	A1	A2	Effects of Addresses
NM24C02/03	ADR	ADR	ADR	2^3 = 8 (8) × (2k) = 16k
NM24C04/05	x	ADR	ADR	2^2 = 8 (8) × (2k) = 16k
NM24C08/09	x	x	ADR	2^1 = 8 (8) × (2k) = 16k
NM24C16/17	x	x	x	2^0 = 8 (8) × (2k) = 16k

BACKGROUND INFORMATION (I^2C Bus)

As mentioned, the I^2C bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

As shown below, the EEPROMs on the I^2C bus may be configured in any manner required, the total memory addressed can not exceed 16k (16,384 bits). EEPROM memory address programming is controlled by 2 methods:

- Hardware configuring the A0, A1, and A2 pins (Device Address pins) with pull-up or pull-down resistors. **All unused pins must be grounded** (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]–[DEVICE ADDRESS]–[PAGE BLOCK ADDRESS]–[BYTE ADDRESS]

Definitions	
WORD	8 bits (byte) of data
PAGE	16 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle
PAGE BLOCK	2,048 (2k) bits organized into 16 pages of addressable memory. (8 bits) × (16 bytes) × (16 pages) = 2,048 bits
MASTER	Any I^2C device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave)
RECEIVER	Device currently receiving data on the bus (Master or Slave)

Pin Descriptions

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

WP Write Protection (03/05/09/17) Only

If tied to V_{CC}, PROGRAM operations onto the upper half of the memory will not be executed. READ operations are possible. If tied to V_{SS}, normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24Cxx supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24Cxx will be considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 2* and *3*.

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24Cxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24Cxx to place the device in the standby power mode.

Write Cycle Timing

ACKNOWLEDGE

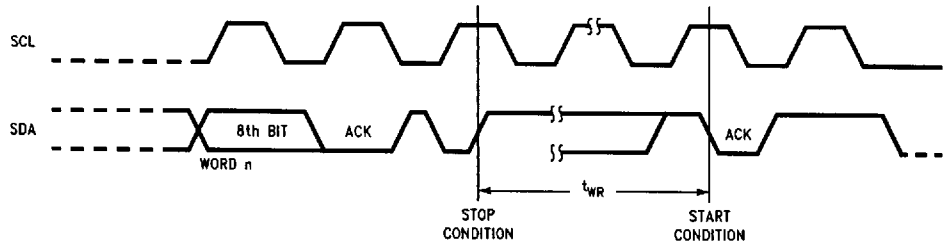
Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits.

During the ninth clock cycle the receiver will pull the SDA line to LOW to acknowledge that it received the eight bits of data. Refer to *Figure 4*.

The NM24Cxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24Cxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM2Cxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Write Cycle Timing (Continued)



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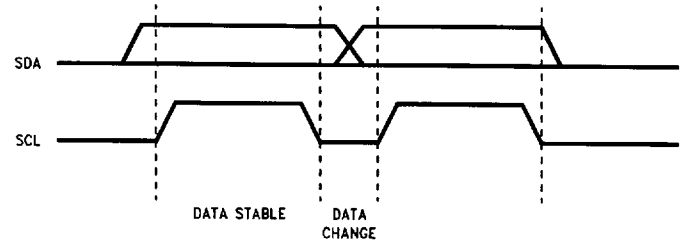

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FIGURE 2. Data Validity

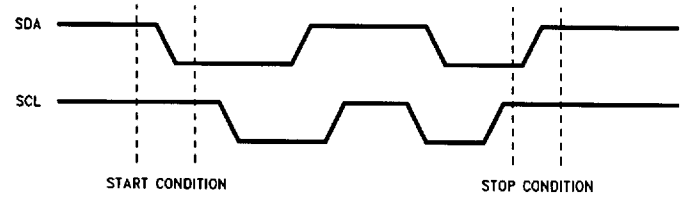

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FIGURE 3. Start and Stop Definition

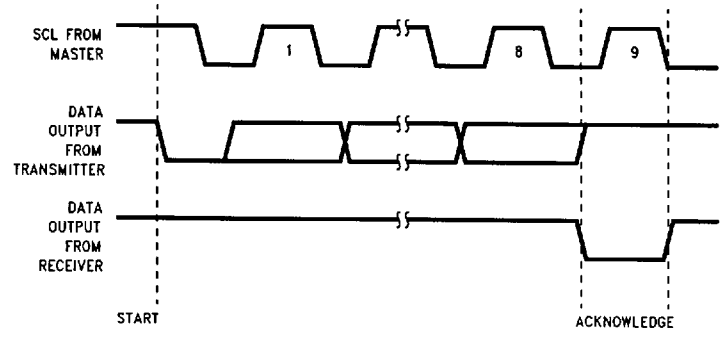

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FIGURE 4. Acknowledge Response from Receiver

Write Cycle Timing (Continued)

DEVICE ADDRESSING

Following a start condition, the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier (see *Figure 5*). This is fixed as 1010 for all devices.

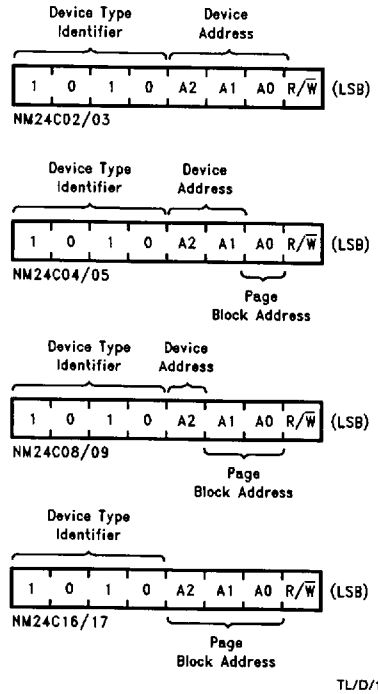

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FIGURE 5. Slave Addresses

Refer to the following table for Slave Addresses string details:

Device	A0	A1	A2	Page Blks	Page Block Addresses
NM24C02/03	A	A	A	1 (2k)	(None)
NM24C04/05	P	A	A	2 (4k)	0 1
NM24C08/09	P	P	A	4 (8k)	00 01 10 11
NM24C16/17	P	P	P	8 (16k)	000 001 010 011 ...111

A: Refers to a hardware configured Device Address pin.
P: Refers to an internal PAGE BLOCK memory segment.

All I²C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2k bits (for Word addressess 0000 through 1111). Therefore, address bits A0, A1, or A2 (if designated "P") are used to access a PAGE BLOCK in conjuction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a read operation is to be executed, and a "0" initiates the write mode.

A simple review: After the NM24Cxx recognizes the start condition, the devices interfaced to the I²C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24Cxx responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24Cxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24Cxx inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

PAGE WRITE

The NM24Cxx is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24Cxx will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 9* for the address, acknowledge, and data transfer sequence.

ACKNOWLEDGE POLLING

Once the stop condition is issued to indicate the end of the host's write operation the NM24Cxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24Cxx is sfill busy with the write operation no ACK will be returned. If the NM24Cxx has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION (03/05/09/17) ONLY

Programming of the upper half of the memory will not take place if the WP pin of the NM24Cxx is connected to V_{CC}. The NM24Cxx will accept slave and word addresses; but if the memory accessed is write protected by the WP pin, the NM24Cxx will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

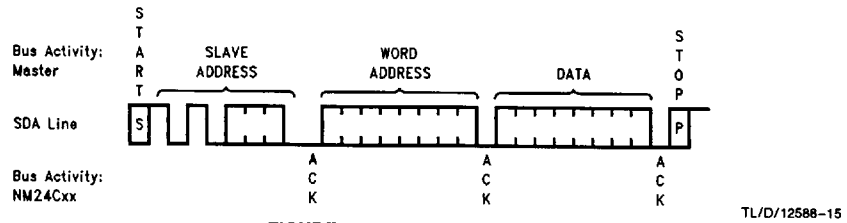


FIGURE 6. Byte Write

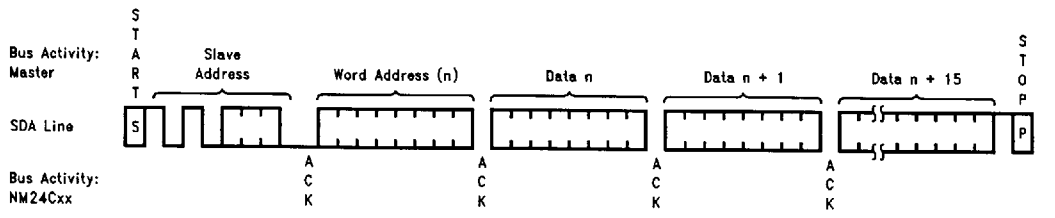


FIGURE 7. Page Write

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

CURRENT ADDRESS READ

Internally the NM24Cxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24Cxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24Cxx discontinues transmission. Refer to *Figure 8* for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24Cxx and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24Cxx discontinues transmission. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24Cxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24Cxx continues to output data for each acknowledge received. Refer to *Figure 10* for the address, acknowledge, and data transfer sequence.

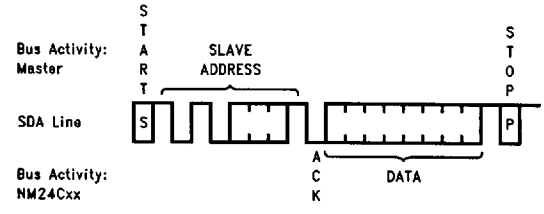


FIGURE 8. Current Address Read

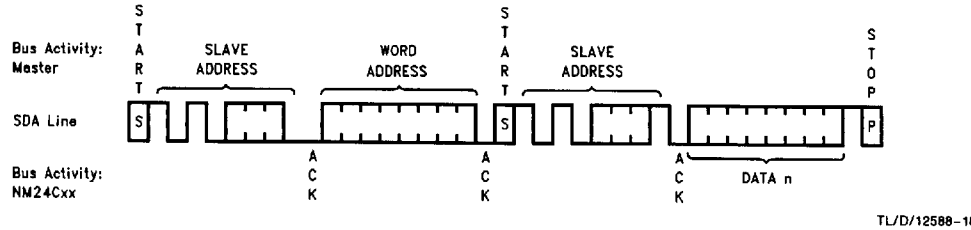
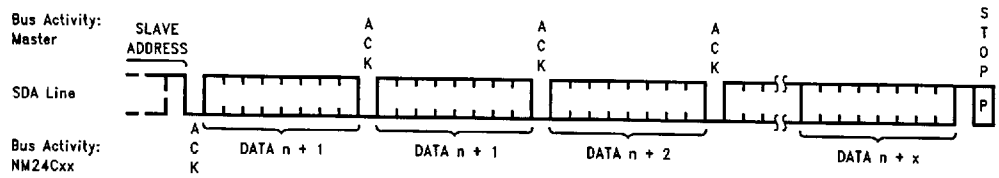


FIGURE 9. Random Read

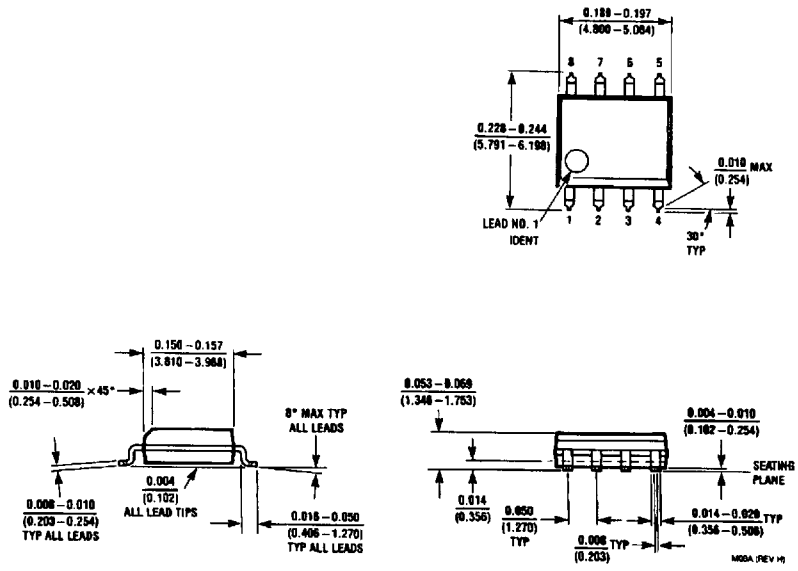
Read Operations (Continued)



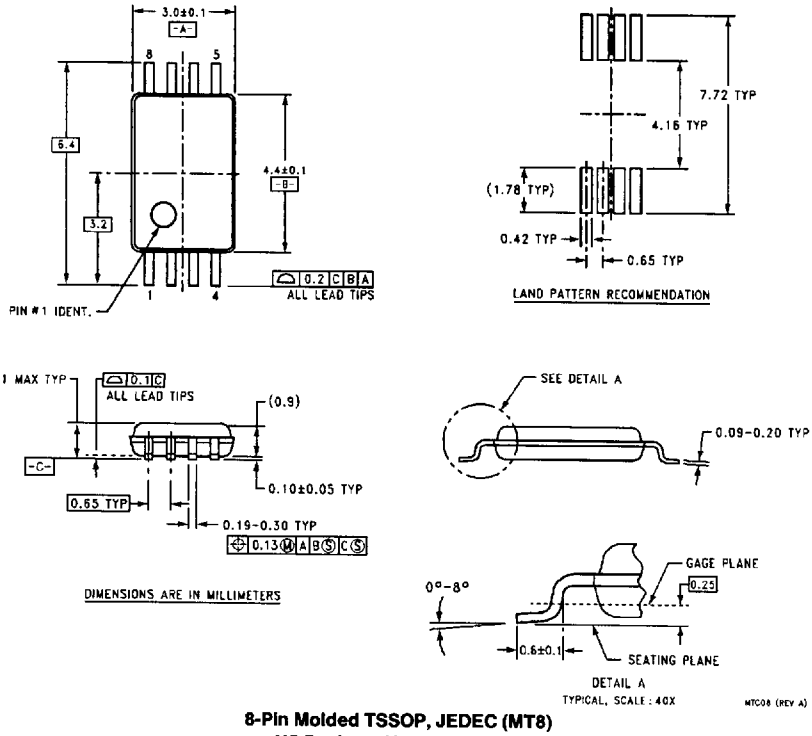
TL/D/12588–19

FIGURE 10. Sequential Read

Physical Dimensions inches (millimeters) unless otherwise noted

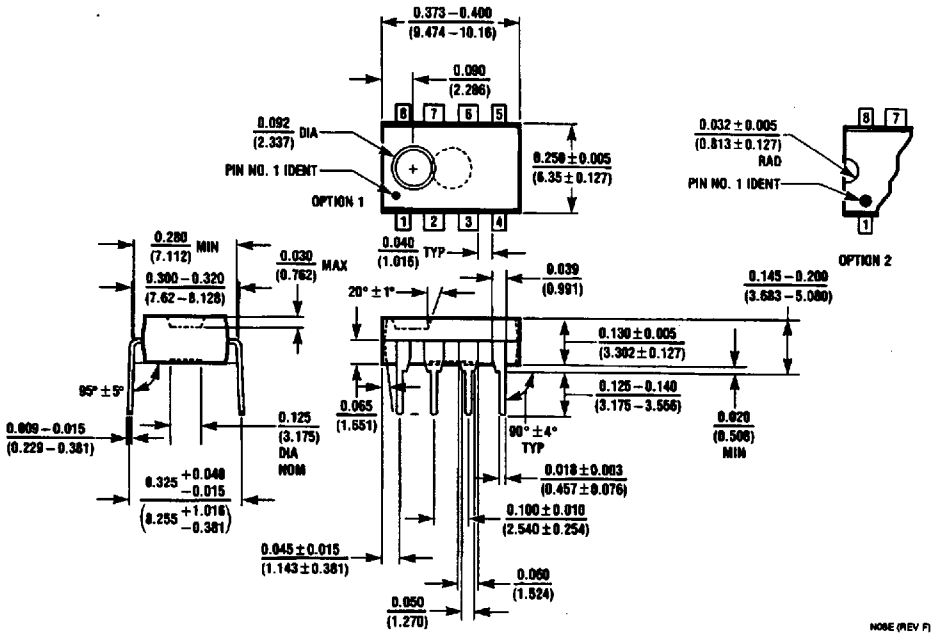


8-Pin Molded Small Outline Package (M8)
NS Package Number M08A



8-Pin Molded TSSOP, JEDEC (MT8)
NS Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
NS Package Number N08E

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