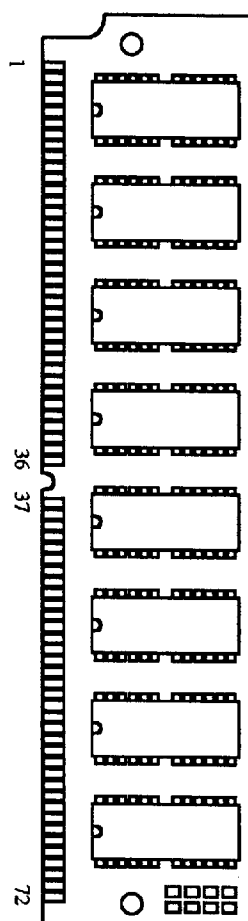


Description

The GMM7324210BNS/SG is a 4M x 32 bits Dynamic RAM MODULE which is assembled 8 pieces of 4M x 4bit EDO DRAMs in 24(26) pin SOJ package on single sides the printed circuit board with decoupling capacitors. The GMM7324210BNS/SG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size. The GMM7324210BNS/SG provides common data inputs and Extended Data Outputs.

• GMM7324210BNS/SG (Single Side)



Features

- 72 pins Single In-Line Package
 - GMM7324210BNS : Solder plating
 - GMM7324210BNSG : Gold plating
- Extended Data Out (EDO) Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time

(Unit: ns)

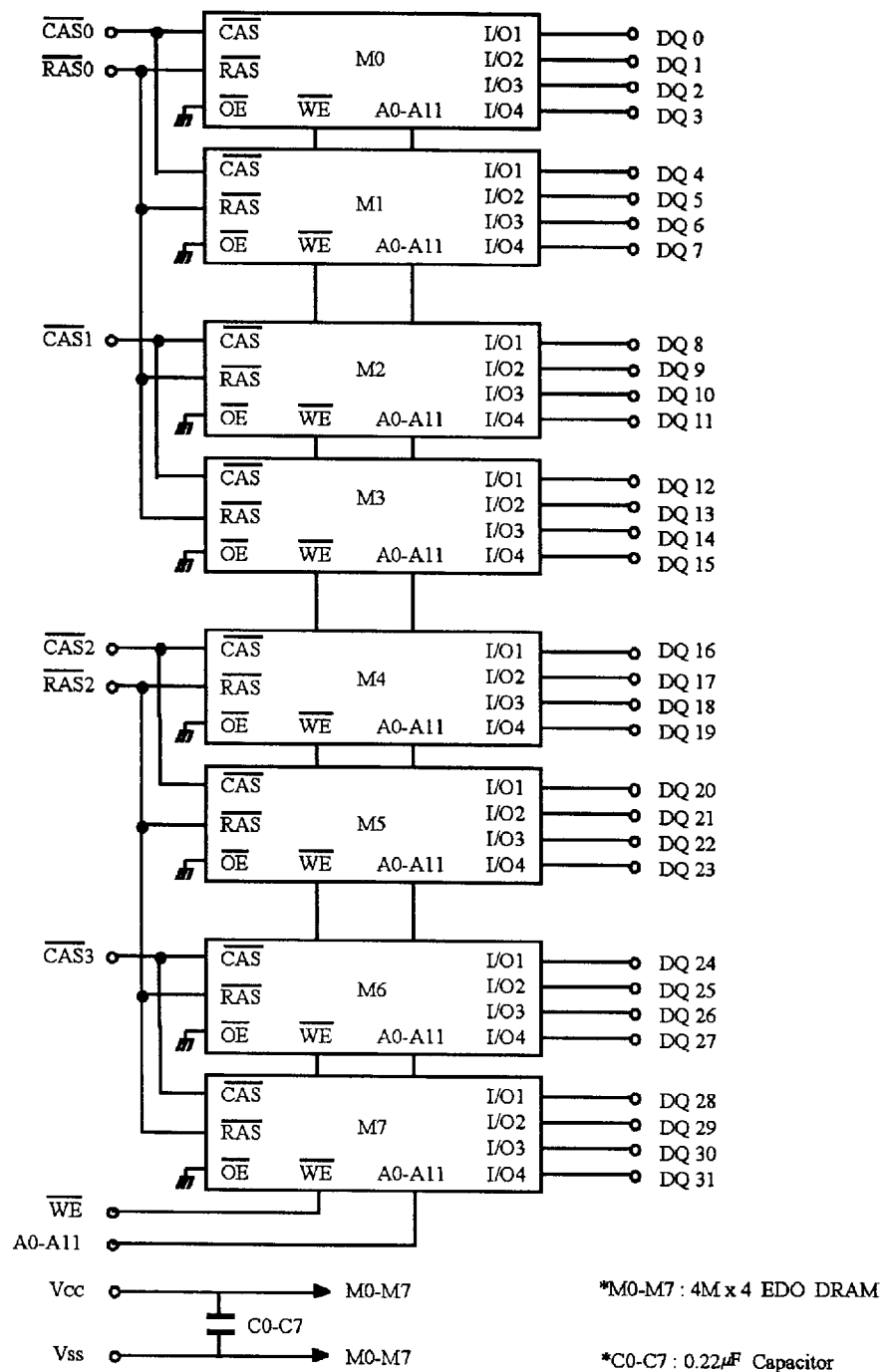
	t _{TRAC}	t _{CAC}	t _{RC}	t _{HPC}
GMM7324210BNS/SG-6	60	15	104	25
GMM7324210BNS/SG-7	70	18	124	30
GMM7324210BNS/SG-8	80	20	144	35

- Low Power
 - Active : 4,840/4,400/3,960 mW (MAX)
 - Standby : 44mW (CMOS level : MAX)
- RAS Only Refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 4096 Refresh Cycles/64ms

Pin Configuration (Top View)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{SS}	19	A ₁₀	37	NC	55	DQ ₁₁
2	DQ ₀	20	DQ ₄	38	NC	56	DQ ₂₇
3	DQ ₁₆	21	DQ ₂₀	39	V _{SS}	57	DQ ₁₂
4	DQ ₁	22	DQ ₅	40	$\overline{\text{CAS}}_0$	58	DQ ₂₈
5	DQ ₁₇	23	DQ ₂₁	41	$\overline{\text{CAS}}_2$	59	V _{CC}
6	DQ ₂	24	DQ ₆	42	$\overline{\text{CAS}}_3$	60	DQ ₂₉
7	DQ ₁₈	25	DQ ₂₂	43	$\overline{\text{CAS}}_1$	61	DQ ₁₃
8	DQ ₃	26	DQ ₇	44	$\overline{\text{RAS}}_0$	62	DQ ₃₀
9	DQ ₁₉	27	DQ ₂₃	45	NC	63	DQ ₁₄
10	V _{CC}	28	A ₇	46	NC	64	DQ ₃₁
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ ₁₅
12	A ₀	30	V _{CC}	48	NC	66	NC
13	A ₁	31	A ₈	49	DQ ₈	67	PD ₁
14	A ₂	32	A ₉	50	DQ ₂₄	68	PD ₂
15	A ₃	33	NC	51	DQ ₉	69	PD ₃
16	A ₄	34	$\overline{\text{RAS}}_2$	52	DQ ₂₅	70	PD ₄
17	A ₅	35	NC	53	DQ ₁₀	71	NC
18	A ₆	36	NC	54	DQ ₂₆	72	V _{SS}

Block Diagram



Pin Description

Pin	Function	Pin	Function
A0-A11	Address Inputs	PD1-PD4	Presence Detect
DQ0-DQ34	Data Input/Output	V _{cc}	Power (+5V)
$\overline{\text{RAS0}}, \overline{\text{RAS2}}$	Row Address Strobe	V _{ss}	Ground
$\overline{\text{CAS0}}, \overline{\text{CAS3}}$	Column Address Strobe	NC	No Connection
$\overline{\text{WE}}$	Read/Write Enable		

Presence Detect Pins (Optional)

Pin	60ns	70ns	80ns
PD1	V _{ss}	V _{ss}	V _{ss}
PD2	NC	NC	NC
PD3	NC	V _{ss}	NC
PD4	NC	NC	V _{ss}

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature under Bias	0 ~ 70	°C
T _{STG}	Storage Temperature (Plastic)	-55 ~ 125	°C
V _{IN} /V _{OUT}	Voltage on any Pin Relative to V _{ss}	-1.0 ~ 7.0	V
V _{CC}	Power Supply Voltage	-1.0 ~ 7.0	V
I _{OUT}	Short Circuit Output Current	50	mA
P _D	Power Dissipation	8	W

*Note: 1. Stress greater than above "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended DC Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V _{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V _{IH}	Input High Voltage	2.4	-	6.5	V	1
V _{IL}	Input Low Voltage	-1.0	-	0.8	V	1

*Note: 1. All voltages referenced to V_{ss}.

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70^\circ C$)

Symbol	Parameter	Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage ($I_{OUT} = -5mA$)	2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage ($I_{OUT} = 4.2mA$)	0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC\ min}$)	60 ns	-	640	mA 1, 2
		70 ns	-	560	
		80 ns	-	520	
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS} = V_{IH}$)	-	16	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC\ min}$)	60 ns	-	640	mA 2
		70 ns	-	560	
		80 ns	-	520	
I_{CC4}	EDO Page Mode Current Average Power Supply Current EDO Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address cycling: $t_{RPC} = t_{RPC\ min}$)	60 ns	-	800	mA 1, 3
		70 ns	-	720	
		80 ns	-	640	
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS} \geq V_{CC} - 0.2V$)	-	8	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current ($t_{RC} = t_{RC\ min}$)	60 ns	-	640	mA
		70 ns	-	560	
		80 ns	-	520	
I_{CC7}	Standby Current $\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IL}$ $D_{OUT} = \text{Enable}$	-	40	mA	1
I_{IL}	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 7V$) All Other Pins Not Under Test = 0V	-80	80	μA	
I_{OL}	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 7V$)	-10	10	μA	

Note: 1. I_{CC} depends on output load condition when the device is selected. $I_{CC(max)}$ is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25^\circ C$, $f = 1MHz$)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (A0~A11)	-	60	pF	1
C_{I2}	Input Capacitance ($\overline{WE}$)	-	70	pF	1, 2
C_{I3}	Input Capacitance ($\overline{RAS0}, \overline{RAS2}$)	-	42	pF	1, 2
C_{I4}	Input Capacitance ($\overline{CAS0} \sim \overline{CAS3}$)	-	25	pF	1, 2
$C_{I/O}$	I/O Capacitance (DQ0~DQ31)	-	17	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{CAS} = V_{IH}$ to disable DOUT.

AC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0 \sim 70^\circ C$, Notes 1, 15)

The GMM7324210BNS/SG writes data only in early write cycle ($twcs \geq twcs(min)$).
 Delayed write cycle is not available because of I/O common.

Read, Write and Refresh Cycle (Common Parameters)

Symbol	Parameter	GMM7324210 BNS/SG-6		GMM7324210 BNS/SG-7		GMM7324210 BNS/SG-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	104	-	124	-	144	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	10	10,000	13	10,000	15	10,000	ns	
t_{ASR}	Row Address Setup Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Setup Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	13	-	15	-	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	52	20	60	ns	9
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	10
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	18	-	20	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	48	-	58	-	68	-	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	8
t_{REF}	Refresh Period	-	32	-	32	-	32	ms	

Read Cycle

Symbol	Parameter	GMM7324210 BNS/SG-6		GMM7324210 BNS/SG-7		GMM7324210 BNS/SG-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RAC}	Access Time from $\overline{\text{RAS}}$	-	60	-	70	-	80	ns	2, 3
t _{CAC}	Access Time from $\overline{\text{CAS}}$	-	15	-	18	-	20	ns	3, 4
t _{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	3, 5, 14
t _{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
t _{RCH}	Read Command Hold Time to $\overline{\text{CAS}}$	0	-	0	-	0	-	ns	6
t _{RRH}	Read Command Hold Time to $\overline{\text{RAS}}$	0	-	0	-	0	-	ns	6
t _{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	30	-	35	-	40	-	ns	
t _{CAL}	Column Address to $\overline{\text{CAS}}$ Lead Time	18	-	23	-	28	-	ns	
t _{OFF}	Output Buffer Turn-off Time	-	15	-	15	-	15	ns	7
t _{OFFR}	Output Buffer Turn-off Time to $\overline{\text{RAS}}$	-	15	-	15	-	15	ns	7, 17
t _{WEZ}	Output Buffer Turn-off Time to $\overline{\text{WE}}$	-	15	-	15	-	15	ns	7
t _{OH}	Output Data Hold Time	3	-	3	-	3	-	ns	
t _{OHR}	Output Data Hold Time form $\overline{\text{RAS}}$	3	-	3	-	3	-	ns	
t _{RCHR}	Read Command Hold Time from $\overline{\text{RAS}}$	60	-	70	-	80	-	ns	
t _{CLZ}	$\overline{\text{CAS}}$ to Output in low-Z	0	-	0	-	0	-	ns	

Write Cycle

Symbol	Parameter	GMM7324210 BNS/SG-6		GMM7324210 BNS/SG-7		GMM7324210 BNS/SG-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	11
t _{WCH}	Write Command Hold Time	10	-	13	-	15	-	ns	
t _{WP}	Write Command Pulse Width	10	-	10	-	10	-	ns	
t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	10	-	13	-	15	-	ns	
t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	10	-	13	-	15	-	ns	
t _{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	12
t _{DH}	Data-in Hold Time	10	-	15	-	15	-	ns	12

Refresh Cycle

Symbol	Parameter	GMM7324210 BNS/SG-6		GMM7324210 BNS/SG-7		GMM7324210 BNS/SG-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{CSR}	$\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	5	-	5	-	5	-	ns	
t _{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t _{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	0	-	0	-	0	-	ns	
t _{WRP}	$\overline{\text{WE}}$ Set-up Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	0	-	0	-	0	-	ns	
t _{WRH}	$\overline{\text{WE}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle)	10	-	10	-	10	-	ns	

Extended Data Out (EDO) Mode Cycle

Symbol	Parameter	GMM7324210 BNS/SG-6		GMM7324210 BNS/SG-7		GMM7324210 BNS/SG-8		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{HPC}	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
t _{CP}	EDO Mode $\overline{\text{CAS}}$ Precharge Time	10	-	13	-	15	-	ns	
t _{RASP}	EDO Mode $\overline{\text{RAS}}$ Pulse Width	-	100,000	-	100,000	-	100,000	ns	16
t _{ACP}	Access Time from $\overline{\text{CAS}}$ Precharge	-	35	-	40	-	45	ns	3,14
t _{RHCP}	$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	35	-	40	-	45	-	ns	
t _{RCHP}	Read Command Hold Time from $\overline{\text{CAS}}$ Precharge	35	-	40	-	45	-	ns	
t _{DOH}	Output Data Hold Time from $\overline{\text{CAS}}$ Low	3	-	3	-	3	-	ns	

Notes:

1. AC measurements assume $t_T = 5\text{ ns}$.
2. Assumes that $\text{trcd} \leq \text{trcd}(\text{max})$ and $\text{trad} \leq \text{trad}(\text{max})$. If trcd or trad is greater than the maximum recommended value shown in this table, trac exceeds the value shown.
3. Measured with a load circuit equivalent to 1TTL loads and 100pF.
4. Assumes that $\text{trcd} \geq \text{trcd}(\text{max})$ and $\text{trad} \leq \text{trad}(\text{max})$.
5. Assumes that $\text{trcd} \leq \text{trcd}(\text{max})$ and $\text{trad} \geq \text{trad}(\text{max})$.
6. Either trch or trrh must be satisfied for a read cycles.
7. $\text{toff}(\text{max})$ defines the time at which the outputs achieve the open circuit condition and is not referenced to output voltage levels.
8. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
9. Operation with the $\text{trcd}(\text{max})$ limit insures that $\text{trac}(\text{max})$ can be met, $\text{trcd}(\text{max})$ is specified as a reference point only, if trcd is greater than the specified $\text{trcd}(\text{max})$ limit, then access time is controlled exclusively by tcac .
10. Operation with the $\text{trad}(\text{max})$ limit insures that $\text{trac}(\text{max})$ can be met, $\text{trad}(\text{max})$ is specified as a reference point only, if trad is greater than the specified $\text{trad}(\text{max})$ limit, then access time is controlled exclusively by taa .
11. twcs is not restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $\text{twcs} \geq \text{twcs}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
12. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles.
13. trasp is defines $\overline{\text{RAS}}$ pulse width in EDO Mode cycles.
14. Access time is determined by the longer of taa or tcac or tacr .
15. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles are required.

Timing Waveforms

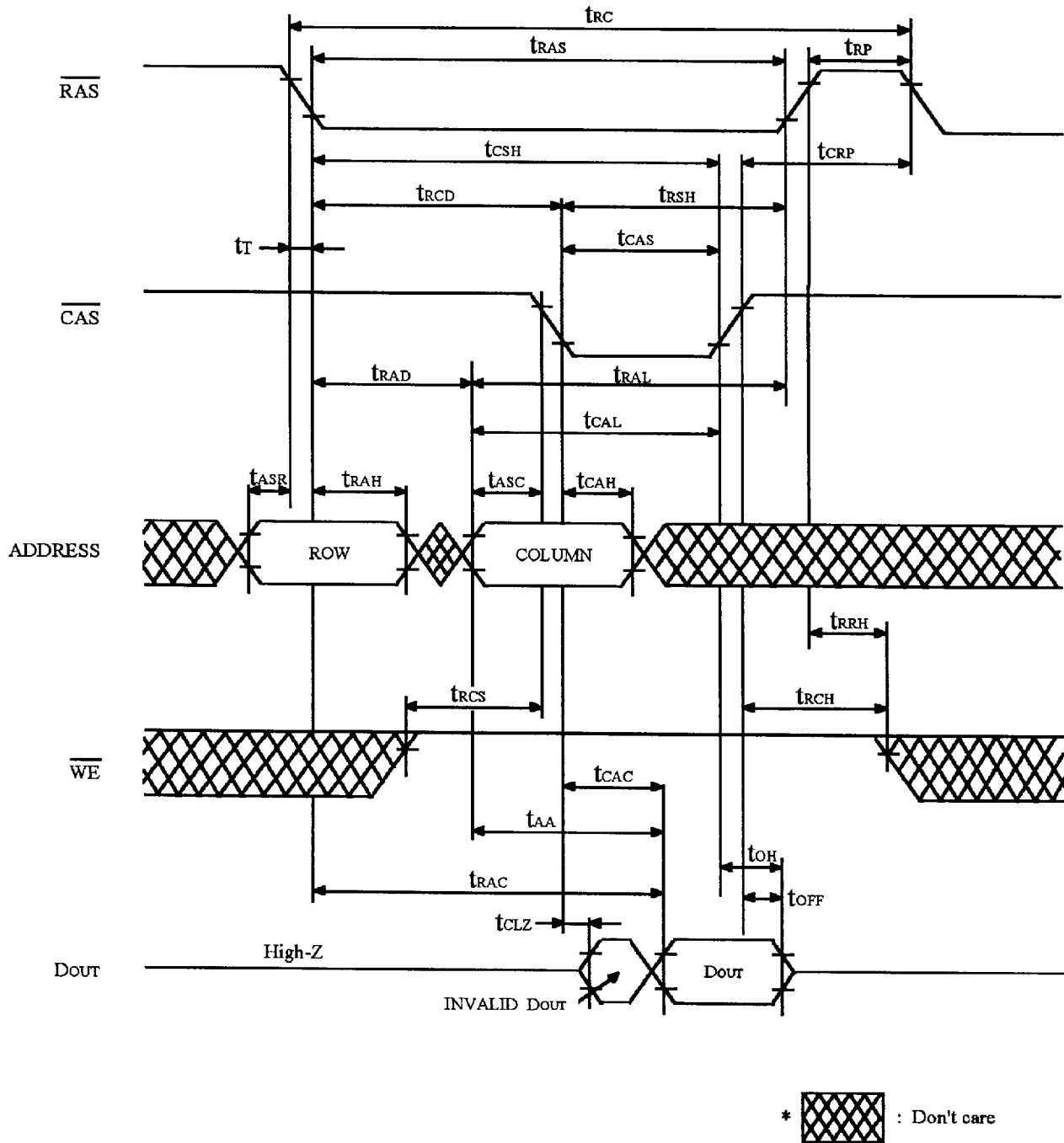
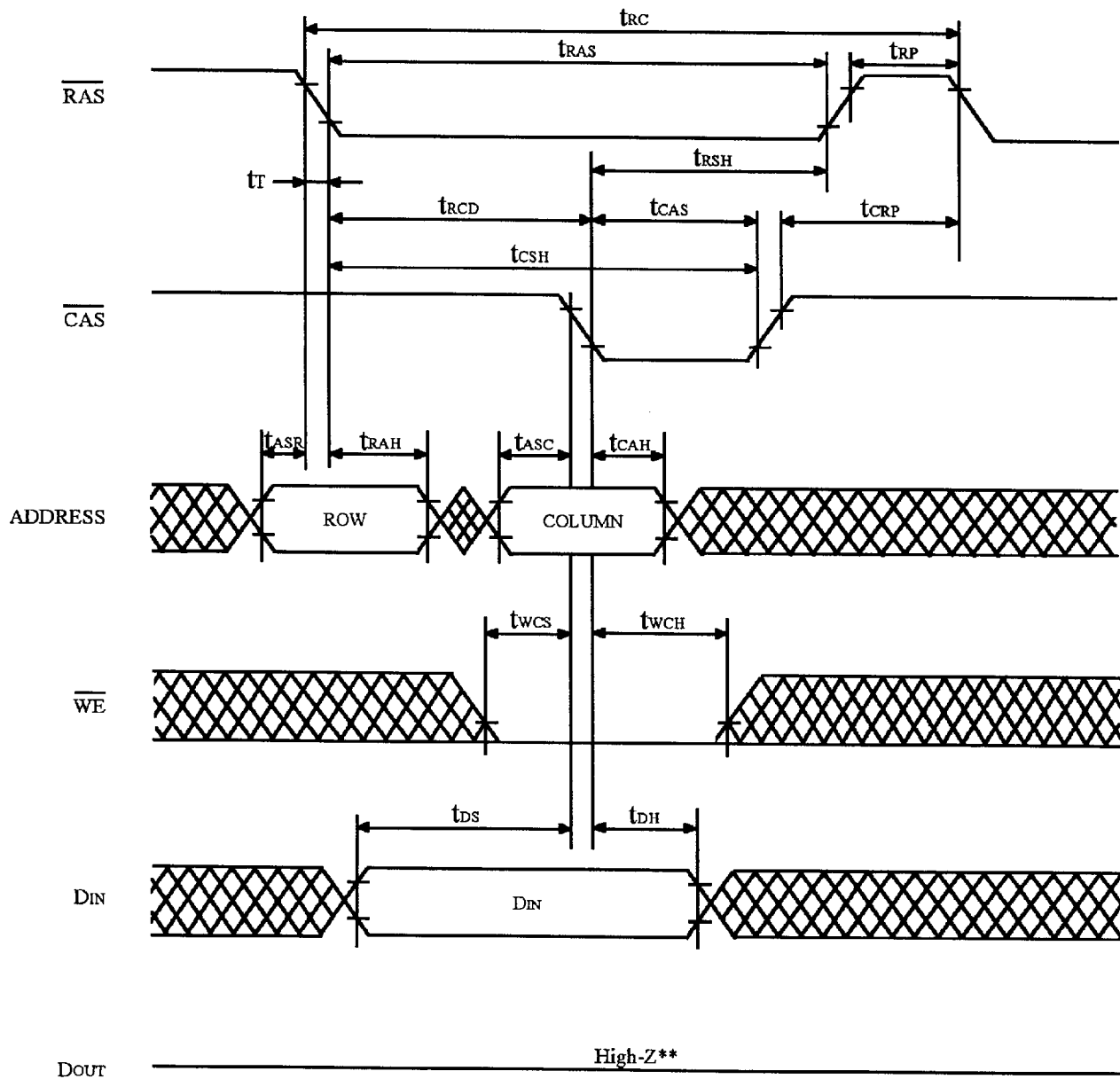


FIGURE 1. READ CYCLE



*  : Don't care

** $t_{wcs} \geq t_{wcs}(\text{min})$

FIGURE 2. EARLY WRITE CYCLE

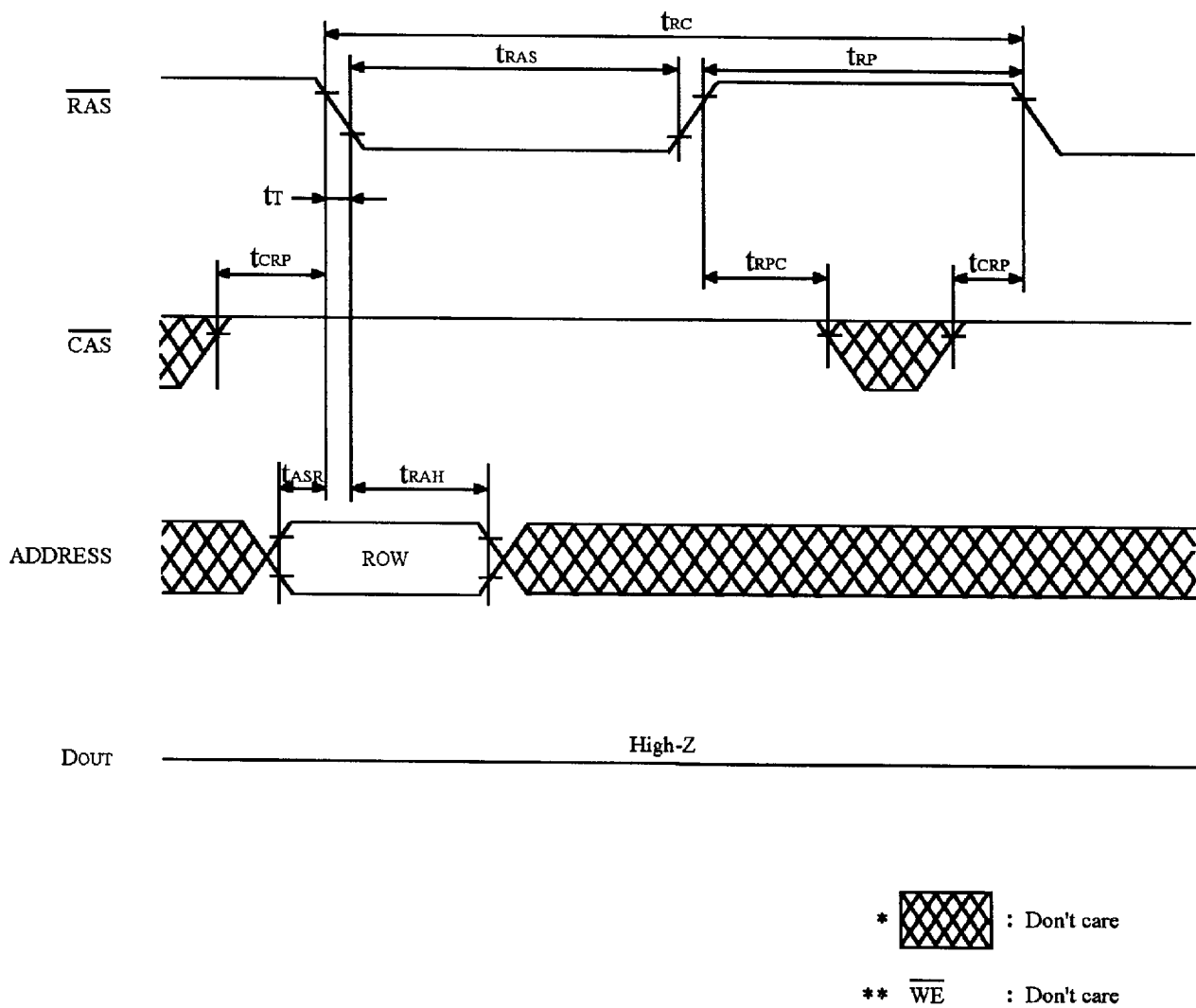
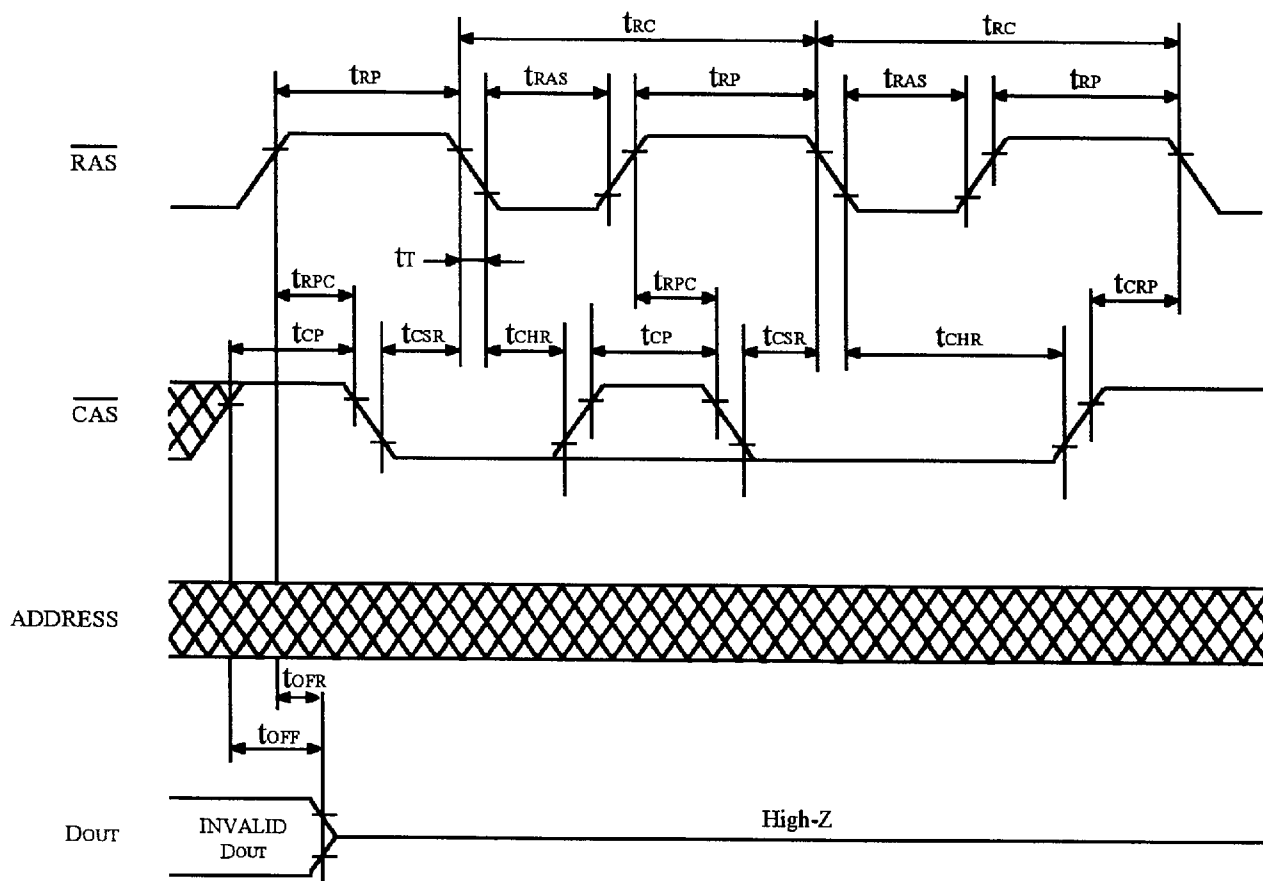


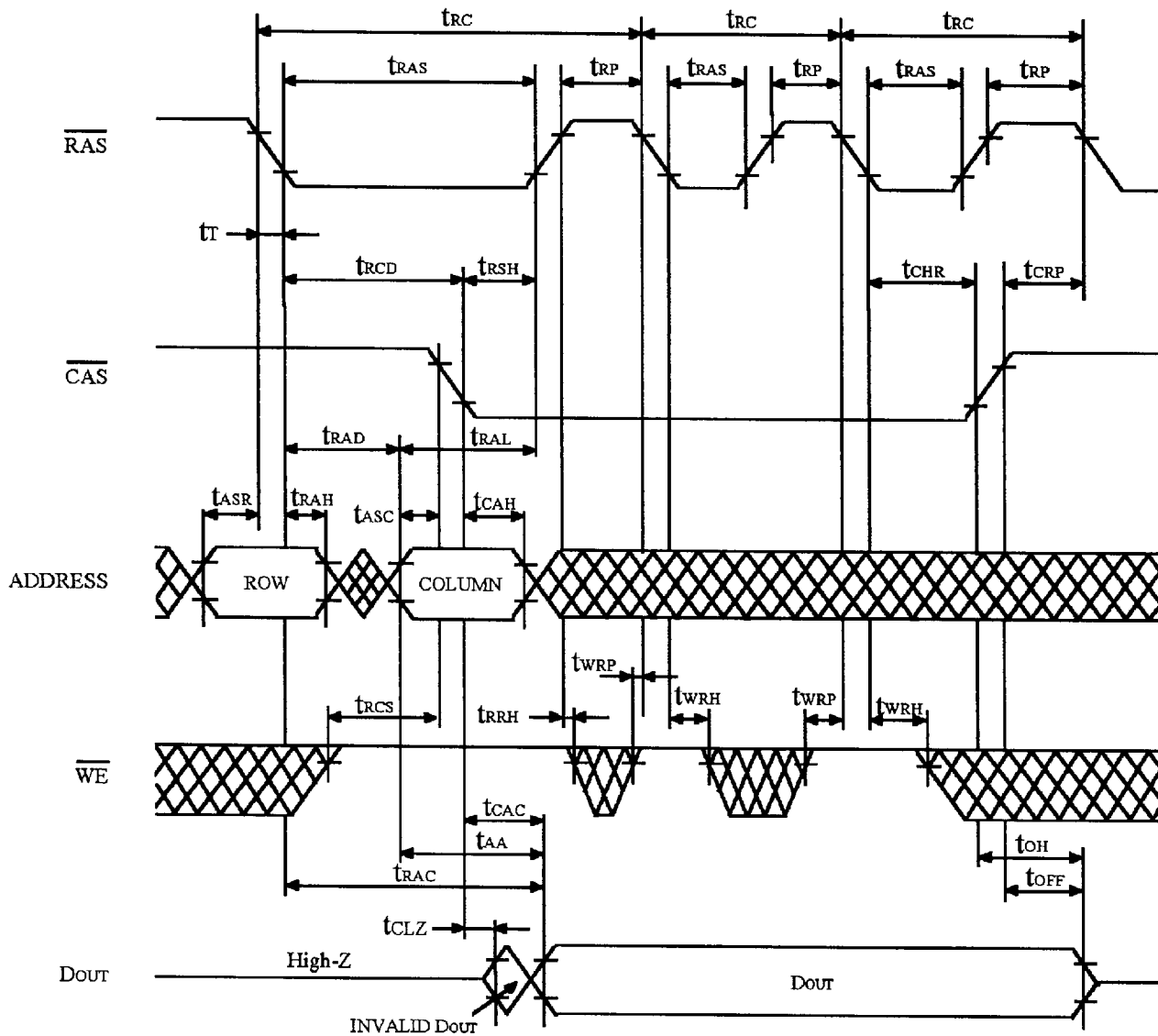
FIGURE 3. $\overline{\text{RAS}}$ ONLY REFRESH CYCLE



*  : Don't care

** $\overline{WE}$: V_{IH}

FIGURE 4. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



*  : Don't care

FIGURE 5. HIDDEN REFRESH CYCLE

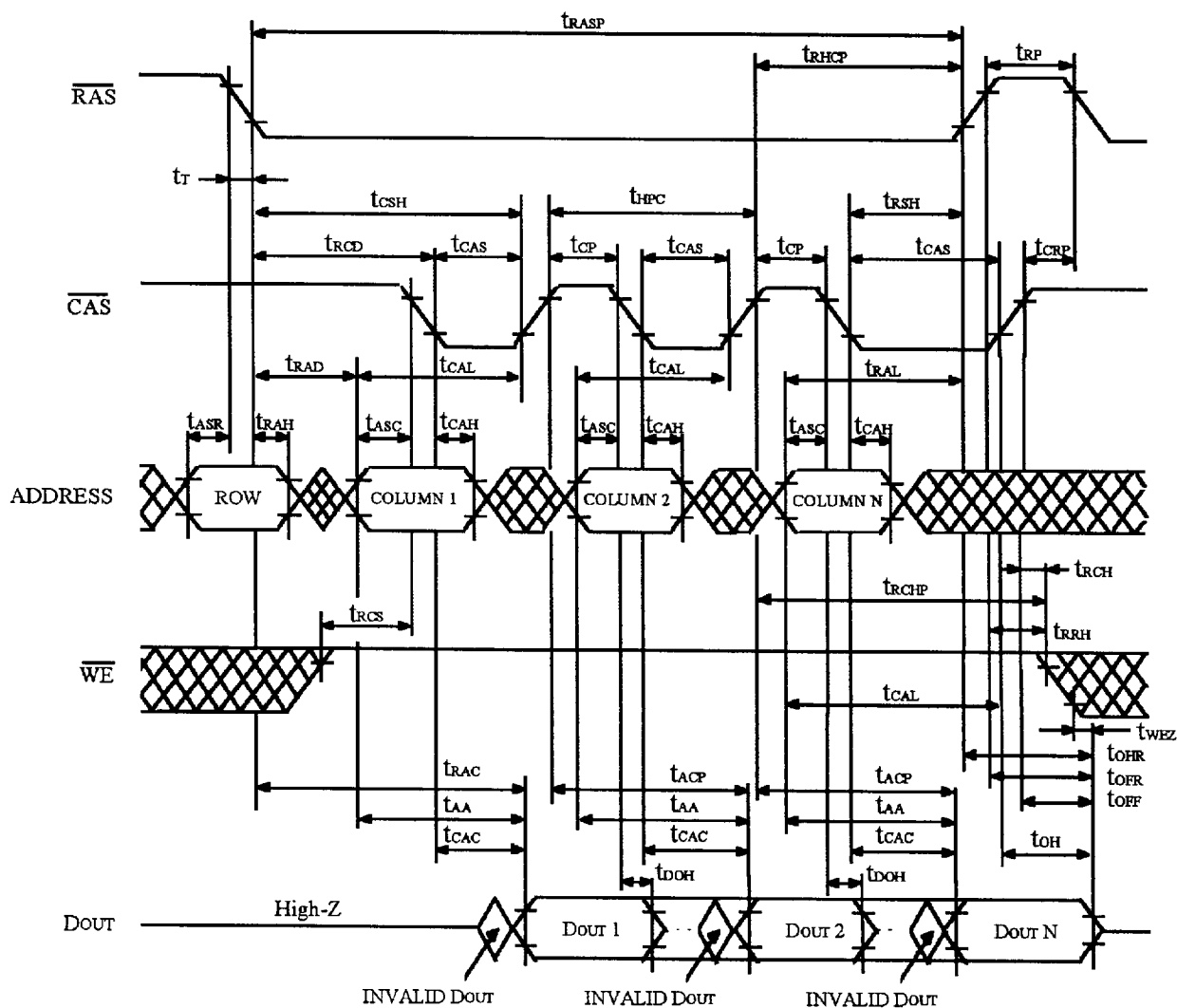
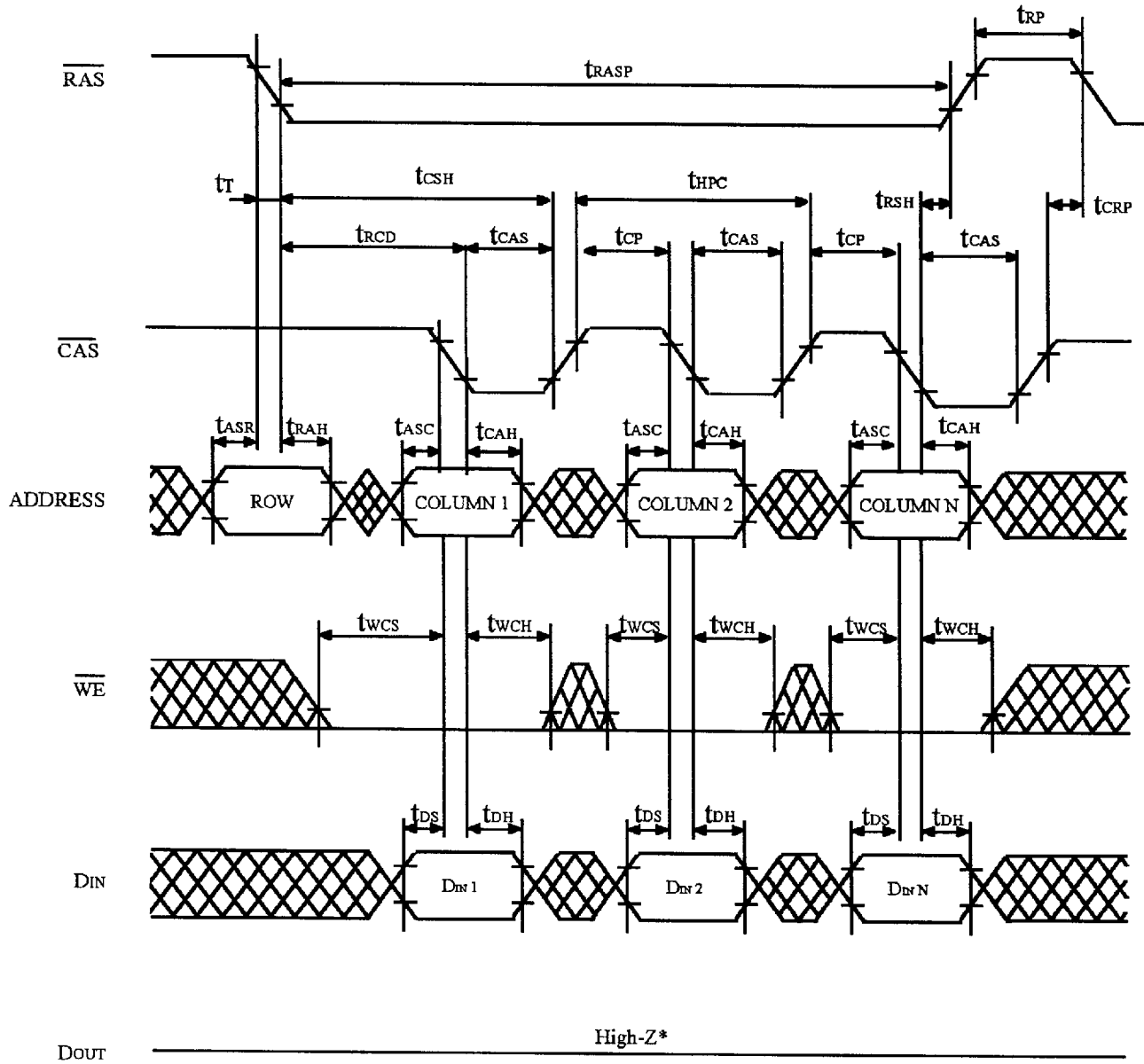


FIGURE 6. EXTENDED DATA OUT MODE READ CYCLE



* $tw_{CS} \geq tw_{CS}(\text{min})$

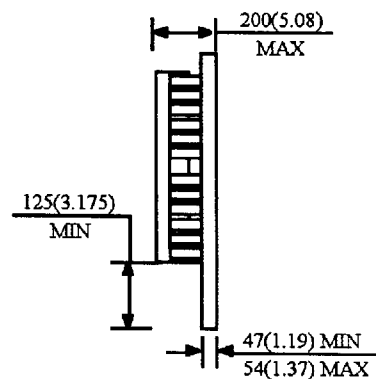
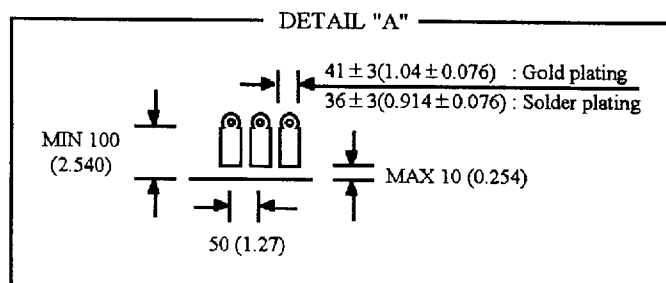
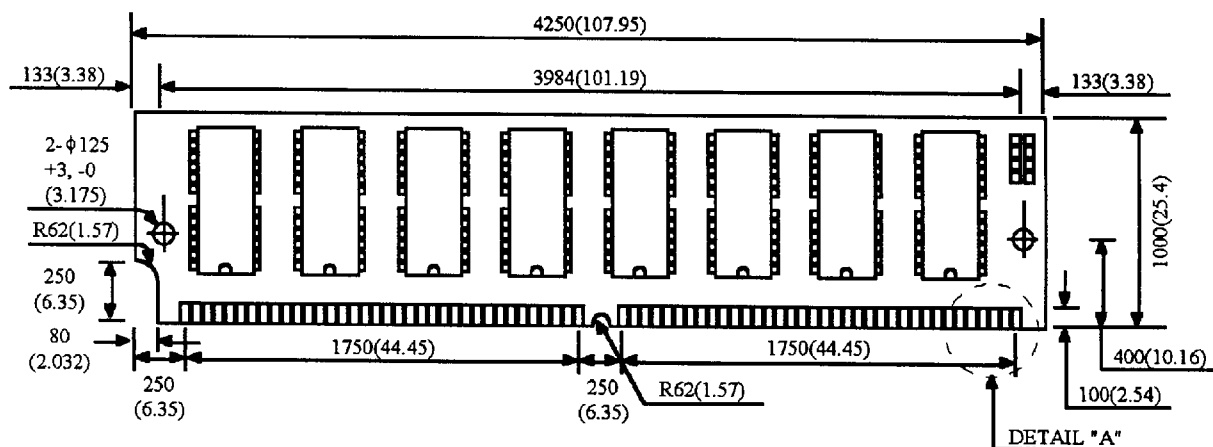
**  : Don't care

FIGURE 7. EXTENDED DATA OUT MODE EARLY WRITE CYCLE

Package Dimension

Unit: mil (mm)

* (1mil = 1/1000 inches)



Tolerances : ± 5 (0.127) unless otherwise specified.