National Semiconductor

NM24C65/C65L/C65LZ/C65XLZ 65,536-Bit Serial EEPROM with Write Protect (I2C Synchronous 2-Wire Bus)

General Description

The NM24C65/C65L/C65LZ/C65XLZ devices are 65,536 bits of CMOS nonvolatile electrically erasable memory. These devices offer the designer different low voltage and low power options, and they conform to all specifications in the I2C 2-wire protocol. Furthermore, they are designed to minimize device pin count and simplify PC board layout requirements.

The upper half of the memory can be disabled (Write Protection) by connecting the WP pin to V_{CC}. This section of memory then becomes ROM.

This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s).

National EEPROMs are designed and tested for applications requiring high endurance, high reliability, and low power consumption.

Features

- Extended Operating Voltages
  C65: 4.5V–5.5V
  C65L: 2.7V–5.5V
  C65LZ: 2.7V–5.5V
  C65XLZ: 1.8V–5.5V
- Low Power CMOS
  2 mA active current typical
  C65/C65L: 60 μA standby current typical
  C65LZ/C65XLZ: less than 1 μA standby current
- 2-wire I2C serial interface
- 32 byte page write mode
- Max write cycle time of 5 ms byte/page
- 40 years data retention
- Endurance: 10^6 data changes
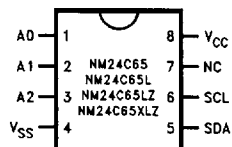- Packages available: 8-pin SO, 8-pin DIP

Block Diagram

TL/D/12521–1

6501126 0074722 105
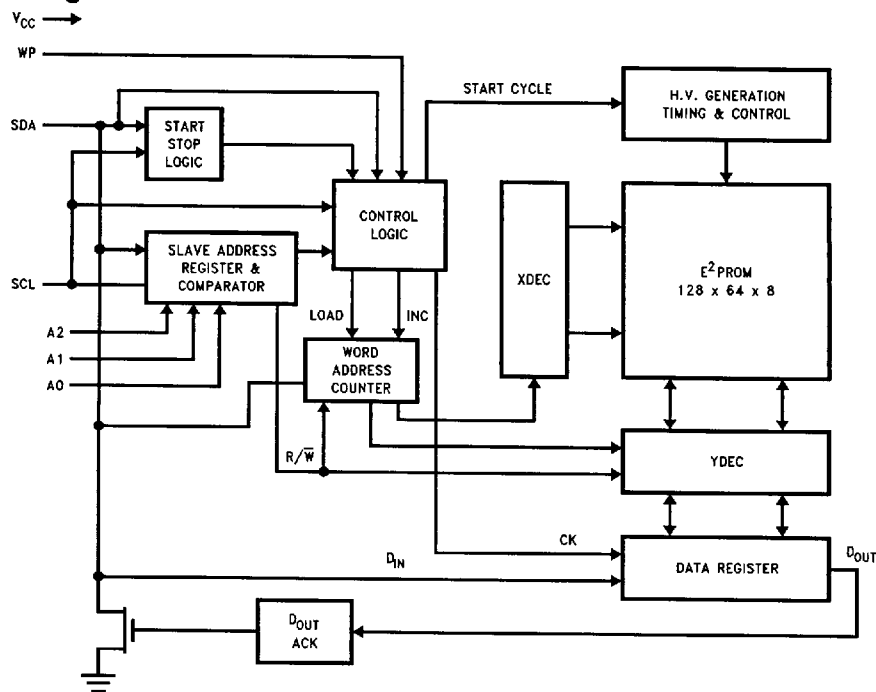
Connection Diagram

Dual-In-Line Package (N)
and 8-Pin SO Package (M8)

```
        ┌───┬───┐
A0 ──│1      8│── V_CC
A1 ──│2      7│── NC
     │ NM24C65 │
     │ NM24C65L│
A2 ──│3 NM24C65LZ 6│── SCL
     │ NM24C65XLZ│
V_SS──│4      5│── SDA
        └───────┘
```

TL/D/12521-2

Top View
See NS Package Number
N08E and M08A

Pin Names

A0, A1, A2	Device Address Input
V_SS	Ground
SDA	Data I/O
SCL	Clock Input
WP	Write Protect
V_CC	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM24C65N/NM24C65LN/ NM24C65LZN/NM24C65XLZN
NM24C65M8/NM24C65LM8/ NM24C65LZM8/NM24C65XLZM8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM24C65EN/NM24C65LEN/ NM24C65LZEN/NM24C65XLZEN
NM24C65EM8/NM24C65LEM8/ NM24C65LZEM8/NM24C65XLZEM8

Extra Low Power (1.8V ≤ V_{CC} < 5.5V) Specifications

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltage with Respect to Ground	V_{CC} + 1 to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM24C65XLZ	0°C to +70°C
NM24C65XLZE	−40°C to +85°C
Power Supply (V_{CC}) Range	1.8V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 1.8V to 5.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ (Note 1)	Max	Units
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 KHz		2	3	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		1	2	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	μA
V_{IL}	Input Low Voltage		−0.3		V_{CC} × 0.3	V
V_{IH}	Input High Voltage		V_{CC} × 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.2	V

Capacitance

T_A = +25°C, f = 1 MHz, V_{CC} = 5V (Note 2)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		8	pF
C_{IN}	Input Capacitance		6	pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.1 V_{CC} to 0.9 V_{CC}
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

Low Power (2.7V ≤ V_{CC} < 5.5V) Specifications

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	$-65°C$ to $+150°C$
All Input or Output Voltage with Respect to Ground	$V_{CC} + 1$ to $-0.3V$
Lead Temperature (Soldering, 10 sec.)	$+300°C$
ESD Rating	2000V

Operating Range

Ambient Operating Temperature	
NM24C65LZ	$0°C$ to $+70°C$
NM24C65LZE	$-40°C$ to $+85°C$
Power Supply (V_{CC}) Range	2.7V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 2.7V to 5.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ (Note 1)	Max	Units
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 KHz		2	3	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		1	2	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	μA
V_{IL}	Input Low Voltage		-0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance
T_A = $+25°C$, f = 1 MHz, V_{CC} = 5V (Note 2)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		8	pF
C_{IN}	Input Capacitance		6	pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).
Note 2: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.1 V_{CC} to 0.9 V_{CC}
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

Low Voltage (2.7V ≤ V_{CC} < 5.5V) Specifications

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltage with Respect to Ground	V_{CC} + 1 to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature
NM24C65L	0°C to +70°C
NM24C65LE	−40°C to +85°C
Power Supply (V_{CC}) Range	2.7V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 2.7V to 5.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 KHz		2	3	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance
T_A = +25°C, f = 1 MHz, V_{CC} = 5V (Note 2)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		8	pF
C_{IN}	Input Capacitance		6	pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.1 V_{CC} to 0.9 V_{CC}
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

Standard Voltage (4.5V ≤ V_{CC} ≤ 5.5V) Specifications

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltage with Respect to Ground	V_{CC} + 1 to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Range

Ambient Operating Temperature

NM24C65	0°C to +70°C
NM24C65E	−40°C to +85°C
Power Supply (V_{CC}) Range	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ (Note 1)	Max	Units
I_{CCA}	Active Power Supply Current	f_{SCL} = 400 KHz		2	3	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		V_{CC} × 0.3	V
V_{IH}	Input High Voltage		V_{CC} × 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance

T_A = +25°C, f = 1 MHz, V_{CC} = 5V (Note 2)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		8	pF
C_{IN}	Input Capacitance		6	pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.1 V_{CC} to 0.9 V_{CC}
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

Extra Low Power (1.8V ≤ V_{CC} < 5.5V) Specifications

READ AND WRITE CYCLE LIMITS

Symbol	Parameter	Conditions	Min	Max	Units
f_{SCL}	SCL Clock Frequency	V_{CC} < 4.5V V_{CC} ≥ 4.5V		100 400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs	V_{CC} < 4.5V V_{CC} ≥ 4.5V		100 50	ns
t_{AA}	SCL Low to SDA Data Out Valid	V_{CC} < 4.5V V_{CC} ≥ 4.5V	0.3 0.3	3.5 0.9	µs
t_{BUF}	Time The Bus Must Be Free Before A New Transmission Can Start	V_{CC} < 4.5V V_{CC} ≥ 4.5V	4.7 1.3		µs
$t_{HD:STA}$	Start Condition Hold Time	V_{CC} < 4.5V V_{CC} ≥ 4.5V	4.0 0.6		µs
t_{LOW}	Clock Low Period	V_{CC} < 4.5V V_{CC} ≥ 4.5V	4.7 1.3		µs
t_{HIGH}	Clock High Period	V_{CC} < 4.5V V_{CC} ≥ 4.5V	4.0 0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	V_{CC} < 4.5V V_{CC} ≥ 4.5V	4.7 0.6		µs
$t_{HD:DAT}$	Data in Hold Time		0		µs
$t_{SU:DAT}$	Data in Setup Time		250		ns
t_R	SDA and SCL Rise Time	V_{CC} < 4.5V V_{CC} ≥ 4.5V		1.0 0.1	µs
t_F	SDA and SCL Fall Time			300	ns
$t_{SU:STO}$	Stop Condition Setup Time	V_{CC} < 4.5V V_{CC} ≥ 4.5V	4.7 0.6		µs
t_{DH}	Data Out Hold Time		300		ns
t_{WR}	Write Cycle Time			5	ms

Low Power (2.7V $\leq$ V$_{CC}$ < 5.5V) Specifications
READ AND WRITE CYCLE LIMITS

Symbol	Parameter	Conditions	Min	Max	Units
f$_{SCL}$	SCL Clock Frequency	V$_{CC}$ < 4.5V V$_{CC}$ $\geq$ 4.5V		100 400	KHz
T$_I$	Noise Suppression Time Constant at SCL, SDA Inputs	V$_{CC}$ < 4.5V V$_{CC}$ $\geq$ 4.5V		100 50	ns
t$_{AA}$	SCL Low to SDA Data Out Valid	V$_{CC}$ < 4.5V V$_{CC}$ $\geq$ 4.5V	0.3 0.3	3.5 0.9	μs
t$_{BUF}$	Time The Bus Must Be Free Before A New Transmission Can Start	V$_{CC}$ < 4.5V V$_{CC}$ $\geq$ 4.5V	4.7 1.3		μs
t$_{HD:STA}$	Start Condition Hold Time	V$_{CC}$ < 4.5V V$_{CC}$ $\geq$ 4.5V	4.0 0.6		μs
t$_{LOW}$	Clock Low Period	V$_{CC}$ < 4.5V V$_{CC}$ $\geq$ 4.5V	4.7 1.3		μs
t$_{HIGH}$	Clock High Period	V$_{CC}$ < 4.5V V$_{CC}$ $\geq$ 4.5V	4.0 0.6		μs
t$_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	V$_{CC}$ < 4.5V V$_{CC}$ $\geq$ 4.5V	4.7 0.6		μs
t$_{HD:DAT}$	Data in Hold Time		0		μs
t$_{SU:DAT}$	Data in Setup Time		250		ns
t$_R$	SDA and SCL Rise Time	V$_{CC}$ < 4.5V V$_{CC}$ $\geq$ 4.5V		1.0 0.1	μs
t$_F$	SDA and SCL Fall Time			300	ns
t$_{SU:STO}$	Stop Condition Setup Time	V$_{CC}$ < 4.5V V$_{CC}$ $\geq$ 4.5V	4.7 0.6		μs
t$_{DH}$	Data Out Hold Time		300		ns
t$_{WR}$	Write Cycle Time			5	ms

Low Voltage (2.7V ≤ V$_{CC}$ < 5.5V) Specifications

READ AND WRITE CYCLE LIMITS

Symbol	Parameter	Conditions	Min	Max	Units
f$_{SCL}$	SCL Clock Frequency	V$_{CC}$ < 4.5V V$_{CC}$ ≥ 4.5V		100 400	KHz
T$_I$	Noise Suppression Time Constant at SCL, SDA Inputs	V$_{CC}$ < 4.5V V$_{CC}$ ≥ 4.5V		100 50	ns
t$_{AA}$	SCL Low to SDA Data Out Valid	V$_{CC}$ < 4.5V V$_{CC}$ ≥ 4.5V	0.3 0.3	3.5 0.9	μs
t$_{BUF}$	Time The Bus Must Be Free Before A New Transmission Can Start	V$_{CC}$ < 4.5V V$_{CC}$ ≥ 4.5V	4.7 1.3		μs
t$_{HD:STA}$	Start Condition Hold Time	V$_{CC}$ < 4.5V V$_{CC}$ ≥ 4.5V	4.0 0.6		μs
t$_{LOW}$	Clock Low Period	V$_{CC}$ < 4.5V V$_{CC}$ ≥ 4.5V	4.7 1.3		μs
t$_{HIGH}$	Clock High Period	V$_{CC}$ < 4.5V V$_{CC}$ ≥ 4.5V	4.0 0.6		μs
t$_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	V$_{CC}$ < 4.5V V$_{CC}$ ≥ 4.5V	4.7 0.6		μs
t$_{HD:DAT}$	Data in Hold Time		0		μs
t$_{SU:DAT}$	Data in Setup Time		250		ns
t$_R$	SDA and SCL Rise Time	V$_{CC}$ < 4.5V V$_{CC}$ ≥ 4.5V		1.0 0.1	μs
t$_F$	SDA and SCL Fall Time			300	ns
t$_{SU:STO}$	Stop Condition Setup Time	V$_{CC}$ < 4.5V V$_{CC}$ ≥ 4.5V	4.7 0.6		μs
t$_{DH}$	Data Out Hold Time		300		ns
t$_{WR}$	Write Cycle Time			5	ms

Standard Voltage (4.5V ≤ V$_{CC}$ ≤ 5.5V) Specifications

READ AND WRITE CYCLE LIMITS

Symbol	Parameter	Conditions	Min	Max	Units
f$_{SCL}$	SCL Clock Frequency			400	KHz
T$_I$	Noise Suppression Time Constant at SCL, SDA Inputs			50	ns
t$_{AA}$	SCL Low to SDA Data Out Valid		0.3	0.9	μs
t$_{BUF}$	Time The Bus Must Be Free Before A New Transmission Can Start		1.3		μs
t$_{HD:STA}$	Start Condition Hold Time		0.6		
t$_{LOW}$	Clock Low Period		1.3		μs
t$_{HIGH}$	Clock High Period		0.6		μs
t$_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)		0.6		μs
t$_{HD:DAT}$	Data in Hold Time		0		μs
t$_{SU:DAT}$	Data in Setup Time		250		ns
t$_R$	SDA and SCL Rise Time			0.1	μs
t$_F$	SDA and SCL Fall Time			300	ns
t$_{SU:STO}$	Stop Condition Setup Time		0.6		
t$_{DH}$	Data Out Hold Time		300		ns
t$_{WR}$	Write Cycle Time			5	ms

Bus Timing
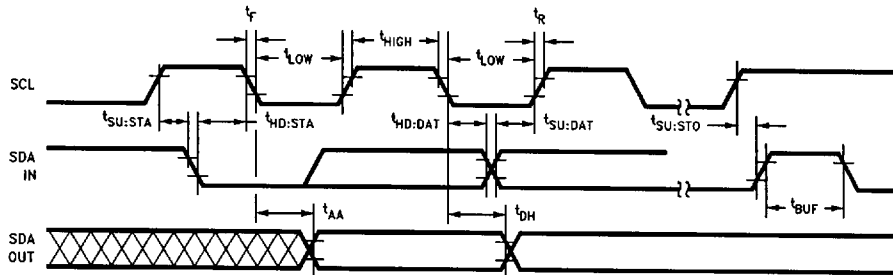
TL/D/12521-3

BACKGROUND INFORMATION (I²C Bus)

As mentioned, the I²C bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the I²C bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string, or control byte, must follow the START condition. For EEPROMs, the first 4-bit of the control byte is 1010 binary for READ and WRITE operations. This is then followed by the device selection bits A2, A1 and A0, and acts as the three most significant bits of the word address. The final bit in the control byte determines the type of operation performed (READ/$\overline{WRITE}$). A "1" signifies a READ while a "0" signifies a WRITE. The control byte is then followed by two bytes that define the word address, which is then followed by the data byte.

The EEPROMs on the I²C bus may be configured in any manner required, providing the total memory addressed does not exceed 512 Kbits (64 Kbytes). EEPROM memory addressing is controlled by hardware configuring the A2, A1, and A0 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (tied to V_{SS}).

Pin Description

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

Device Address Inputs (A0, A1, A2)

Device address pins A0, A1, and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address for multiple device configuration. A total of eight different devices can be attached to the same SDA bus.

Write Protection (WP)

If WP is tied to V_{CC}, program WRITE operations onto the upper half of the memory (32 Kbits) will not be executed. READ operations are always available.

If WP is tied to V_{SS}, normal memory operation is enabled, READ/WRITE over the entire 64 Kbit memory array.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming writes. When WRITE is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Definitions	
Word	8 bits (byte) of data
Page	32 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
Master	Any I²C device CONTROLLING the transfer of data (such as a microcontroller).
Slave	Device being controlled (EEPROMs are always considered Slaves)
Transmitter	Device currently SENDING data on the bus (may be either a Master or Slave)
Receiver	Device currently receiving data on the bus (Master or Slave)

Device Operation

The NM24C65xxx supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving devices as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C64xxx is considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH and reserved for indication start and stop conditions. Refer to *Figures 1 and 2*.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C65xxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C65xxx to place the device in the standby power mode.

## Device Operation (Continued)

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The NM24C65xxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the NM24C65xxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the READ mode the NM24C65xxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Write Cycle Timing
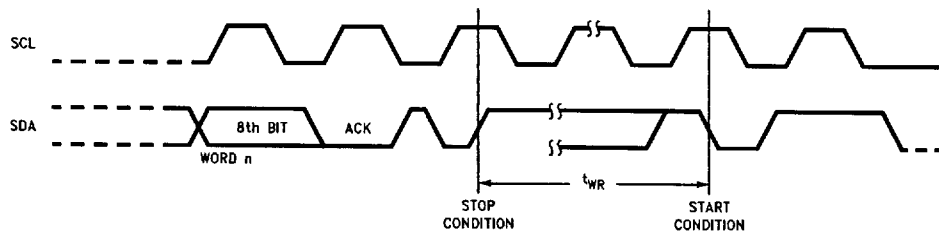
TL/D/12521-4
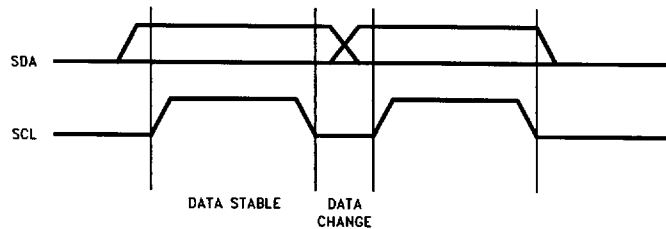
TL/D/12521-5

FIGURE 1. Data Validity
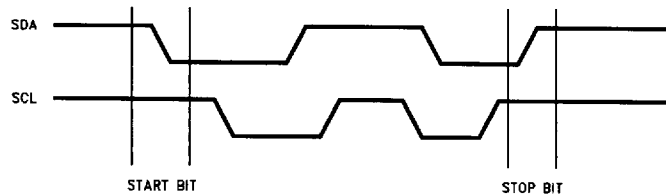
TL/D/12521-6

FIGURE 2. Definition of Start and Stop

Write Cycle Timing (Continued)
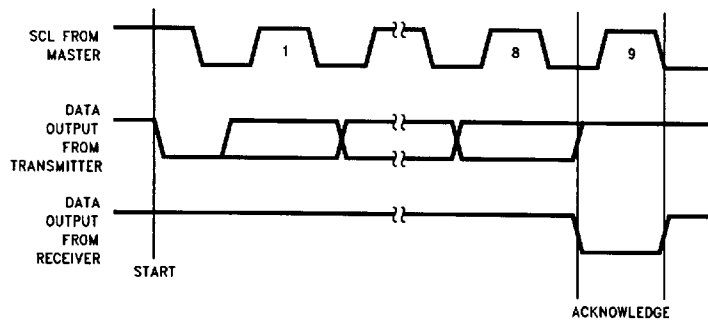
FIGURE 3. Acknowledge Response from Receiver

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Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier. This is fixed as 1010 for all four devices: NM24C65, NM24C65L, NM24C65LZ and NM24C65XLZ.

The next three bits identifies the device address. Address from 000 to 111 are acceptable thus allowing up to eight devices to be connected to the I2C bus.

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a READ operation is to be executed and a "0" initiates the WRITE mode.

A simple review: After the NM24C65xxx recognizes the start condition, the devices interfaced to the I2C bus waits for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge. signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a WRITE operation, two additional address fields are required after the control byte acknowledge which is the word address and is comprised of thirteen bits to provide access to any one of the 8k words in the selected page of memory. The first byte indicates the high-order byte of the word address.

Only the five least significant bits can be changed, the three most significant bits are pre-assigned the value "0". Following the acknowledgment from the first word address, the next byte indicates the low-order byte of the word address. Upon receipt of the word address, the NM24C65xxx responds with another acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24C65xxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress, the device's inputs are disabled and the device will not respond to any requests from the master. Refer to *Figure 4* for the address, acknowledge and data transfer sequence.

PAGE WRITE

The NM24C65xxx is capable of thirty-two byte page write operation. It is initiated in the same manner as the byte write operation; but instead of termination the write cycle after the first data word is transferred, the master can transmit up to thirty-one more words.

After the receipt of each word, the device responds with an acknowledge. After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than thirty-two words prior to generating the stop condition, the address counter will "roll over" and the previous written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.
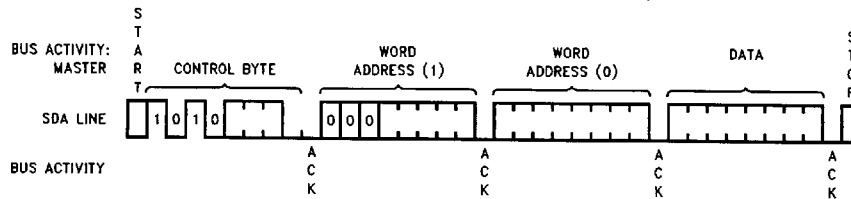

FIGURE 4. Byte Write

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Acknowledge Polling

Once the stop condition is issued to indicate the end of the host's write operation, the NM24C65xxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24C65xxx is still busy with the write operation, no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

Write Protection

Programming of the upper half of memory will not take place if the WP pin is connected to V_{CC} (+5V). The device will accept control and word addresses; but if the memory accessed is write protected by the WP pin, the NM24C65xxx will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Read Operation

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to "1". There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24C65xxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24C65xxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate

a stop condition, and therefore discontinues transmission. Refer to *Figure 6* for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to "1", the master must first perform a "dummy" write operation. The master issues a start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to "1". This will be followed by an acknowledge from the NM24C65xxx and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C65xxx discontinues transmission. Refer to *Figure 7* for the address, acknowledge and data transfer sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C65xxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24C65xxx continues to output data for each acknowledge received. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.
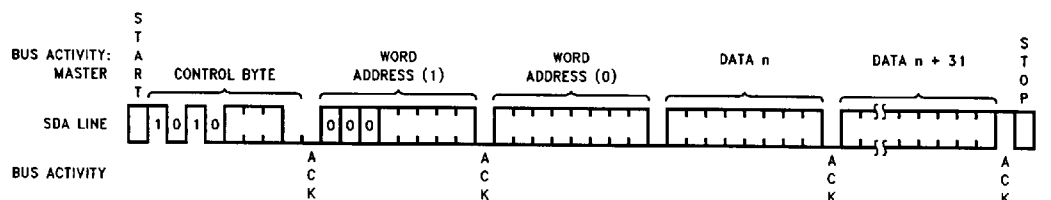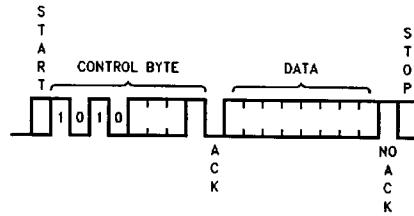

FIGURE 5. Page Write

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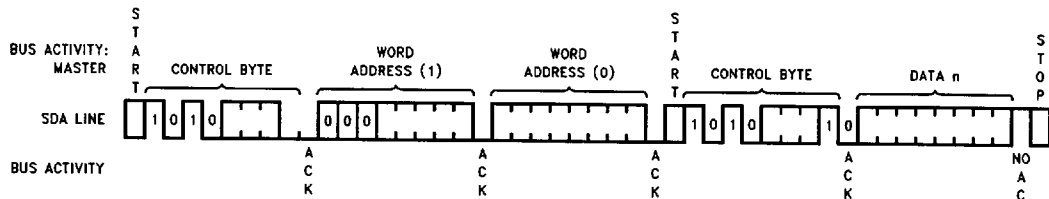**FIGURE 6. Current Address Read**

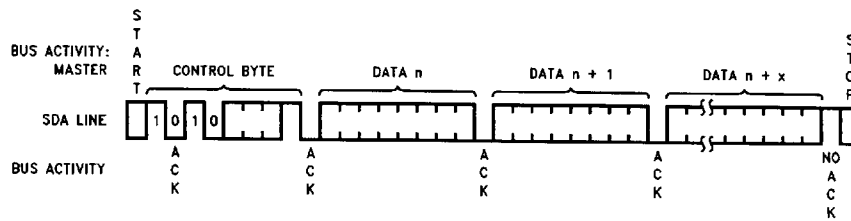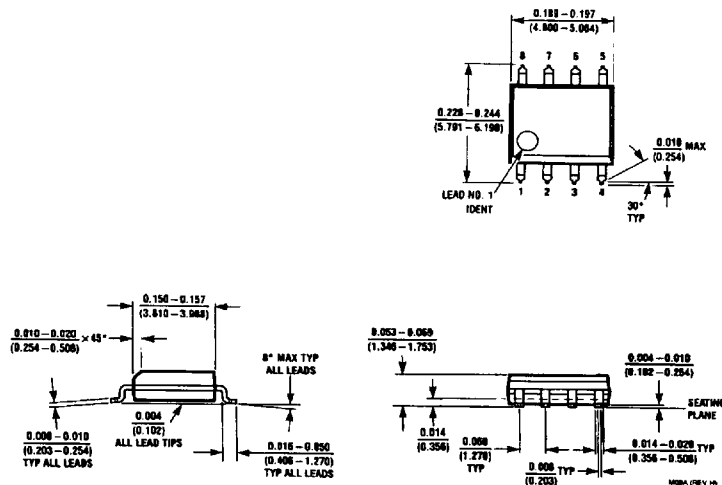TL/D/12521–10

FIGURE 7. Random Read

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FIGURE 8. Sequential Read

TL/D/12521–12

Physical Dimensions inches (millimeters)

Molded Small Out-Line Package (M8)
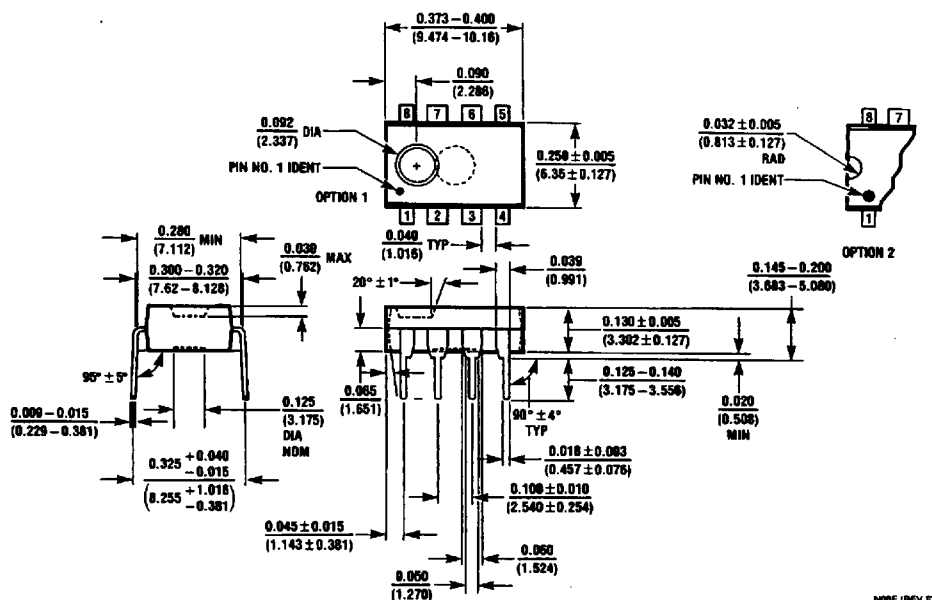Order Number NM24C65xxxM8 or NM24C65xxxEM8
NS Package Number M08A

/ 6

Physical Dimensions inches (millimeters) (Continued)

Molded Dual-In-Line Package (N)
Order Number NM24C65xxxN or NM24C65xxxEN
NS Package Number N08E

LIFE SUPPORT POLICY

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