National Semiconductor

NM25C160
16,384-Bit Serial CMOS EEPROM
(Serial Peripheral Interface (SPI™) Synchronous Bus)

General Description

The NM25C160 is a 16,384-bit CMOS EEPROM with a SPI compatible serial interface. The NM25C160 is designed for data storage in applications requiring both non-volatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI interface for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C160 is implemented in National Semiconductor's Floating gate CMOS process that provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select ($\overline{CS}$), Clock (SCK), Serial Data In (SI), and Serial Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

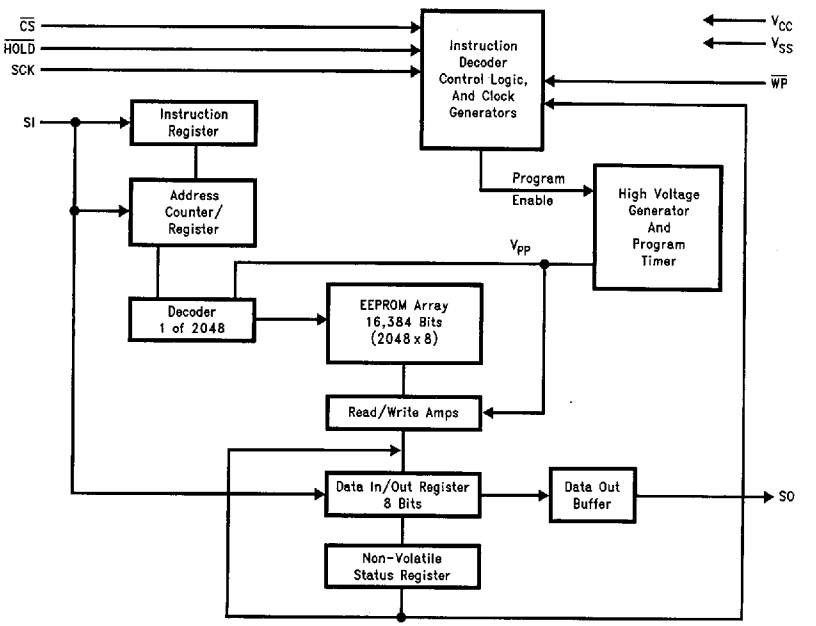
BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally, separate write enable and write disable instructions are provided for data protection.

Hardware data protection is provided by the $\overline{WP}$ pin to protect against accidental data changes. The $\overline{HOLD}$ pin allows the serial communication to be suspended without resetting the serial sequence.

Features

- 2.1 MHz clock rate
- 16,384 bits organized as 2048 x 8
- Multiple chips on the same 3-wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 16 bytes at a time
- Status register can be polled during programming to monitor RDY/BUSY
- Write Protect ($\overline{WP}$) pin and write disable instruction for both hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP or 8-pin SO

Block Diagram



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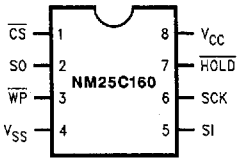
Connection Diagram

Dual-In-Line Package (N)
and SO Package (M8)



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Top View

See NS Package Number N08E (N) and M08A (M8)

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Input
V_{CC}	Power Supply

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM25C160N/M8 NM25C160LN/LM8/LZN/LZM8

Extended Temperature Range (−40°C to +85°C)

Order Number
NM25C160EN/EM8 NM25C160LEN/LEM8/LZEN/LZEM8

Automotive Temperature Range (−40°C to +125°C)

Order Number
NM25C160VN/VM8 NM25C160LVN/LVM8/LZVN/LZVM8

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Standard Voltage 4.5 ≤ V_{CC} ≤ 5.5V Specifications

Absolute Maximum Ratings 5V (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C160	0°C to +70°C
NM25C160E	−40°C to +85°C
NM25C160V	−40°C to +125°C
Power Supply (V_{CC})	4.5V–5.5V

DC and AC Electrical Characteristics 4.5V ≤ V_{CC} ≤ 5.5V unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC}	Operating Current		$\overline{CS}$ = V_{IL}		3	mA
I_{CCSB}	Standby Current		$\overline{CS}$ = V_{CC}		50	μA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC}	−1	+1	μA
I_{OL}	Output Low Leakage		V_{IN} = 0V to V_{CC}	−1	+1	μA
V_{IL}	Input Low Voltage			−0.3	0.3*V_{CC}	V
V_{IH}	Input High Voltage			0.7*V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage		I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High Voltage		I_{OH} = −0.8 mA	V_{CC} − 0.8		V
f_{OP}	SCK Frequency	NM25C160			2.1	MHz
t_{RI}	Input Rise Time				2.0	μs
t_{FI}	Input Fall Time				2.0	μs
t_{CLH}	Clock High Time	NM25C160	(Note 2)	190		ns
t_{CLL}	Clock Low Time	NM25C160	(Note 2)	190		V
t_{CSH}	Min $\overline{CS}$ High Time	NM25C160	(Note 3)	240		ns
t_{CSS}	$\overline{CS}$ Setup Time	NM25C160		240		ns
t_{DIS}	Data Setup Time			100		ns

DC and AC Electrical Characteristics $4.5V \le V_{CC} \le 5.5V$ unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{HDS}	$\overline{HOLD}$ Setup Time			90		ns
t_{CSN}	$\overline{CS}$ Hold Time	NM25C160		240		ns
t_{DIN}	Data Hold Time			100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time			90		ns
t_{PD}	Output Delay	NM25C160	C_L = 200 pF		240	ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z	NM25C160			240	ns
t_{DF}	Output Disable Time	NM25C160	C_L = 200 pF		240	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z	NM25C160			240	ns
t_{WP}	Write Cycle Time		1–16 Bytes		10	ms

Capacitance T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} – 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} – 0.7 * V_{CC}

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SCK frequency specification specifies a minimum clock period of 476 ns; therefore, in an SCK clock cycle, $t_{CLH} + t_{CLL}$ must be greater than or equal to 476 ns. For example, if t_{CLL} = 190 ns, then the minimum t_{CLH} = 286 ns in order to meet the SCK frequency specification.

Note 3: $\overline{CS}$ must be brought high for a minimum of 240 ns (t_{CSH}) between consecutive instruction cycles.

Low Voltage 2.7V ≤ V_{CC} ≤ 5.5V Specifications

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C160L	0°C to +70°C
NM25C160LE	−40°C to +85°C
NM25C160LV	−40°C to +125°C
Power Supply (V_{CC})	2.7V–5.5V

DC and AC Electrical Characteristics 2.7V ≤ V_{CC} ≤ 5.5V unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC}	Operating Current		$\overline{CS}$ = V_{IL}		3	mA
I_{CCSB}	Standby Current	L LZ	$\overline{CS}$ = V_{CC}		10 1	µA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC}	−1	+1	µA
I_{OL}	Output Leakage		V_{OUT} = 0V to V_{CC}	−1	+1	µA
V_{IL}	Input Low Voltage			−0.3	0.3*V_{CC}	µA
V_{IH}	Input High Voltage			0.7*V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	NM25C160L	I_{OL} = 1.6 µA		0.2*V_{CC}	V
V_{OH}	Output High Voltage		I_{OH} = −0.8 µA	V_{CC} − 0.8		V
f_{OP}	SCK Frequency				1	MHz
t_{RI}	Input Rise Time				2.0	µs
t_{FI}	Input Fall Time				2.0	µs
t_{CLH}	Clock High Time		(Note 2)	410		ns
t_{CLL}	Clock Low Time		(Note 2)	410		ns
t_{CSH}	Minimum $\overline{CS}$ High Time		(Note 3)	500		ns
t_{CSS}	$\overline{CS}$ Setup Time			500		ns
t_{DIS}	Data Setup Time			100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time			240		ns
t_{CSN}	$\overline{CS}$ Hold Time			500		ns
t_{DIN}	Data Hold Time			100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time			240		ns
t_{PD}	Output Delay		C_L = 200 pF		500	ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z				240	ns
t_{DF}	Output Disable Time		C_L = 200 pF		500	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z				240	ns
t_{WP}	Write Cycle Time		1–16 Bytes		15	ms

Capacitance $T_A = 25°C, f = 1\ MHz$

Symbol	Test	Type	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	$I_{OL} = 10\ \mu A$, $I_{OH} = 10\ \mu A$
Input Pulse Levels	$0.1 * V_{CC} - 0.9 * V_{CC}$
Timing Measurement Reference Level	$0.3 * V_{CC} - 0.7 * V_{CC}$

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SCK frequency specification specifies a minimum clock period of 1000 ns; therefore, in an SCK clock cycle, $t_{CLH} + t_{CLL}$ must be greater than or equal to 1000 ns. For example, if $t_{CLL} = 410$ ns, then the minimum $t_{CLH} = 590$ ns in order to meet the SCK frequency specification.

Note 3: $\overline{CS}$ must be brought high for a minimum of 500 ns (t_{CSH}) between consecutive instruction cycles.

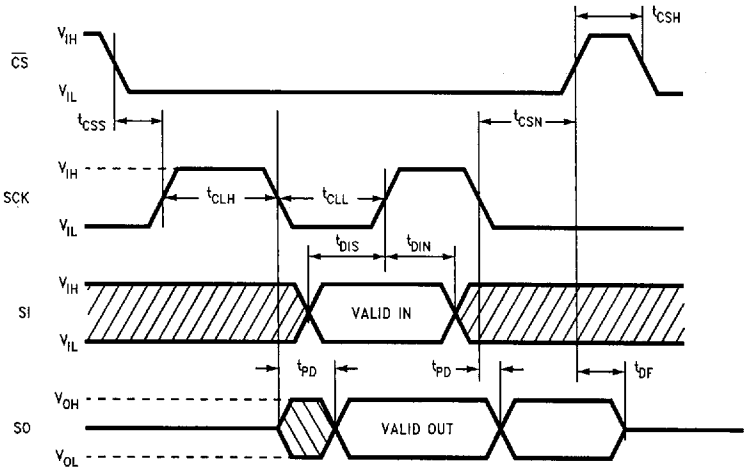

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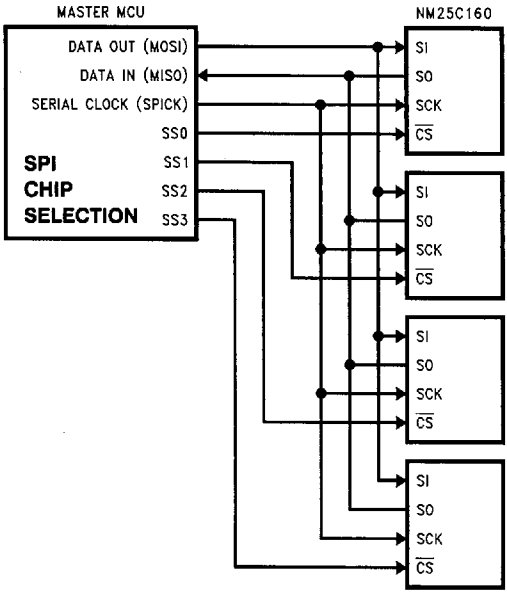
FIGURE 1. Synchronous Data Timing Diagram



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Note: When connected to the SFI port of a 68HC11 microcontroller, the NM25C160 accepts a clock phase of 0 and 9 clock polarity of 0.

FIGURE 2. SPI Serial Interface

Functional Description

MASTER: The device that generates the serial clock is designated as the master. The NM25C160 can never function as a master.

SLAVE: The NM25C160 always operates as a slave as the serial clock pin is always an input.

TRANSMITTER/RECEIVER: The NM25C16 has separate pins for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin $\overline{CS}$ is low. When the chip is *not* selected, data will not be accepted from pin SI, and the output pin SO is in high impedance.

SERIAL OP-CODE: The first byte transmitted after the chip is selected with $\overline{CS}$ going low contains the op-code that defines the operation to be performed.

PROTOCOL: When connected to the SPI port of a 68HC11 microcontroller, the NM25C160 accepts a clock phase of 0 and a clock polarity of 0. The SPI protocol for this device defines the byte transmitted on the SI and SO data lines for proper chip operation. See *Figure 3*.

Data is clocked in on the positive SCK edge and out on the negative SCK edge.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ to select the device. Once the device is selected and a serial sequence is underway, $\overline{HOLD}$ may be forced low to suspend further serial communication with the device without resetting the serial sequence. Note that $\overline{HOLD}$ must be brought low while the SCK pin is low. The device must remain selected during this sequence. To resume serial communication $\overline{HOLD}$ is brought high while the SCK pin is low. Pins SI, SCK and SO are at a high impedance state during $\overline{HOLD}$. See *Figure 4*.

INVALID OP-CODE: After an invalid code is received, no data is shifted into the NM25C160, and the SO data output pin remains high impedance until a new $\overline{CS}$ falling edge reinitializes the serial communication. See *Figure 5*.

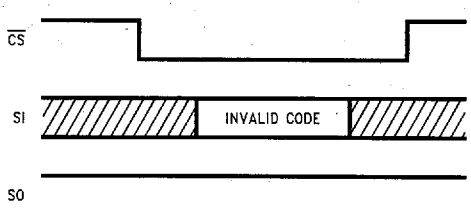

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FIGURE 5. Invalid Op-Code

TABLE I

Instruction Name	Instruction Format	Operation
WREN	00000110	Set Write Enable Latch
WRDI	00000100	Reset Write Enable Latch
RDSR	00000101	Read Status Register
WRSR	00000001	Write Status Register
READ	00000011	Read Data from Memory Array
WRITE	00000010	Write Data to Memory Array

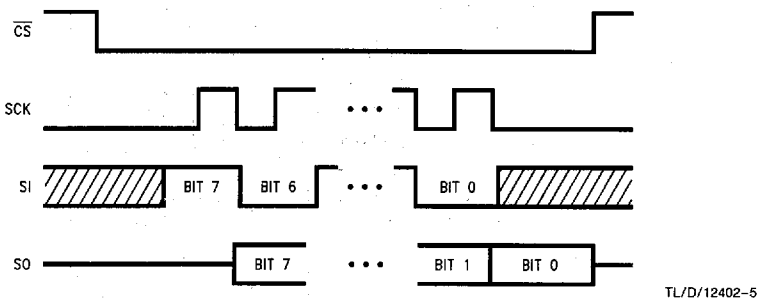

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FIGURE 3. SPI Protocol

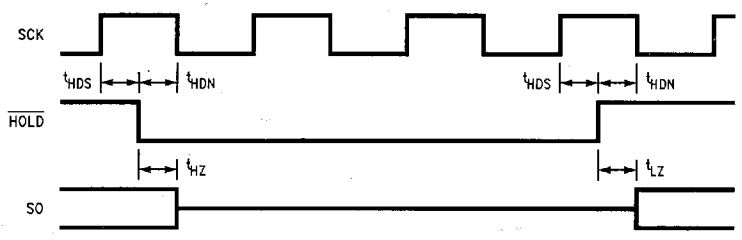

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FIGURE 4. $\overline{HOLD}$ Timing

Functional Description (Continued)

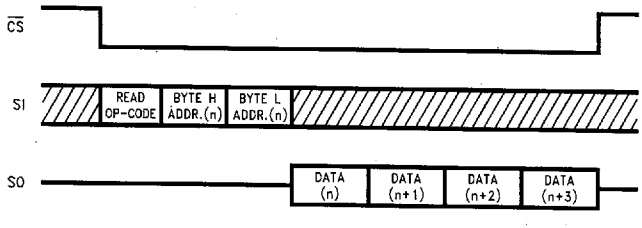

FIGURE 6. Read Sequence

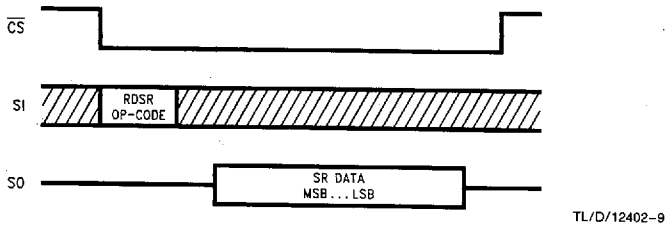

FIGURE 7. Read Status

READ SEQUENCE: (One or More Bytes): Reading the memory via the serial SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code is transmitted on the SI line followed by the high order address byte (A10–A8), and the low order address byte (A7–A0). The leading five bits in the high order address byte will be ignored. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached (7FF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See *Figure 6*.

READ STATUS REGISTER (RDSR): The Read Status Register (RDSR) instruction provides access to the status register which is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION. The status register format is shown in Table II.

TABLE II. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	1	BP1	BP0	WEN	$\overline{RDY}$

Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table III. Note that if a RDSR instruction is executed during a programming cycle only the $\overline{RDY}$ bit is valid. All other bits are 1s. See *Figure 7*.

TABLE III. Block Write Protection Levels

Level	Status Register Bits		Array Address Protected
	BP1	BP0	
0	0	0	None
1	0	1	600–7FF
2	1	0	400–7FF
3	1	1	000–7FF

WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all programming modes must be preceded by a WRITE ENABLE (WREN) instruction. Additionally, the $\overline{WP}$ pin must be held high during a WRITE ENABLE instruction. At the completion of a WRITE or WRSR cycle the device is automatically returned to the write disable state. Note that a WRITE DISABLE (WRDI) instruction will also return the device to the write disable state. The WRITE ENABLE instruction is independent of the status of the $\overline{WP}$ pin. See *Figure 8*.

Functional Description (Continued)

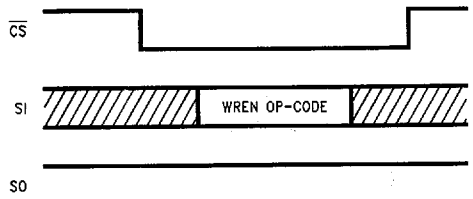

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FIGURE 8. Write Enable

WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. The WRITE DISABLE instruction is independent of the status of the $\overline{WP}$ pin. See *Figure 9*.

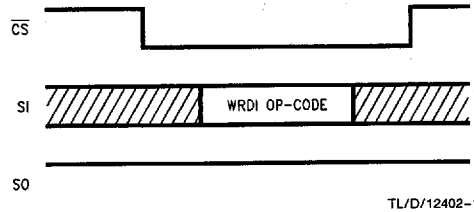

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FIGURE 9. Write Disable

WRITE SEQUENCE: To program the device the WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table III.

A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code is transmitted on the SI line followed by the high order address byte (A10–A8) and the low order address byte (A7–A0). The leading five bits in the high order address byte will be ignored. The address is followed by the data (D7–D0) to be written. Programming will start after the $\overline{CS}$ pin is forced back to a high level. Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. See *Figure 10*.

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

The NM25C160 is capable of a 16 byte PAGE WRITE operation. After receipt of each byte of data the four low order address bits are internally incremented by one. The seven high order bits of the address will remain constant. If the master should transmit more than 16 bytes of data, the address counter will "roll over", and the previously loaded data will be reloaded.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when $\overline{CS}$ is forced high. A new $\overline{CS}$ falling edge is required to re-initialize the serial communication. The WRITE instruction is independent of the status of the $\overline{WP}$ pin. See *Figure 11*.

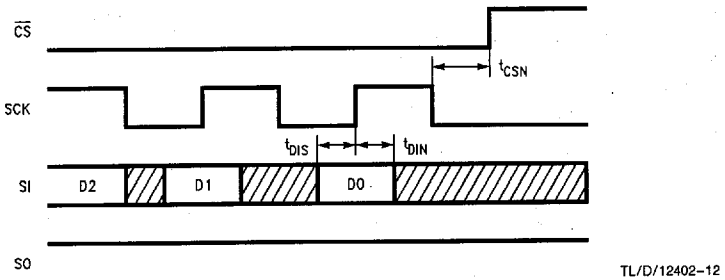

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FIGURE 10. Write Sequence

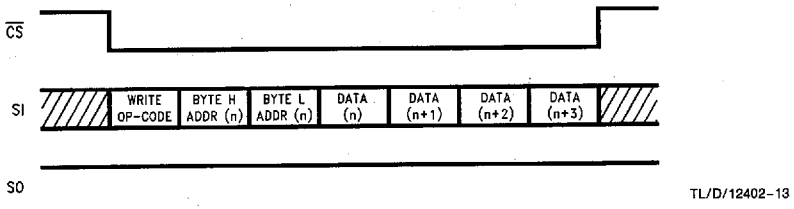

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FIGURE 11. Start Write Condition

Functional Description (Continued)

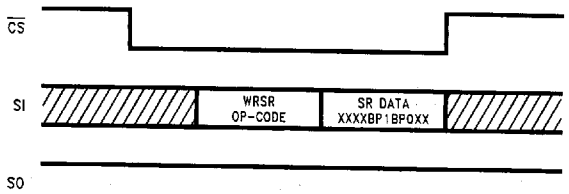

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FIGURE 12. Write Status Register

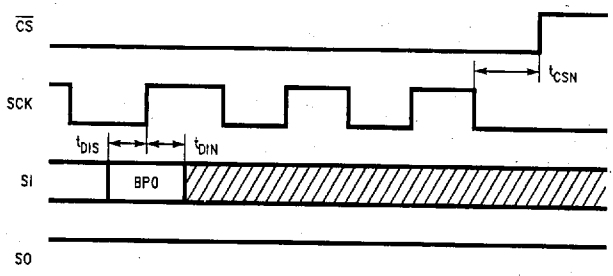

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FIGURE 13. Start WRSR Condition

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and BP1). The WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRSR instruction must be executed.

The WRSR command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed. See *Figure 12*.

Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the $\overline{CS}$ pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the last don't care bit. See *Figure 13*.

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

Functional Description (Continued)

Mode 2: Master Reset

Sequence of Operation

1. Input and Output Ready, HF and FULL can be in any state before the reset sequence with Master Reset ($\overline{MR}$) HIGH.
2. Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width t_{MRW} before rising again.
3. Master Reset rises.
4. IR rises (if not HIGH already) to indicate ready to write state recovery time t_{MRIRH} after the falling edge of $\overline{MR}$. Both HF and FULL will go LOW indicating an empty FIFO, occurring recovery times t_{MRE} and t_{MRO} respectively after the falling edge of $\overline{MR}$. OR falls recovery time t_{MRORL} after $\overline{MR}$ falls. Data at outputs goes LOW recovery time t_{MRONL} after $\overline{MR}$ goes LOW.
5. Shift-In can be taken HIGH after a minimum recovery time t_{MRSIH} after $\overline{MR}$ goes HIGH.

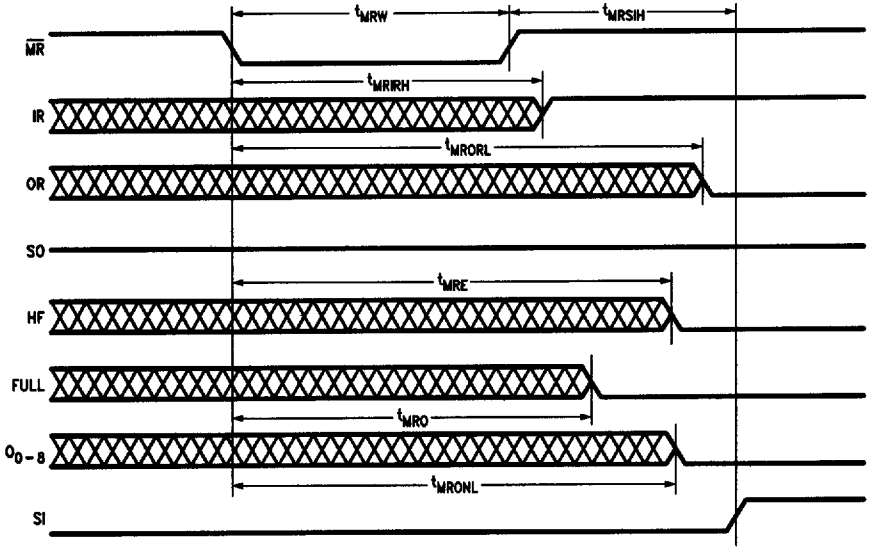

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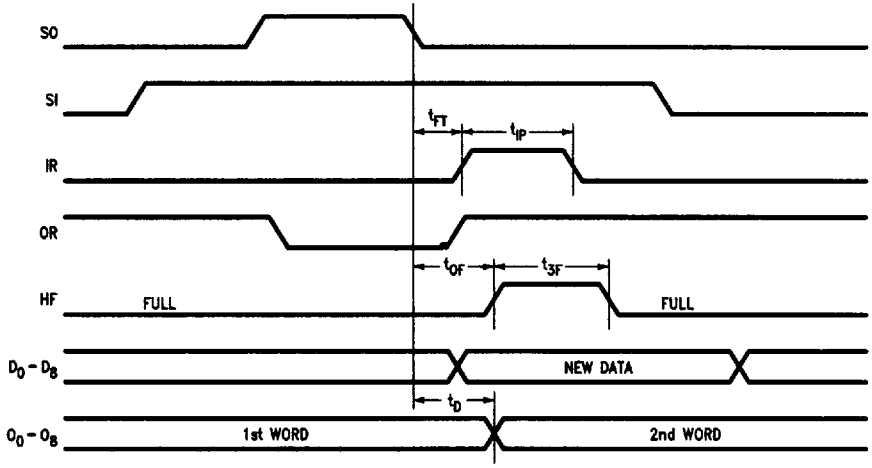
FIGURE 2. Mode of Operation Mode 2

Functional Description (Continued)

Mode 3: With FIFO Full, Shift-In is Held HIGH In Anticipation of an Empty Location

Sequence of Operation

1. The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. Shift-Out is LOW. IR is LOW.
2. Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after propagation delay t_D. New data is written into the FIFO after SO goes LOW.
3. Input Ready goes HIGH one fall-through time, t_{FT}, after the falling edge of SO. Also, HF goes HIGH one t_{OF} after SO falls, indicating that the FIFO is no longer full.
4. IR returns LOW pulse width t_{IP} after rising and shifting new data in. Also, HF returns LOW pulse width t_{3F} after rising, indicating the FIFO is once more full.
5. Shift-In is brought LOW to complete the shift-in process and maintain normal operation



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Note: $\overline{MR}$ and FULL are HIGH; $\overline{OE}$ is LOW.

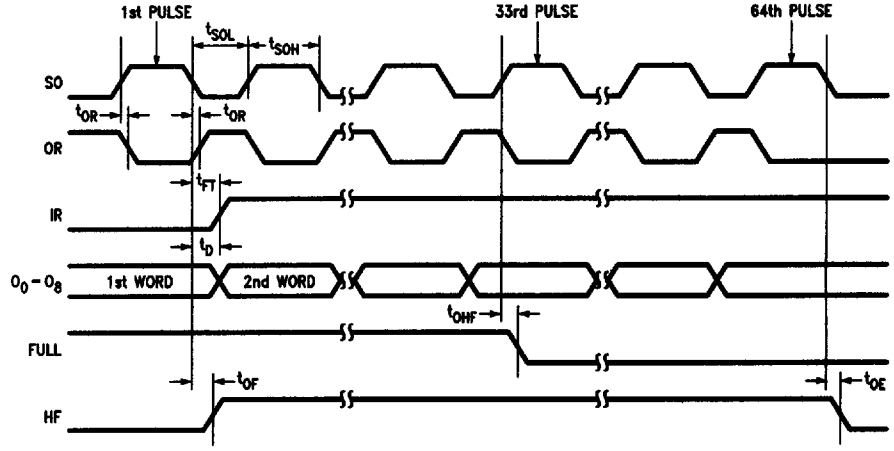
FIGURE 3. Modes of Operation Mode 3

Functional Description (Continued)

Mode 4: Shift-Out Sequence, FIFO Full to Empty

Sequence of Operation

1. FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.
2. SO goes HIGH, resulting in OR going LOW one propagation delay, t_{OR}, after SO rises. OR LOW indicates output stage is busy.
3. SO goes LOW, new data reaches output one propagation delay, t_D, after SO falls; OR goes HIGH one propagation delay, t_{OR}, after SO falls and HF rises one propagation delay, t_{OF}, after SO falls. IR rises one fall-through time, t_{FT}, after SO falls.
4. Repeat process through the 64th SO pulse. FULL flag goes LOW one propagation delay, t_{OHF}, after the rising edge of 33rd SO, indicating that the FIFO is less than half full. On the falling edge of the 64th SO, HF goes LOW one propagation delay, t_{OE}, after SO, indicating the FIFO is empty. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.



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Note: SI and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH; D_0–D_8 are immaterial.

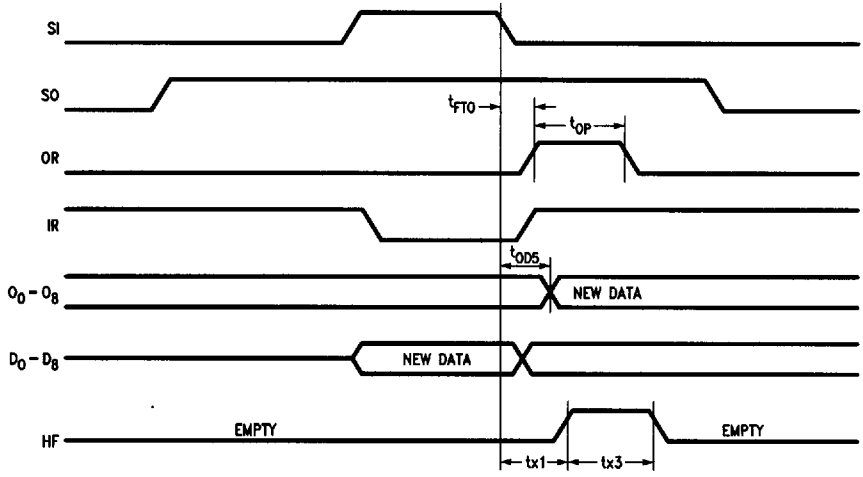
FIGURE 4. Modes of Operation Mode 4

Functional Description (Continued)

Mode 5: With FIFO Empty, Shift-Out is Held HIGH in Anticipation of Data

Sequence of Operation

1. FIFO is initially empty; Shift-Out goes HIGH.
2. Shift-In pulse loads data into the FIFO and IR falls. HF rises propagation delay t_{X1} after the falling edge of SI.
3. OR rises a fall-through time of t_{FTO} after the falling edge of Shift-In, indicating that new data is ready to be output.
4. Data arrives at output one propagation delay, t_{OD5}, after the falling edge of Shift-In.
5. OR goes LOW pulse width t_{OP} after rising and HF goes LOW pulse width t_{X3} after rising, indicating that the FIFO is empty once more.
6. Shift-Out goes LOW, necessary to complete the Shift-Out process.



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Note: FULL is LOW; $\overline{MR}$ is HIGH; $\overline{OE}$ is LOW; $t_{DOF} = t_{FTO} - t_{OD5}$. Data output transition—valid data arrives at output stage t_{DOF} after OR is HIGH.

FIGURE 5. Modes of Operation Mode 5