# GP001A/1RZ

**Advance Information**

T-49-17-51

# CMOS/SOS 8-Bit General Processor Unit (GPU)

Aerospace Class S Screening

**Features:**

- *Fully static operation to 10 MHz*
- *Full military temperature range operation*
- *16 dual-access 8-bit general-purpose registers*
- *8-bit parallel Arithmetic Logic Circuit (ALC)*
- *Expandable*
- *Separate data input and data output*
- *Tri-state outputs*
- *Pipeline operation*

**Radiation Features:**

- *Radiation hardened to 100K rads (Si)*
- *Latch-up free under transient radiation*
- *Resistance to upset under transient radiation rate of up to 1 x $10^{10}$ rads (Si)/sec*

The RCA GP001 is an 8-bit, central-processing-unit bit slice intended for use in CPU's, peripheral controllers, microprogrammable computers, and dedicated controllers. It is a high-speed, low-power CMOS/SOS device that can be cascaded, allowing it to efficiently emulate any computer whose word lengths are in multiples of eight bits.

The performance of the GP001 is the result of the coordinated exercise of several distinct subfunctions: a two-port register file, a port 1 buffer register, (P1B), a port 2 buffer register (P2B), a left data type selector (LDTS), a right data type selector (RDTS), an arithmetic logic circuit (ALC), a shifter, a boundary and connect control, separate data input and data output paths and a temporary storage (TS) flip-flop. All of these functions are shown in Fig. 1. The GPU is capable of full-cycle-operation up to 10 MHz; that is, it can access two operands from the file, operate on them through the ALC and store the result in the register file. A more detailed description of each of these subfunctions and their operation is presented below.

The GP001A/1RZ is available in a 64-lead ceramic flat pack (K suffix) and in a 48-contact leadless chip carrier (J suffix).

## ARCHITECTURE

### Register File

The register file contains 16 words of 8-bits each. The file is parallel-word organized with two 8-bit outputs reflecting the contents of the register enabled to the respective ports. The two output ports are referred to hereafter as port 1 and port 2. Any two words addressed by the addresses R and T can be read simultaneously at port 1 and port 2, respectively. Identical data appears at both ports if R and T are equal. Port 1 is addressed via the 4-bit R address; port 2 is addressed via the 4-bit T address.

Data is stored into a selected register through a separate write-data path and under direct control of the load clock (LC). The register addressed by the R address field (port 1) receives data which replaces its previous contents when the load clock goes high. When the clock returns low, the data is locked into the register, i.e., the register is disconnected from the write-data path. Note that it is not possible to write into a register addressed by the T address field.

### Port Buffers P1B and P2B

Ports 1 and 2 are connected to port buffers 1 and 2, P1B and P2B, respectively. These buffers operate in different modes under control of the load clock and some of the programming bit fields: S (source select), M (destination select), and A (ALC function).

**Port 1 Buffer (P1B) -** Port buffer P1B can operate in three different modes, depending on bit-fields S and M. In mode 1, P1B functions as a latch for the direct-input data, DI. In this mode P1B follows DI while LC is low. Data is latched, retaining the value of DI, at the time of the rising clock edge.

In mode 2, port buffer P1B becomes a master/slave register and takes its input (Port 1) from the register file. In this mode, hereafter referred to as the master/slave mode, the contents of the register file are written into the master when the load clock is high. At the negative-going edge of the clock, the slave is isolated from the master and retains its contents. New data can be entered at the next negative-going clock edge. In mode 2 address field R does not affect buffer P1B when the load clock is low. If R or the contents of the register file (R) change while the clock is low, port buffer P1B will retain its data from the last high-to-low clock transition. This mode is used for writing into the register file from DI.

In mode 3, the P1B buffer **in combination** with the addressed register file forms a master/slave function. While the load clock is high, data is written into the addressed register file (R). At the negative-going clock edge, the data is locked in

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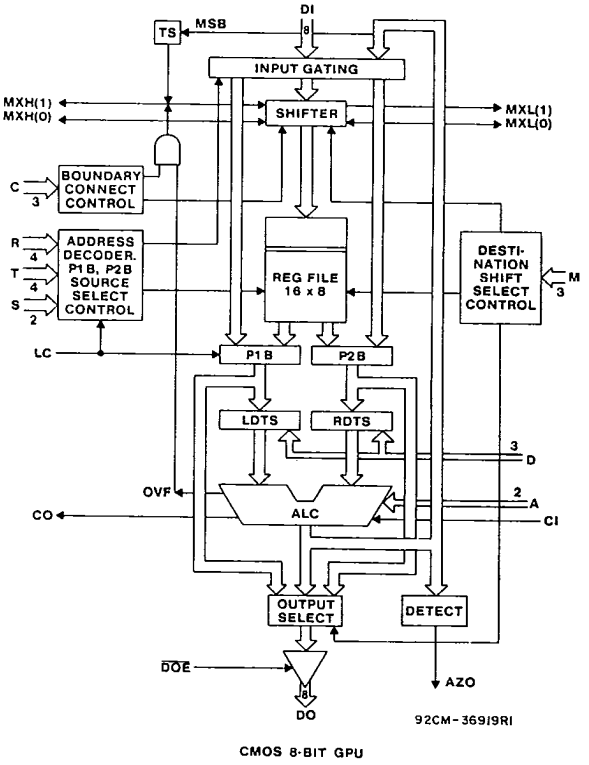
the master while the slave (P1B) follows the contents of the register file. At the next rising clock edge, the master is once more write-enabled while the contents in the slave are locked up for the duration of the high clock cycle.

If the address field R changes while the clock is low, new data is entered into the slave (P1B). The operation of P1B during the low clock cycle, if the address is changed, is the only difference between modes 2 and 3. Mode 3 is referred to hereafter as the slave mode.

**Port Buffer P2B -** Port buffer P2B can also operate in three modes determined by the control fields A and S and the address field T. In the first mode, mode 1, P2B is simply a data follower to incoming data from DI, and is independent of the clock.

In mode 2, which is similar to the slave mode described for P1B, port buffer P2B **in combination** with the register file addressed by T forms a master/slave register. As long as the load clock is low, the slave follows the contents of the master, i.e., the register file addressed by T. At the rising clock edge, the master is disconnected and the contents of the slave are stored. At the next negative-going clock edge, the slave can change if the contents of the master change. As described earlier, if the address T changes while the clock is low, P2B will follow the contents of the newly addressed register file. (Note that there is no write path into a register file addressed by T.)

In mode 3, P2B is simply disconnected from the master (register file) by control bits S and A. Whatever the contents were at the time of disabling, they remain indefinitely until the mode is changed.




CMOS 8-BIT GPU

*Fig. 1 - Block diagram of the CMOS 8-bit general processor unit, GP001.*

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### Data Sources for Register File

The 3-bit M field determines the source of the data to be written into the register file. If M = 100, the load clock is disabled and nothing can be written into the register file. If M = 000 and S = 01, DI is written into the register file. If M = 001, 010, or 011, the output of the shifter is written into the register file. If M = 101, 110, or 111, the output of the ALC is written into the register file.

### Arithmetic-Logic-Circuit (ALC) Operations

The two data type selectors select data for the ALC inputs primarily under control of the D bit field. The left data type selector (LDTS) receives data from P1B and supplies the left ALC port with P1B unmodified, P1B complemented, all zeroes, or P1B right-shifted one bit. For right shift (via LDTS) the A bits must also be programmed (A = 01). In the case where the left operand of the LDTS (P1B) is shifted right one bit, the most significant bit (i.e., the bit that is shifted in) is controlled by the C bit field. For C = 001, the most significant bit of LDTS receives its input from MXH(1), and the least significant bit of LDTS is output to MXL(1). For some values of C, a sign extended shift is caused: i.e., the most significant bit of the left ALC operand is set equal to bit 7 of P1B.

The right data type selector (RDTS) receives data from P2B and supplies the right ALC port with P2B unmodified, P2B complemented, or all zeros. The ALC, controlled by the A bits, provides three basic functions from the GPU: ADD, logical OR, and logical AND. There is one-carry-input to the least significant bit, and one carry-output from the most significant bit. A group look-ahead carry circuit is incorporated in the ALC.

The GPU detects boundary conditions during arithmetic operations and indicates overflow. Overflow is defined as a change in the sign bit when performing addition or subtraction. For example, if the sign bit goes to a one state (negative) during the addition of two positive numbers, overflow has occurred. The GPU detects overflow by taking the exclusive OR of the carry-into and the carry-out of the most significant bit. The overflow signal output is time-shared with shift data on the MHX(1) pin under control of the C bits.

Detection of an all-zero output (AZO) of the ALC is also provided. An external pull-up resistor is required for the AZO output, permitting a wire-OR when more than one GPU is used. An all-zero group status is represented by a logical 1 on the bused AZO; a not-all zero group status is represented by a logical zero.

Note that for logical operations, the carry-out always equals the carry-in. Of course, the carry bit will not affect the result of AND and OR operations.

The ALC functions and data-type operands that can be selected are combined in a matrix in Fig. 2, which shows the various functions that can be implemented by programming the A and D fields. The basic arithmetic and logical functions are:

| | |
|---|---|
| ADD | AND |
| SUBTRACT | OR |
| COMPLEMENT | NAND |
| INCREMENT | NOR |
| CLEAR | SHIFT RIGHT AND ADD |
| PASS | |

| D \ A | 00 | 01 | 10 | 11 | MNEMONICS 00 | 01 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|
| 000 | $\bar{R}$+CI | $\bar{R}$+CI | 0 | $\bar{R}$ | COMP R [1] | COMP R [1] | CLR | NOT R |
| 001 | L+$\bar{R}$+CI | L+$\bar{R}$+CI | L ∧ $\bar{R}$ | L ∨ $\bar{R}$ | SUB L, R [2] | SUB L, R [2] | INHL, R [4] | IMP R, L [5] |
| 010 | $\bar{L}$+$\bar{R}$+CI | $\frac{L}{2}$ +$\bar{R}$+CI | $\bar{L}$ ∧ $\bar{R}$ | $\bar{L}$ ∨ $\bar{R}$ | | SUB $\frac{L}{2}$, R [3] | NOR L, R | NAND L, R |
| 011 | $\bar{L}$+CI | $\bar{L}$+CI | 0 | $\bar{L}$ | COMP L [1] | COMP L [1] | CLR | NOT L |
| 100 | R+CI | R+CI | 0 | R | INC R [3] | INC R [3] | CLR | PASS R |
| 101 | L+R+CI | L+R+CI | L ∧ R | L ∨ R | ADD L, R | ADD L, R | AND L, R | OR L, R |
| 110 | $\bar{L}$+R+CI | $\frac{L}{2}$ +R+CI | $\bar{L}$ ∧ R | $\bar{L}$ ∨ R | SUB R, L [2] | ADD $\frac{L}{2}$, R | INH R, L [4] | IMP L, R [5] |
| 111 | L+CI | L+CI | 0 | L | INC L [3] | INC L [3] | CRL | PASS L |

∧ = AND, ∨ = OR, ∀ = EX. OR

NOTES:
1. CI = 1, TWO'S COMPLEMENT
2. CI = 1, TWO'S COMPLEMENT ARITHMETIC
3. CI = 1
4. INH L, R = L ∧ $\bar{R}$; INH R, L = $\bar{L}$ ∧ R) INHIBIT FUNCTION; L ∀ R = (L ∧ $\bar{R}$) ∨ ($\bar{L}$ ∧ R)
5. IMP R, L = $\bar{L}$ ∨ $\bar{R}$; IMPL, R = $\bar{L}$ ∨ R) IMPLICATION FUNCTION; L ∀ R = (L ∨ $\bar{R}$) ∧ ($\bar{L}$ ∨ R)

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*Fig. 2 - Operand and arithmetic-logic unit function matrix.*

The shift right one bit and ADD function is useful in implementing multiply algorithms. Note also that P1B-P2B and P2B-P1B subtractions can be done. Exclusive OR and exclusive NOR functions can be performed, but require more than one microcycle.

### Shift Operations

In addition to the one-bit right shift of LDTS described above, there is a dedicated shifter providing powerful left-right shift capability on the output of the ALC before it is stored back in the register file. The shift-select logic is capable of straight-through (no shift) operation, shifting the ALC output one bit position right, two bit positions right, or one bit position left. The destination of the shifted data is always the register specified by the port 1 address (R field). Direct data input (DI) to the register file from the data input pins also flows through the shifter (unshifted). Again, data is written into the register specified by the port 1 address. The shift function is determined directly by the M bits. The M field can also disable the load clock to the register file, thereby preventing data from being written. The C bits control shifting indirectly; they are the boundary connect control.

During a shift operation, the user has a wide choice as to the shift carry that replaces the vacant bit position. For example, for M = 010 and C = 010, a one-bit right shift takes place with a 1 going into the most significant bit position.

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The C field, which is the boundary connect control, determines what is input and output to four leads. MXH(1) and MXH(0) are the most significant shift bits and bidirectional pins. MXL(1) and MXL(0) are the least significant shift bits; of these, MXL(0) is bidirectional while MXL(1) represents tristate output only.

The C bits provide three general classes of states for the four MX shift pins. The first class configures the GPU for normal intercircuit shift operations in a multiple GPU machine (C = 001). The second class of states causes the overflow status indicator to be output on MXH(1) while zero or one is shifted into the shifter (C = 010 or 011). The third class of states causes special outputs to be connected to the MXH bits for left shifts and MSB extension for right shifts.

The C field conditions the data paths of the MX bits for shift operations; if a shift is not specified by the M bits, the C-bit decoding does not affect the data entering the shifter. C = 000 turns off the MXH bits regardless of the M-bit control; however, the MXL bits are not affected.

**The Temporary Storage (TS) Bit**

Bit 7 of the ALC output can be latched into the D-type flip-flop temporary storage bit, TS. TS is enabled for input only when C = 111. To store data in TS, the C bits must change to a value other than 111 before bit 7 of the ALC changes. Whenever TS holds meaningful data, C must never be allowed to equal 111, which could possibly happen on a transition of the C bits, for example, from 011 to 100.

**Data Output**

The GPU can output 8-bits in parallel on the data output (DO) pins if the data output enable ($\overline{DOE}$) signal is low. One of three values can be output on DO: the output of the ALC, the output of P1B, or the output of P2B. The M bit field controls the output gating.

For application information, refer to ICAN-7202, "An Introduction to the Use of the General-Processor Unit, GP001."

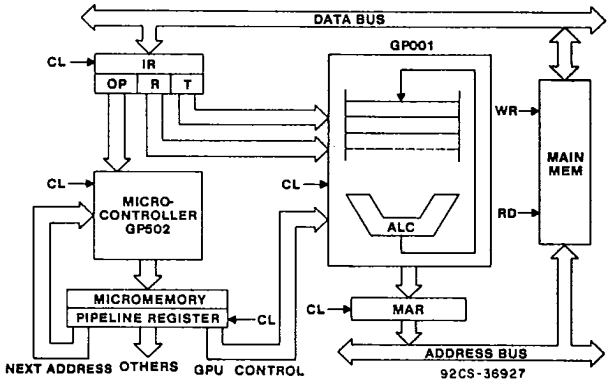


*Fig. 3 - Typical microprogrammed architecture using 8-bit GPU slices, GP001.*

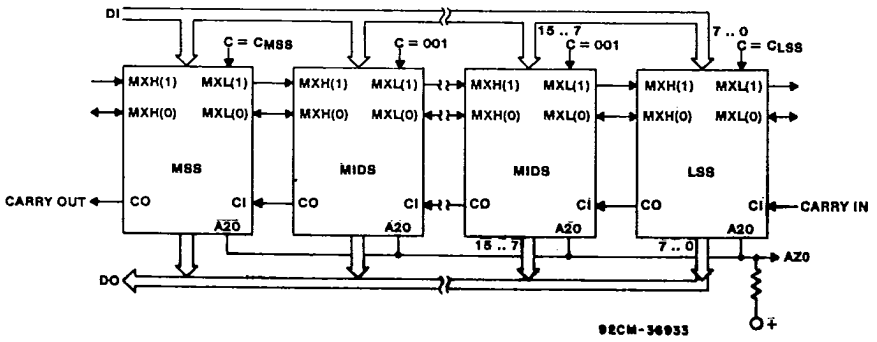


*Fig. 4 - Concatenation of general processor units.*

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**Input/Output Fields of GP001**

| A | S | D | M | C | CI | $\overline{DOE}$ | LC | INPUT CONTROL FIELDS |
|---|---|---|---|---|---|---|---|---|
| 2 | 2 | 3 | 3 | 3 | 1 | 1 | 1 | Number of Bits |

| R | T | DI | MX * | DATA/ADDRESS INPUT FIELDS |
|---|---|---|---|---|
| 4 | 4 | 8 | 3 | Number of Bits |

| DO | CO | AZO | MX * | DATA OUTPUT FIELDS |
|---|---|---|---|---|
| 8 | 1 | 1 | 4 | Number of Bits |

* 3 bits in the MX shift field are bi-directional. MXL1 is output only.

**Definition of Fields for GP001**

| FIELD | FUNCTION |
|---|---|
| **Control** | |
| A | Select ALU Function |
| S | Select Source and Mode for Port Buffers |
| D | Select Left and Right Data Type into ALC |
| M | Select Data Path and Destination |
| C | Select Boundary Conditions for Shifts |
| CI | Carry Input |
| $\overline{DOE}$ | Data Output Enable |
| LC | Clock |
| **Input Data/Address** | |
| R | Address Field for Write/Read Register File |
| T | Address Field for Read Only Register File |
| DI | Data Input |
| MX * | Bits to be Shifted In |
| **Output** | |
| DO | Data Output |
| CO | Carry Out |
| AZO | Accumulator all Zero |
| MX * | Bits Shifted Out |

* 3 bits in the MX field are bi-directional.

**Pin/Signal List for GP001 in 48-Lead LCC**

| PIN NO. | MNEMONIC | DESCRIPTION | INPUT/ OUTPUT |
|---|---|---|---|
| 1 | $V_{SS}$ | 0 Volt, Ground Reference | — |
| 2 | DO3 | Data Output, bit 3 | O |
| 3 | DO4 | Data Output, bit 4 | O |
| 4 | DO5 | Data Output, bit 5 | O |
| 5 | DO6 | Data Output, bit 6 | O |
| 6 | DO7 | Data Output, bit 7 | O |
| 7 | CO | Carry Out | O |
| 8 | $\overline{DOE}$ | Data Out Enable | I |
| 9 | AZO | All Zero Detect Out | O |
| 10 | MXH0 | Multiplexer-Shift High, bit 0 | I/O |
| 11 | MXH1 | Multiplexer-Shift High, bit 1 | I/O |
| 12 | C0 | Boundary, Connect Control bit 0 | I |
| 13 | C1 | Boundary, Connect Control bit 1 | I |
| 14 | C2 | Boundary, Connect Control bit 2 | I |
| 15 | DI7 | Data Input bit 7 | I |
| 16 | DI6 | Data Input bit 6 | I |
| 17 | DI5 | Data Input bit 5 | I |
| 18 | DI4 | Data Input bit 4 | I |
| 19 | DI3 | Data Input bit 3 | I |
| 20 | DI2 | Data Input bit 2 | I |
| 21 | DI1 | Data Input bit 1 | I |
| 22 | DI0 | Data Input bit 0 | I |
| 23 | S1 | Source Select Control bit 1 | I |
| 24 | S0 | Source Select Control bit 0 | I |

| PIN NO. | MNEMONIC | DESCRIPTION | INPUT/ OUTPUT |
|---|---|---|---|
| 25 | $V_{DD}$ | Power Supply | — |
| 26 | R2 | Port 1 Register Select bit 2 | I |
| 27 | R3 | Port 1 Register Select bit 3 | I |
| 28 | T2 | Port 2 Register Select bit 2 | I |
| 29 | T3 | Port 2 Register Select bit 3 | I |
| 30 | R1 | Port 1 Register Select bit 1 | I |
| 31 | T1 | Port 2 Register Select bit 1 | I |
| 32 | T0 | Port 2 Register Select bit 0 | I |
| 33 | R0 | Port 1 Register Select bit 0 | I |
| 34 | M1 | Destination Select Control bit 1 | I |
| 35 | M0 | Destination Select Control bit 0 | I |
| 36 | M2 | Destination Select Control bit 2 | I |
| 37 | MXL0 | Multiplexer Shift Low bit 0 | I/O |
| 38 | MXL1 | Multiplexer Shift Low bit 1 | O |
| 39 | LC | Load Clock | I |
| 40 | D2 | Data Type Select Control bit 2 | I |
| 41 | A0 | ALU Control bit 0 | I |
| 42 | A1 | ALU Control bit 1 | I |
| 43 | C1 | Carry In | I |
| 44 | D1 | Data Type Select Control bit 1 | I |
| 45 | D0 | Data Type Select Control bit 0 | I |
| 46 | DO0 | Data Output bit 0 | O |
| 47 | DO1 | Data Output bit 1 | O |
| 48 | DO2 | Data Output bit 2 | O |

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## TABLES FOR MICROPROGRAMMING THE GP001

### ALC Functions

| A | FUNCTION | OPERANDS |
|---|---|---|
| 00 | ADD | LEFT + RIGHT + CARRY-IN |
| 01 | ADD | LEFT + RIGHT + CARRY-IN |
| 10 | AND | LEFT AND RIGHT |
| 11 | OR | LEFT OR RIGHT |

### Source Select Control — S-Bit

| S | Register File | | P1B | P2B | |
|---|---|---|---|---|---|
| 00 | M≠000 | No Effect | SLAVE TO REG(R) | A≠01 | SLAVE TO REG(T) |
| | M=000 | Write Inhibit | | A=01 | P2B-VALUE NOT CHANGING |
| 01 | M≠000 | No Effect | M≠000 Latch for DI | A≠01 | SLAVE TO REG(T) |
| | M=000 | Write Enable | M=000 Master/Slave Mode | A=01 | P2B-VALUE NOT CHANGING |
| 10 | M≠000 | No Effect | SLAVE TO REG(R) | A≠01 | FOLLOWS DI |
| | M=000 | Write Inhibit | | A=01 | SLAVE TO REG(T) |
| 11 | M≠000 | *R(0) ← 1 | SLAVE TO REG(R+1) | A≠01 | FOLLOWS DI |
| | M=000 | Write Inhibit | | A=01 | SLAVE TO REG(T) |

*LSB of R-Address is forced to one, thus only odd-address register can be accessed.

### Data Type Selector Control — D-Bit

| D | Left Data Type Select | | Right Data Type Select | MXL(1) | | |
|---|---|---|---|---|---|---|
| 000 | 0 | | $\overline{P2B}$ | M≠011 | HIGH Z | |
| | | | | M=011 | ALC(1) | |
| 001 | P1B | | $\overline{P2B}$ | M≠011 | HIGH Z | |
| | | | | M=011 | ALC(1) | |
| 010 | A≠01 | $\overline{P1B}$ | $\overline{P2B}$ | M≠011 | A≠01 | HIGH Z |
| | A=01 | ½ • P1B* | | | A=01 | P1B(0) |
| | | | | M=011 | ALC(1) | |
| 011 | $\overline{P1B}$ | | 0 | M≠011 | HIGH Z | |
| | | | | M=011 | ALC(1) | |
| 100 | 0 | | P2B | M≠011 | HIGH Z | |
| | | | | M=011 | ALC(1) | |
| 101 | P1B | | P2B | M≠011 | HIGH Z | |
| | | | | M=011 | ALC(1) | |
| 110 | A≠01 | $\overline{P1B}$ | P2B | M≠011 | A≠01 | HIGH Z |
| | A=01 | ½ • P1B* | | | A=01 | P1B(0) |
| | | | | M=011 | ALC(1) | |
| 111 | P1B | | 0 | M≠011 | HIGH Z | |
| | | | | M=011 | ALC(1) | |

*Shifted right one bit. The value of this vacant (MSB) bit is determined by the C-bits.

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**Boundary and Connect Control — C-Bits**

| C | Shift Carries † | | | | Left Data Type Select* | MXH(1) | MXH(0) | | TS |
|---|---|---|---|---|---|---|---|---|---|
| | Left 1 Bit | Right 1 Bit | Right 2 Bits | | | | | | |
| | Bit 0 | Bit 7 | Bit 7 | Bit 6 | Bit 7 | | | | |
| 000 | MXL(0) | ALC(7)⊕OVF** | ALC(7)⊕OVF** | ALC(7)⊕OVF** | PIB(7) | INPUT | INPUT | | DISABLED |
| 001 | MXL(0) | MXH(0) | MXH(1) | MXH(0) | MXH(1) | INPUT | M≠01x | ALC(7) | DISABLED |
| | | | | | | | M=01x | Input | |
| 010 | 1 | 1 | 1 | 1 | UNDEF. | OVF | M≠01x | ALC(7) | DISABLED |
| | | | | | | | M=01x | HIGH Z | |
| 011 | 0 | 0 | 0 | 0 | UNDEF. | OVF | M≠01x | ALC(7) | DISABLED |
| | | | | | | | M=01x | HIGH Z | |
| 100 | MXL(0) | ALC(7)⊕OVF** | ALC(7)⊕OVF** | ALC(7)⊕OVF** | P1B(7) | ALC(6) | M≠01x | ALC(7) | DISABLED |
| | | | | | | | M=01x | HIGH Z | |
| 101 | MXL(0) | MXH(0) | TS | MXH(0) | TS | TS | M≠01x | ALC(7) | DISABLED |
| | | | | | | | M=01x | Input | |
| 110 | MXL(0) | MXH(0) | P2B(7) | MXH(0) | P2B(7) | P2B(7) | M≠01x | ALC(7) | DISABLED |
| | | | | | | | M=01x | Input | |
| 111 | MXL(0) | MXH(0) | P2B(7) | MXH(0) | P2B(7) | P2B(7) | M≠01x | ALC(7) | ENABLED |
| | | | | | | | M=01x | Input | |

*Applicable only when D=x10 and A=01.
**MSB is set to Bit 7 of ALC output unless there is an overflow. Then the MSB is set to $\overline{\text{BIT 7}}$ of the ALC output.
†Signifies bits to be shifted into positions left empty by a shift operation.

**Destination Select Control — M-Bits**

| M | DO* | SHIFTER | MXL(1) | | MXL(0) | MXH(0) | | LC | Source of Write-Data for Register File | | P1B MODE | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 | ALC | | D≠x10 or A≠01 | High Z | HIGH Z | C≠000 | ALC(7) | Enabled | S≠01 | Write Inhibit | S≠01 | Slave to Reg(R) |
| | | | D=x10 and A=01 | P1B(0) | | C=000 | HIGH Z | | S=01 | DI | S=01 | Master/Slave to Reg(R) |
| 001 | ALC | Shift left 1 bit | D≠x10 or A≠01 | High Z | INPUT | C≠000 | ALC(7) | Enabled | SHIFTER | | S≠01 | Slave to Reg(R) |
| | | | D=x10 and A=01 | P1B(0) | | C=000 | HIGH Z | | | | S=01 | Latch for DI |
| 010 | ALC | Shift right 1 bit | D≠x10 or A≠01 | High Z | ALC(0) | INPUT | | Enabled | SHIFTER | | S≠01 | Slave to Reg(R) |
| | | | D=x10 and A=01 | P1B(0) | | | | | | | S=01 | Latch for DI |
| 011 | ALC | Shift right 2 bits | D≠x10 or A≠01 | ALC(1) | ALC(0) | INPUT | | Enabled | SHIFTER | | S≠01 | Slave to Reg(R) |
| | | | D=x10 and A=01 | P1B(0) | | | | | | | S=01 | Latch for DI |
| 100 | ALC | | D≠x10 or A≠01 | High Z | HIGH Z | C≠000 | ALC(7) | Disabled | WRITE INHIBIT | | S≠01 | Slave to Reg(R) |
| | | | D=x10 and A=01 | P1B(0) | | C=000 | HIGH Z | | | | S=01 | Latch for DI |
| 101 | ALC | | D≠x10 or A≠01 | High Z | HIGH Z | C≠000 | ALC(7) | Enabled | ALC | | S≠01 | Slave to Reg(R) |
| | | | D=x10 and A=01 | P1B(0) | | C=000 | HIGH Z | | | | S=01 | Latch for DI |
| 110 | P2B | | D≠x10 or A≠01 | High Z | HIGH Z | C≠000 | ALC(7) | Enabled | ALC | | S≠01 | Slave to Reg(R) |
| | | | D=x10 and A=01 | P1B(0) | | C=000 | HIGH Z | | | | S=01 | Latch for DI |
| 111 | P1B | | D≠x10 or A≠01 | High Z | HIGH Z | C≠000 | ALC(7) | Enabled | ALC | | S≠01 | Slave to Reg(R) |
| | | | D=x10 and A=01 | P1B(0) | | C=000 | HIGH Z | | | | S=01 | Latch for DI |

*When $\overline{\text{DOE}}$=1, the DO pins are in the high-impedance state.

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**MAXIMUM RATINGS,** *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, ($V_{DD}$):
(All voltage values referenced to $V_{SS}$ terminal) ..... -0.5 to +11V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to $V_{DD}$ +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE ($P_D$):
For $T_A$ = -55 to +100°C ..... 500 mW
For $T_A$ = +100 to +125°C ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For $T_A$ = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE ($T_A$) ..... -55 to +125°C
STORAGE TEMPERATURE RANGE ($T_{stg}$) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING FOR K PACKAGE TYPES):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

**OPERATING CONDITIONS at $T_A$ = -55°C to +125°C. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:**

| CHARACTERISTIC | LIMITS | | UNITS |
|---|---|---|---|
| | MIN. | MAX. | |
| DC Operating Voltage Range | 5 | 10.5 | V |

**STATIC ELECTRICAL CHARACTERISTICS, $V_{DD}$ = 10 V ± 5%**

| CHARACTERISTIC | | CONDITIONS | LIMITS | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | -55°C, +25°C | | +125°C | | POST ‡ RADIATION +25°C | | |
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Quiescent Device Current | $I_{DD}$ | $V_{IN}$ = 0 V or $V_{DD}$ | — | 2.5 | — | 3.0 | — | 3.0 | mA |
| Operating Device Current | $I_{OPR}$ (Note 3) | Open Circuit Outputs Cycle Time = 200 ns | — | 10 | — | 12 | — | 12 | mA |
| | | Open Circuit Outputs Cycle Time = 1000 ns | — | 2.5 | — | 3.0 | — | 3.0 | mA |
| Input Leakage Current Low | $I_{IL}$ | $V_{IN}$ = 0 (Note 1) | — | 20 | — | 40 | — | 40 | μA |
| Input Leakage Current High | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ (Note 1) | — | 20 | — | 40 | — | 40 | μA |
| 3-State Output Leakage Current | $I_{OZL}$ | Applied Voltage = 0 V (Note 1) | — | 20 | — | 40 | — | 40 | μA |
| 3-State Output Leakage Current | $I_{OZH}$ | Applied Voltage = $V_{DD}$ (Note 1) | — | 20 | — | 40 | — | 40 | μA |
| Output (Sink) Current (Note 4) | $I_{OL1}$ | $V_{OUT}$ = 0.5 V | 8 | — | 6 | — | 6 | — | mA |
| Output (Sink) Current | $I_{OL2}$ | $V_{OUT}$ = 0.5 V | 4 | — | 3.0 | — | 3.0 | — | mA |
| Output (Source) Current | $I_{OH}$ | $V_{OUT}$ = $V_{DD}$ -0.5 V | 2.25 | — | 1.75 | — | 1.75 | — | mA |
| Output Voltage Low Level | $V_{OL}$ | Note 2 | — | 0.5 | — | 0.5 | — | 0.5 | V |
| Output Voltage High Level | $V_{OH}$ | Note 2 | 9.5 | — | 9.5 | — | 9.5 | — | V |
| Input Low Voltage | $V_{IL}$ | $V_{OUT}$ = 1 V or 9 V | — | 3 | — | 3 | — | 3 | V |
| Input High Voltage | $V_{IH}$ | $V_{OUT}$ = 1 V or 9 V | 7 | — | 7 | — | 7 | — | V |

‡ The limits shown are for tests performed within 1 hour of radiating to 100 Krads (Si).

Notes: 1. All other inputs (non-measured) are held at opposite logic level.
2. Input levels shall be $V_{DD}$ and $V_{SS}$. Outputs open.
3. Measured while running the vector set.
4. AZO.

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**STATIC ELECTRICAL CHARACTERISTICS, $V_{DD}$ = 5 V**

| CHARACTERISTIC | | CONDITIONS | LIMITS | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | -55°C, +25°C | | +125°C | | POST ‡ RADIATION +25°C | | |
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Quiescent Device Current | $I_{DD}$ | $V_{IN}$ = 0 V or $V_{DD}$ | — | 0.5 | — | 1.0 | — | 1.0 | mA |
| Operating Device Current | $I_{OPR}$ | Open Circuit Outputs Cycle Time = 200 ns | — | 3 | — | 4 | — | 4 | mA |
| | | Open Circuit Outputs Cycle Time = 1000 ns | — | 1 | — | 1.5 | — | 1.5 | mA |
| Input Leakage Current Low | $I_{IL}$ | $V_{IN}$ = 0 (Note 1) | — | 10 | — | 20 | — | 20 | μA |
| Input Leakage Current High | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ (Note 1) | — | 10 | — | 20 | — | 20 | μA |
| 3-State Output Leakage Current | $I_{OZL}$ | Applied Voltage = 0 V (Note 1) | — | 10 | — | 20 | — | 20 | μA |
| 3-State Output Leakage Current | $I_{OZH}$ | Applied Voltage = $V_{DD}$ (Note 1) | — | 10 | — | 20 | — | 20 | μA |
| Output (Sink) Current | $I_{OL1}$ | $V_{OUT}$ = 0.4 V | 4 | — | 3 | — | 3 | — | mA |
| Output (Sink) Current | $I_{OL2}$ | $V_{OUT}$ = 0.4 V | 1.25 | — | 1 | — | 1 | — | mA |
| Output (Source) Current | $I_{OH}$ | $V_{OUT}$ = $V_{DD}$ -0.4 V | 1.25 | — | 1 | — | 1 | — | mA |
| Output Voltage Low Level | $V_{OL}$ | Note 2 | — | 0.5 | — | 0.5 | — | 0.5 | V |
| Output Voltage High Level | $V_{OH}$ | Note 2 | 4.5 | — | 4.5 | — | 4.5 | — | V |
| Input Low Voltage | $V_{IL}$ | $V_{OUT}$ = 0.5 V or 4.5 V | — | 1.5 | — | 1.5 | — | 1.5 | V |
| Input High Voltage | $V_{IH}$ | $V_{OUT}$ = 0.5 V or 4.5 V | 3.5 | — | 3.5 | — | 3.5 | — | V |

‡ The limits shown are for within 1 hour of radiating to 100 Krads (Si).

Notes: 1. All other inputs (non-measured) are held at opposite logic level.
2. Input levels shall be $V_{DD}$ and $V_{SS}$.
3. Measured while running the vector set.
4. AZO.

**DYNAMIC ELECTRICAL CHARACTERISTICS, $V_{DD}$ = 10 V ± 5%**

| CHARACTERISTIC | PROP. DELAY | MAXIMUM LIMITS | | | UNITS | FIG. |
|---|---|---|---|---|---|---|
| | | -55°C, +25°C | +125°C | POST ‡ RADIATION +25°C | | |
| A → ALU (OR) → DO | $t_{PD}$ | 95 | 120 | 120 | ns | 5 |
| LC → $AZO_{LH}$ | $t_{PD}$ | 165 | 200 | 200 | ns | 6 |
| S → P1B → DO | $t_{PD}$ | 70 | 90 | 90 | ns | 7 |
| LC → ALU (ADD) → DO | $t_{PD}$ | 75 | 95 | 95 | ns | 8 |
| LC → ALU (AND) → DO | $t_{PD}$ | 85 | 105 | 105 | ns | 8 |
| LC → ALU (OR) → DO | $t_{PD}$ | 75 | 95 | 95 | ns | 8 |
| LC → MXH0 | $t_{PD}$ | 90 | 115 | 115 | ns | 9 |
| LC → MXH1 | $t_{PD}$ | 75 | 95 | 95 | ns | 9 |
| LC → MXL0 | $t_{PD}$ | 75 | 95 | 95 | ns | 9 |
| LC → MXL1 | $t_{PD}$ | 80 | 100 | 100 | ns | 9 |
| (R) → P1B → DO | $t_{PD}$ | 95 | 120 | 120 | ns | 10 |
| (T) → P2B → DO | $t_{PD}$ | 95 | 120 | 120 | ns | 10 |
| CI → CO | $t_{PD}$ | 30 | 40 | 40 | ns | 11 |

‡ Radiation measurements are made on two samples/wafer. The limits shown are for tests performed within one hour of radiating to 100 Krads (Si).

**DYNAMIC ELECTRICAL CHARACTERISTICS, $V_{DD}$ = 5 V**

| CHARACTERISTIC | PROP. DELAY | MAXIMUM LIMITS | | | UNITS | FIG. |
|---|---|---|---|---|---|---|
| | | -55°C, +25°C | +125°C | POST ‡ RADIATION +25°C | | |
| A → ALU (OR) → DO | $t_{PD}$ | 200 | 250 | 250 | ns | 5 |
| LC → $AZO_{LH}$ | | 330 | 410 | 410 | | 6 |
| S → P1B → DO | | 145 | 180 | 180 | | 7 |
| LC → ALU (ADD) → DO | | 170 | 210 | 210 | | 8 |
| LC → ALU (AND) → DO | | 190 | 230 | 230 | | 8 |
| LC → ALU (OR) → DO | | 160 | 200 | 200 | | 8 |
| LC → MXH0 | | 190 | 230 | 230 | | 9 |
| LC → MXH1 | | 185 | 230 | 230 | | 9 |
| LC → MXL0 | | 180 | 225 | 225 | | 9 |
| LC → MXL1 | | 180 | 225 | 225 | | 9 |
| (R) → P1B → DO | | 220 | 275 | 275 | | 10 |
| (T) → P2B → DO | | 220 | 275 | 275 | | 10 |
| CI → CO | | 70 | 90 | 90 | | 11 |

‡ Radiation measurements are made on two samples/wafer. The limits shown are for tests performed within one hour of radiating to 100 Krads (Si).

**Timing Diagrams for Dynamic Electrical Characteristics**

9

Figure numbers are referred to in Dynamic Electrical Characteristics Charts.

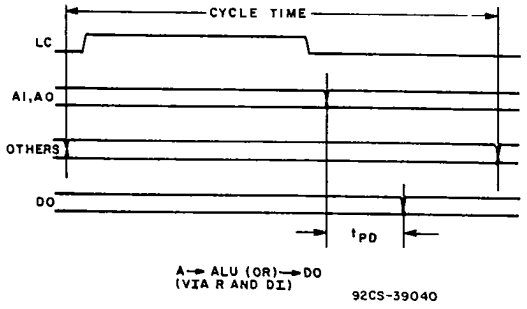


*Fig. 5*

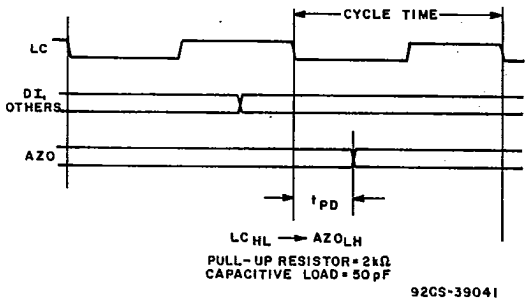


*Fig. 6*

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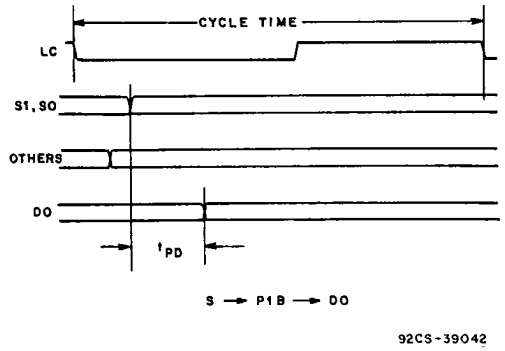


Fig. 7

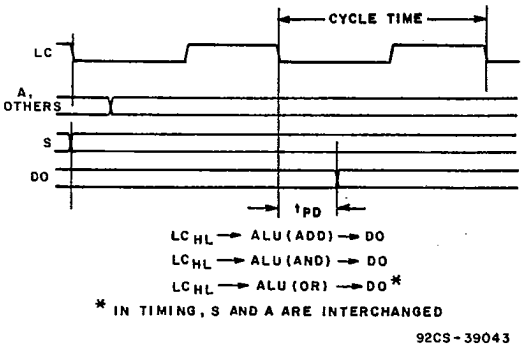


Fig. 8

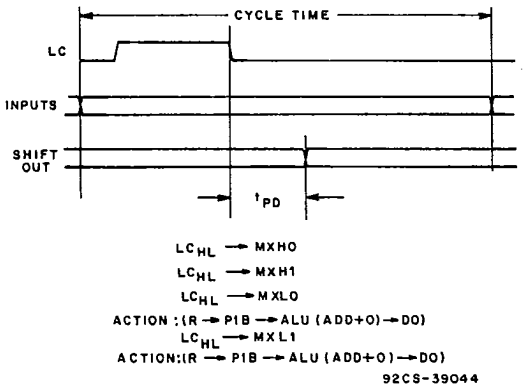


Fig. 9

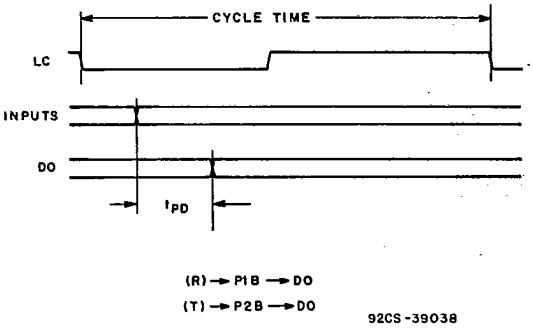


Fig. 10

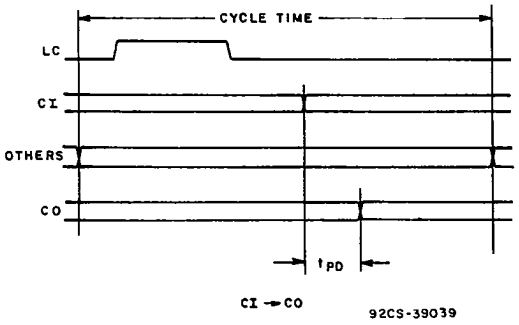


Fig. 11

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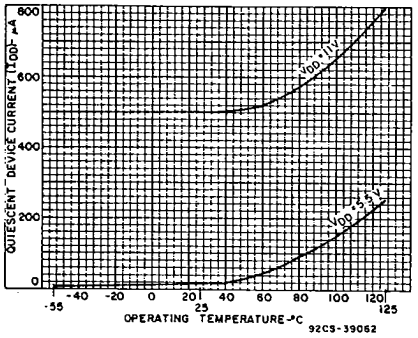


*Fig. 12 - Typical quiescent device current as a function of operating temperature.*

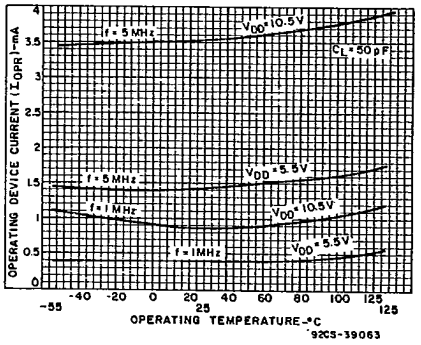


*Fig. 13 - Typical operating device current as a function of operating temperature.*

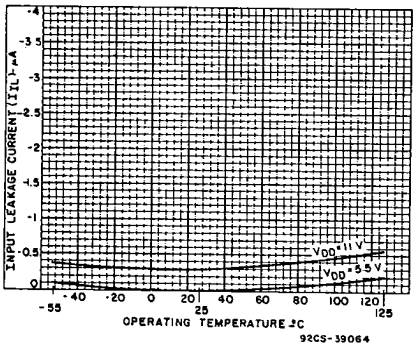


*Fig. 14 - Typical input leakage current low as a function of operating temperature.*

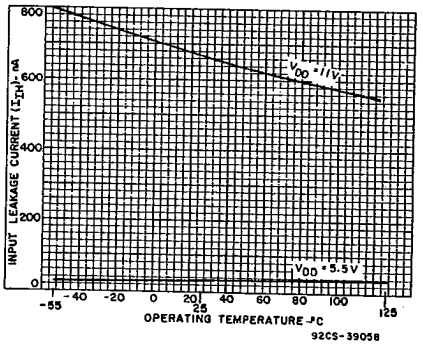


*Fig. 15 - Typical input leakage current high as a function of operating temperature.*

9

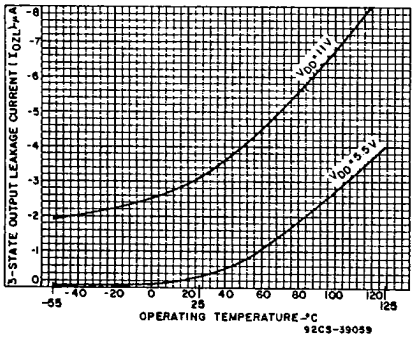


*Fig. 16 - Typical 3-state output leakage current as a function of operating temperature.*

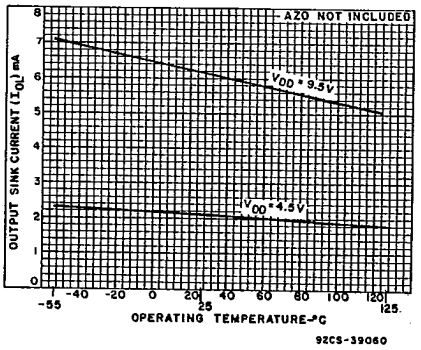


*Fig. 17 - Typical output sink current as a function of operating temperature.*

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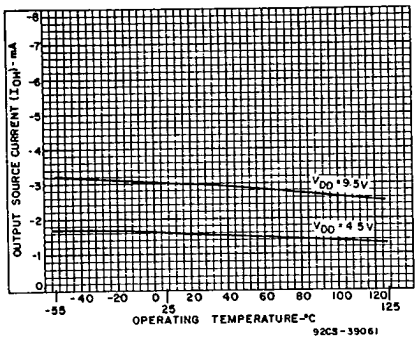



*Fig. 18 - Typical output source current as a function of operating temperature.*

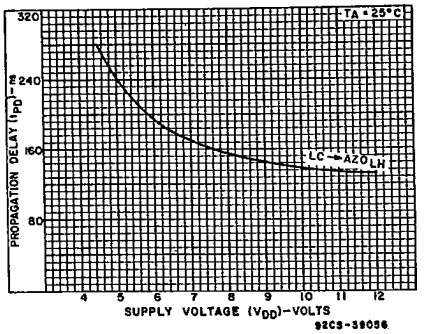



*Fig. 19 - Typical propagation delay times as a function of supply voltage.*

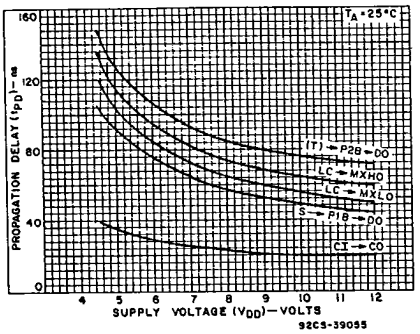



*Fig. 20 - Typical propagation delay times as a function of supply voltage.*

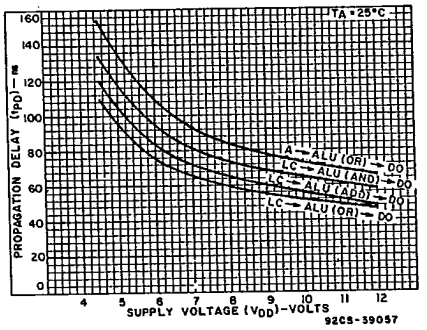



*Fig. 21 - Typical propagation delay times as a function of supply voltage.*

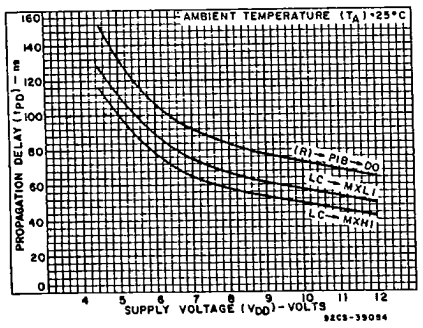



*Fig. 22 - Typical propagation delay times as a function supply voltage.*

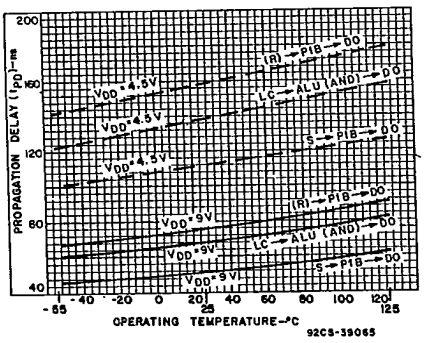



*Fig. 23 - Typical propagation delay times as a function of operating temperature.*

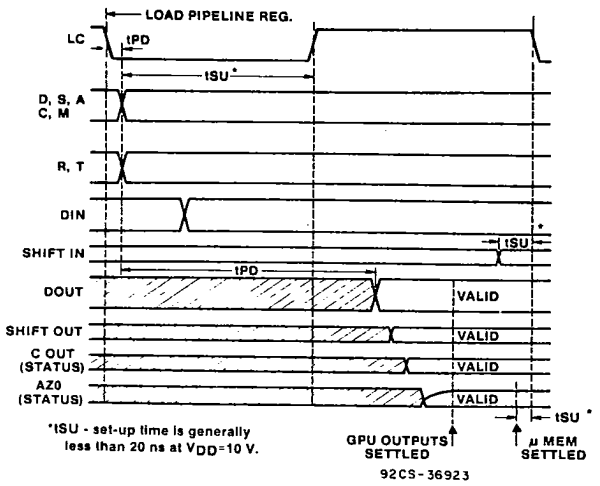
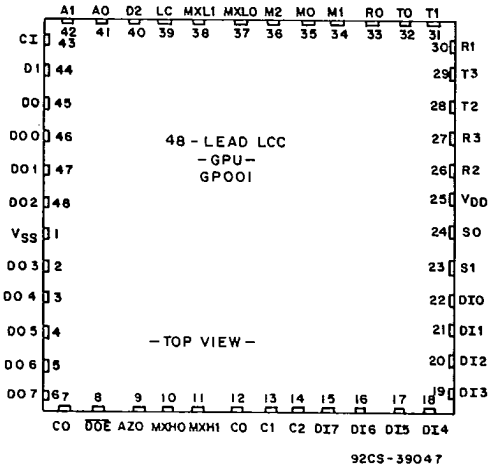
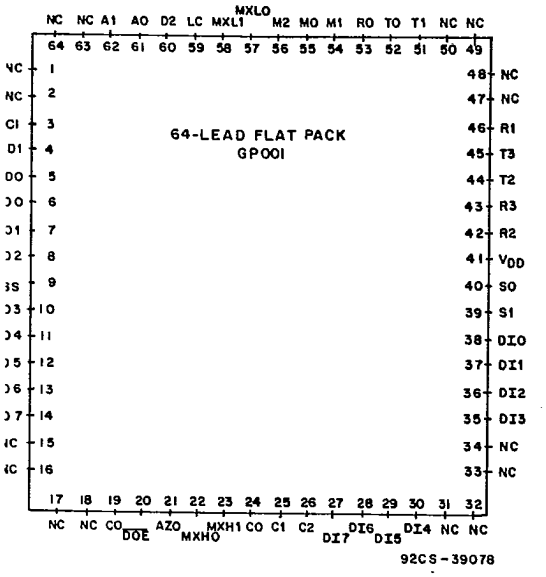



*Fig. 24 - Timing diagram of major events in a microcycle.*




**TERMINAL ASSIGNMENT FOR J PACKAGE (48-CONTACT, LEADLESS CHIP CARRIER)**

**Package Specifications**
See Section 11, Fig. 36, c1




**TERMINAL ASSIGNMENT FOR K PACKAGE (64-LEAD, CERAMIC FLATPACK)**

**Package Specifications**
See Section 11, Fig. 31

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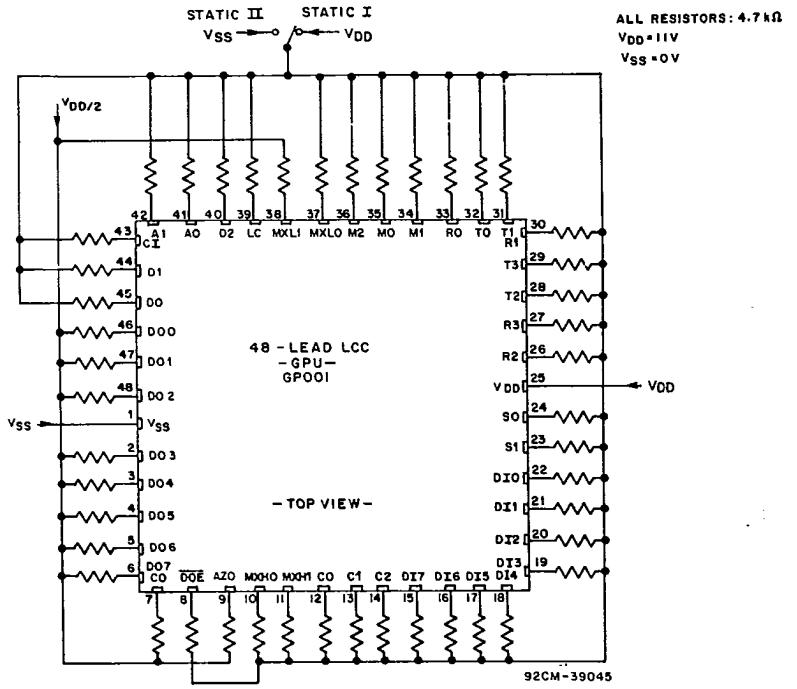


*Fig. 25 - 48-Lead LCC static I and II burn-in circuit.*

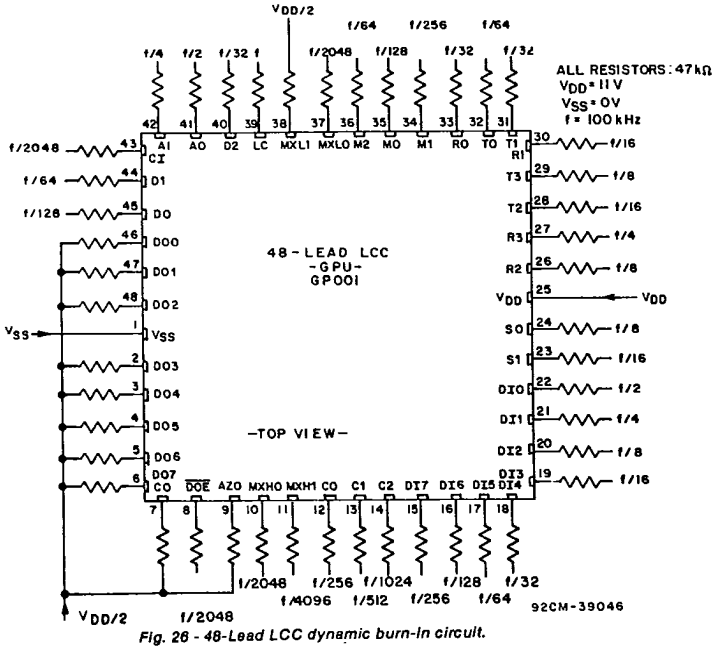


*Fig. 26 - 48-Lead LCC dynamic burn-in circuit.*

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**Modified Class S Screening for GP001A/1RZ per MIL-STD-883 Method 5004**

| | |
|---|---|
| Wafer Lot Acceptance (All Lots) | Method 5007 (Includes SEM) |
| Radiation Verification (Each Wafer) | Method 1019 - 100K rads (Si) Total Dose, >100 rads/sec<br>2 samples/wafer, 0 reject |
| Nondestructive Bond Pull (100%) | Method 2023 |
| Internal Visual (100%) | Method 2010 - See, "Visual Inspection" |
| Stabilization Bake (100%) | Method 1008 - Condition C (24 hr min., 150°C min.) |
| Temperature Cycling (100%) | Method 1010 - Condition C (-65°C to 150°C) |
| Constant Acceleration (100%) | Method 2001 - Condition E, $Y_1$ (30,000 g) |
| PIND Testing (100%) | Method 2020 - Condition A (20 g peak at 60 Hz) |
| Visual Inspection (100%) | — |
| Serialization (100%) | — |
| Initial Electrical Tests (100%) | See Table I |
| Dynamic Burn-In I (100%) | 160 hrs, 125°C, See Table II |
| Interim Electrical Tests I (100%) | PDA 10% all tests, See Table I |
| Static Burn-In I (100%) | 24 hrs, 125°C, See Table II |
| Static Burn-In II (100%) | 24 hrs, 125°C, See Table II |
| Interim Electrical Tests II (100%) | See Tables I and III |
| Dynamic Burn-In II (100%) | 240 hrs, 125°C, See Table II |
| Interim Electrical Tests III (100%) | PDA 5% all tests, PDA 3% functional, See Tables I and III |
| Fine and Gross Seal (100%) | Method 1014 |
| Final Electrical Tests (100%) | See Table I |
| Radiographic (100%) | Method 2012 (1 view) |
| External Visual (100%) | Method 2009 |
| Quality Conformance | |
| Group A (All Tests) | Method 5005 (Class S), See Table I |
| Group B (Optional) | Method 5005 (Class S), See Table I |
| Group D (Optional) | Method 5005 (Class S), See Table I |
| CSI and, or, GSI (Optional) | — |

**Table I - Electrical Tests**

For individual tests, refer to the Static and Dynamic Characteristics Charts.

| | |
|---|---|
| Post Radiation | Post Radiation, 25°C |
| Initial Electrical Tests | 25°C |
| Interim Electrical Tests I | 25°C |
| Interim Electrical Tests II | 25°C |
| Interim Electrical Tests III | 25°C |
| Final Electrical Tests | -55°C, 25°C, 125°C |
| Quality Conformance | |
| Group A | -55°C, 25°C, 125°C |
| Group B | 25°C |
| Group D | 25°C |

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**Table II - Burn-In and Life-Test Circuits and Timing Waveforms**

| TEST | TEMPERATURE | DURATION MIN. | $V_{DD}$ MIN. |
|---|---|---|---|
| Dynamic I | 125°C | 160 hr | 11 V |
| Static I | 125°C | 24 hr | 11 V |
| Static II | 125°C | 24 hr | 11 V |
| Dynamic II | 125°C | 240 hr | 11 V |
| Life Test | 125°C | 1000 hr | 10.5 V |

**Table III - Delta Limits**

| TEST | SYMBOL | DELTA LIMITS * |
|---|---|---|
| Quiescent Device Current | $I_{DD}$ | ±20% |
| Output Low Current | $I_{OL}$ | ±20% † |
| Output High Current | $I_{OH}$ | ±20% † |
| 3-State Output Leakage Current, Low | $I_{OZL}$ | ±20% |
| 3-State Output Leakage Current, High | $I_{OZH}$ | ±20% |

$V_{DD}$ = 10 V ± 5% * Limits apply at +25°C † Measured from initial value

**Table IV - Delta Calculations**

| DELTA CALCULATION | INITIAL READING | FINAL READING |
|---|---|---|
| I | Interim Electrical Tests I | Interim Electrical Tests II |
| II | Interim Electrical Tests I | Interim Electrical Test III |

**VISUAL INSPECTION**

*Visual Inspection for Class S is performed to MIL-STD-883, Method 2010, Condition A except as follows:*

**Use:**

3.2.1.1 - Metallization Scratches
3.2.1.2 - Metallization Voids
3.2.1.6 - Metallization Bridging
3.2.1.7 - Metallization Alignment
3.2.3 - Scribing and Die Defects. In addition, semi-circular cracks that point away from the active circuit area are acceptable.
3.2.3c - A crack that exceeds 5 mils in length must also point towards or cross a scribe grid line.
3.1.7b - Lifting or Peeling of Glassivation, add NOTE of 3.2.7b to 3.1.7b.

**Notes:**

A. High magnification inspection is performed at 200X to 300X and applies to the high current areas of the chip. The remainder of the chip is inspected at 75X to 150X where high magnification is required.

B. Criteria 3.2.1.1a Metallization Scratches, and 3.2.1.2a Metallization Voids shall also apply to metallization over a passivation step (3.2.1.1d, 3.2.1.2b). Underlying oxide must also be exposed.

C. Criteria 3.2.1.7 Metallization Alignment and 3.1.2 Diffusion and Passivation Faults are applied to the center and two opposite corners of the chip. Areas of sufficient complexity are viewed to assure general alignment and contact coverage and shall consist only of the area exposed to the immediate field of view.

D. SOS Technology Devices
1. Diffusion faults 3.1.2.1 are not applicable. SOS devices are inspected for complete islands, bridging between islands and missing adjacent contacts from a row in a contact chain.
2. The 1-mil wire clearance criteria is not applicable.
3. Passivation faults are not applicable when a second free-flow oxide is used prior to metallization.
4. Oxide gate bridge inspection is not applicable.
5. Semicircular cracks not in an active area which start and end at the pellet edge are acceptable.