

NM43256A 262 144-Bit CMOS Static RAM

General Description

The NM43256A is a high speed, low power, 32768 words by 8 bits CMOS static RAM fabricated with advanced silicon-gate CMOS technology. The NM43256A is a low standby power device using n-channel memory cell with polysilicon resistors. Furthermore, a novel circuit technique makes the NM43256A a high speed and low operating power device which requires no clocking or refreshing to operate.

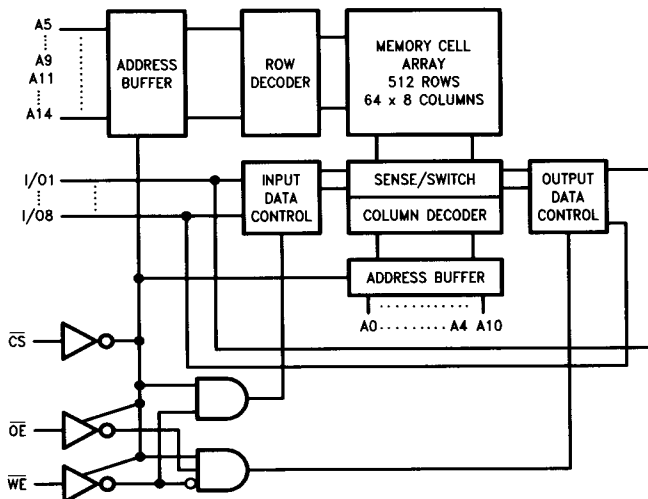
Minimum standby power is drawn by this device when $\overline{CS}$ is at a high level, independent of the other input levels.

Data retention is guaranteed at a power supply voltage as low as 2V. The NM43256AMX is packaged in TSOP (Thin Small Outline Package), supporting high density applications.

Features

- Single +5V supply
- Fully static operation: No clock or refresh required
- TTL compatible: All inputs and outputs
- Common I/O using TRI-STATE® output
- One chip select and one output enable inputs for easy application
- Fast access time:
 - NM43256A-10 100 ns max.
 - NM43256A-12 120 ns max.
 - NM43256A-15 150 ns max.
- Low power dissipation:
 - Standby supply current 2 μ A typ.
 - Data retention supply current 1 μ A typ.
 - Active 40 mA max.
 - Standby NM43256AMX-10LL/12LL 50 μ A max.
- Data retention voltage: 2 V_{min}

Block Diagram



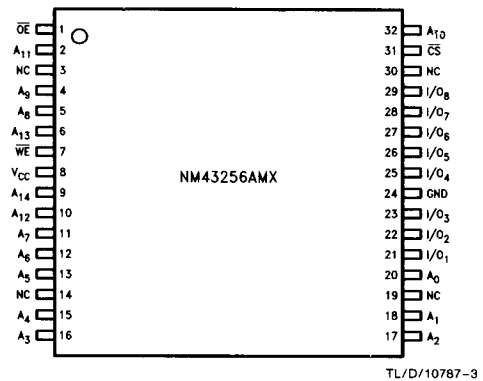
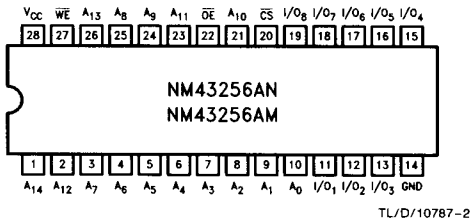
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Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	I_{CC}
H	X	X	Not Selected	HI-Z	Standby
L	H	H	Not Selected	HI-Z	Active
L	L	H	Read	D _{OUT}	Active
L	X	L	Write	D _{IN}	Active

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Pin Configuration



Pin Names

A ₀ to A ₁₄	Address Input
I/O ₁ to I/O ₈	Data Input/Output
$\overline{CS}$	Chip Select
OE	Output Enable
WE	Write Enable
V _{CC}	Power Supply (+ 5V)
GND	GND
NC	No Connection

Ordering Information

Part Number	Access Time Max.	Package Type	Note
NM43256AN-10	100 ns	28-Pin Plastic DIP (600 Mil)	L Version
NM43256AN-12	120 ns		
NM43256AN-15	150 ns		
NM43256AN-10L	100 ns		
NM43256AN-12L	120 ns		
NM43256AN-15L	150 ns		
NM43256AM-10L	100 ns	28-Pin Plastic SOP (450 Mil)	L Version
NM43256AM-12L	120 ns		
NM43256AM-15L	150 ns		
NM43256AMX-10L	100 ns	32-Pin Plastic TSOP	L Version
NM43256AMX-12L	120 ns		LL Version
NM43256AMX-10LL	100 ns		
NM43256AMX-12LL	120 ns		
NM43256AMXR-10L	100 ns	32-Pin Plastic TSOP (Reverse Bent)	L Version
NM43256AMXR-12L	120 ns		LL Version
NM43256AMXR-10LL	100 ns		
NM43256AMXR-12LL	120 ns		

Absolute Maximum Ratings*

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	$-0.5V^{**}$ to $+7.0V$
Input or Output Voltage	$-0.5V^{**}$ to $V_{CC} + 0.5V$
Operating Temperature	$0^{\circ}C$ to $+70^{\circ}C$

Storage Temperature

$-55^{\circ}C$ to $+125^{\circ}C$

Power Dissipation

1.0W

*Note: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note: $-3.0 V_{min}$ (Pulse width 50 ns)

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage V_{CC}	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2		$V_{CC} + 0.5$	V
V_{IL}	Input Low Voltage	-0.3^{**}		0.8	V
T_A	Ambient Temperature	0		70	$^{\circ}C$

** $-3.0 V_{min}$ (Pulse width 50 ns).

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{LI}	Input Leakage Current	$V_{IN} = 0$ to V_{CC}	-1.0		1.0	μA
I_{LO}	I/O Leakage Current	$V_{CS} = V_{IH}$ or $V_{OE} = V_{IH}$ or $V_{WE} = V_{IL}$, $I_{I/O} = 0$ to V_{CC}	-1.0		1.0	μA
I_{CCA1}	Operating Supply Current	$V_{CS} = V_{IL}$, Min Cycle, $I_{I/O} = 0$			(Note 1)	mA
I_{CCA2}		$V_{CS} = V_{IL}$, $I_{I/O} = 0$			10	mA
I_{CCA3}		$V_{CS} \leq 0.2V$, $f = 1$ MHz, $I_{I/O} = 0$, $V_{IL} \leq 0.2V$, $V_{IH} \geq V_{CC} - 0.2V$			10	mA
I_{SB}	Standby Supply Current	$V_{CS} = V_{IH}$			3	mA
I_{SB1}		$V_{CS} \geq V_{CC} - 0.2V$		2	(Note 2)	μA
V_{OH1}	Output High Voltage	$I_{OH} = -1.0$ mA	2.4			V
V_{OH2}		$I_{OH} = -0.1$ mA	$V_{CC} - 0.5$			V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.4	V

Note 1: NM43256A-10 40 mA max.
NM43256A-12 40 mA max.
NM43256A-15 35 mA max.

Note 2: NM43256AN-10/-12/-15 2 mA max.
NM43256A-10L/-12L/-15L 100 μA max.
NM43256AMX-10LL/-12LL/-15LL 50 μA max.

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0\text{V}$			5	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = 0\text{V}$			8	pF

Note: This parameter is periodically sampled and not 100% tested.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

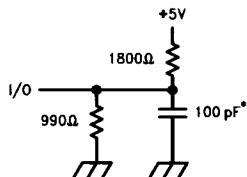
AC TEST CONDITIONS

Input Pulse Levels 0.8V to 2.2V

Input Pulse Rise and Fall Time 5 ns

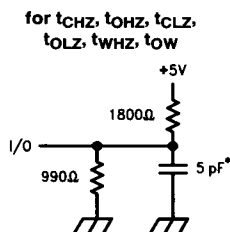
Timing Reference Levels 1.5V

Output Load: See Figures 1, 2



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FIGURE 1



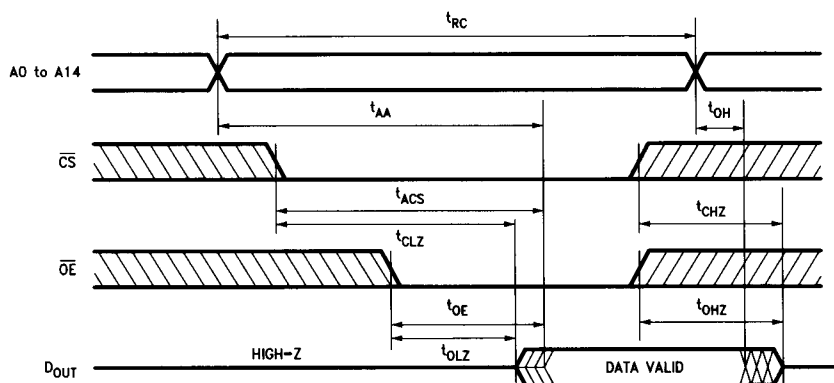
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FIGURE 2

Read Cycle

Symbol	Parameter	NM43256AN-10/-10L NM43256AM-10L NM43256AMX-10L/-10LL		NM43256AN-12/-12L NM43256AM-12L NM43256AMX-12L/-12LL		NM43256AN-15/-15L NM43256AM-15L		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	100		120		150		ns
t_{AA}	Address Access Time		100		120		150	ns
t_{ACS}	Chip Select Access Time		100		120		150	ns
t_{OE}	Output Enable to Output Valid		50		60		70	ns
t_{OH}	Output Hold from Address Change	10		10		10		ns
t_{CLZ}	Chip Select to Output in LO-Z	10		10		10		ns
t_{OLZ}	Output Enable to to Output in LO-Z	5		5		5		ns
t_{CHZ}	Chip Select to to Output in HI-Z		35		40		50	ns
t_{OHZ}	Output Enable to Output in HI-Z		35		40		50	ns

Read Cycle Timing Chart (Notes: 1, 2, 3)



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Note 1: $\overline{WE}$ is high for read cycle.

Note 2: Device is continuously selected, $\overline{CS} = \overline{OE} = V_{IL}$.

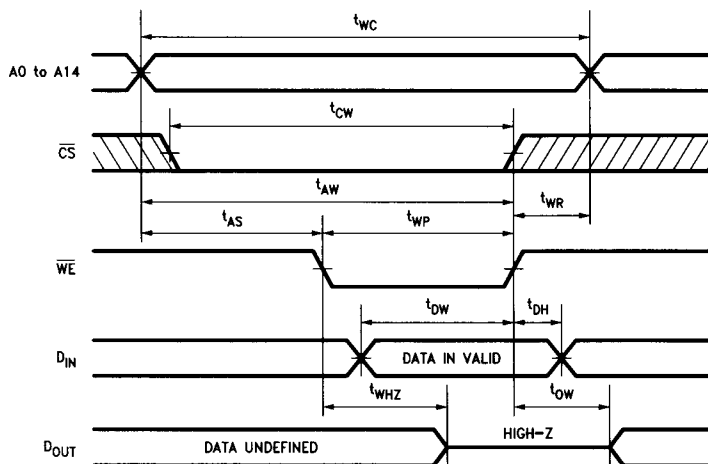
Note 3: Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

Symbol	Parameter	NM43256AN-10/-10L NM43256AM-10L NM43256AMX-10L/-10LL		NM43256AN-12/-12L NM43256AM-12L NM43256AMX-12L/-12LL		NM43256AN-15/-15L NM43256AM-15L		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	100		120		150		ns
t_{CW}	Chip Select to End of Write	80		85		100		ns
t_{AW}	Address Valid to End of Write	80		85		100		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	70		70		90		ns
t_{WR}	Write Recovery Time	5		5		5		ns
t_{DW}	Data Valid to End of Write	40		50		60		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WHZ}	Write Enable to Output in HI-Z		35		40		50	ns
t_{OW}	Output Active from End of Write	10		10		10		ns

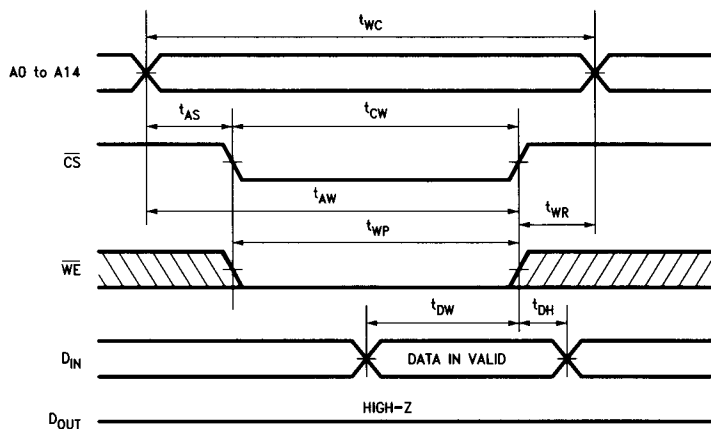
Write Cycle Timing Charts

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (Notes: 1, 2, 3, 4)



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WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (Notes: 1, 2)



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Note 1: A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

Note 2: $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

Note 3: If $\overline{OE}$ is high, I/O pins remain in a high impedance state.

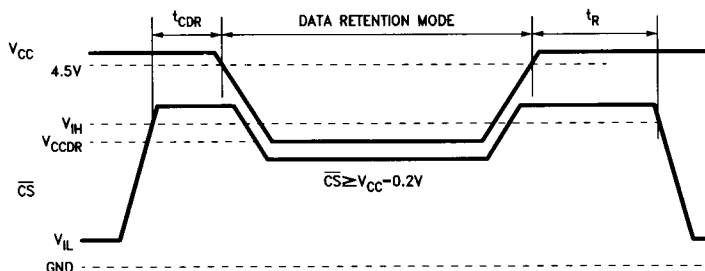
Note 4: During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

Low V_{CC} Data Retention Characteristics ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CCDR}	Data Retention Supply Voltage	$\overline{CS} \geq V_{CC} - 0.2\text{V}$	2.0		5.5	V
I_{CCDR}	Data Retention Supply Current	$V_{CC} = 3.0\text{V}$, $\overline{CS} \geq V_{CC} - 0.2\text{V}$		1	(Note 1)	μA
t_{CDR}	Chip Deselection to Data Retention Mode		0			ns
t_R	Operation Recovery Time		t_{RC}			ns

Note 1: NM43256A-10L/-12L/-15L 50 μA max. ($T_A = 0^\circ\text{C} \sim 70^\circ\text{C}$)
 15 μA max. ($T_A = 0^\circ\text{C} \sim 40^\circ\text{C}$)
 NM43256AMX-10LL/-12LL 20 μA max. ($T_A = 0^\circ\text{C} \sim 70^\circ\text{C}$)
 3 μA max. ($T_A = 0^\circ\text{C} \sim 40^\circ\text{C}$)

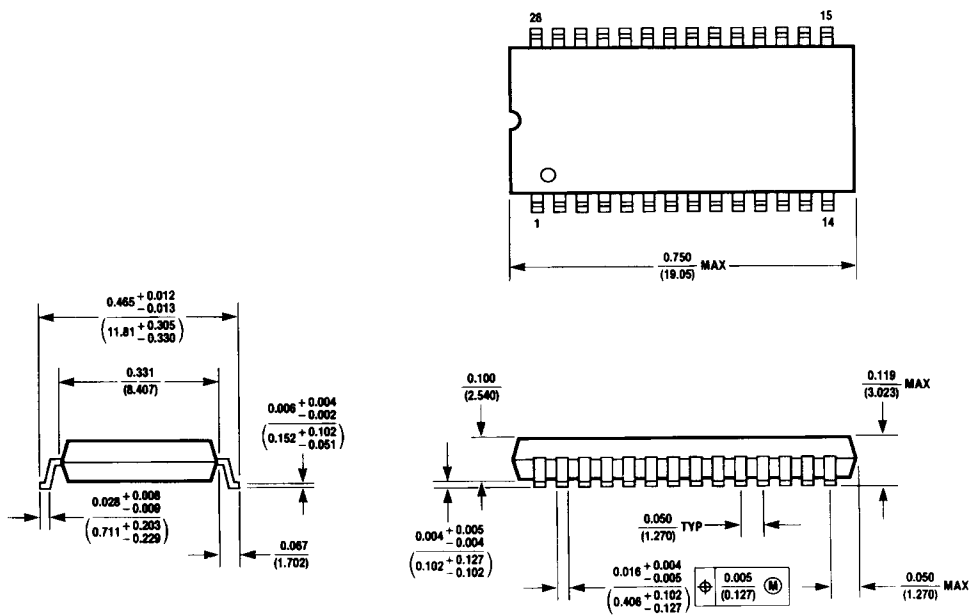
DATA RETENTION TIMING CHART (Note 1)



Note 1: The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a high impedance state.

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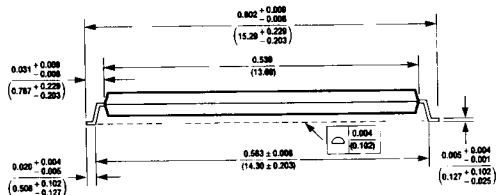
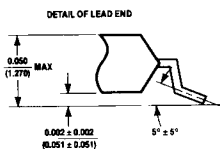
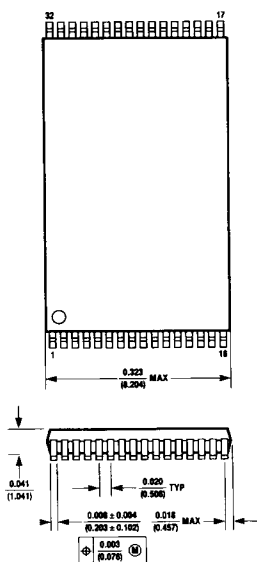
Package Information



28-Pin Plastic SOP (450 mil)
Order Number NM43256AM

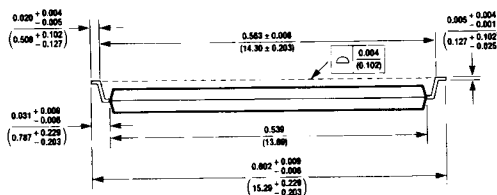
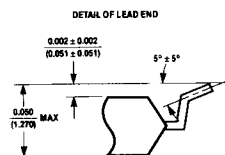
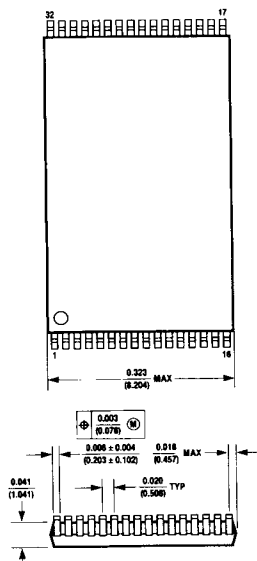
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Package Information (Continued)



32-Pin Plastic TSOP (600 mil)
Order Number NM43256AMX

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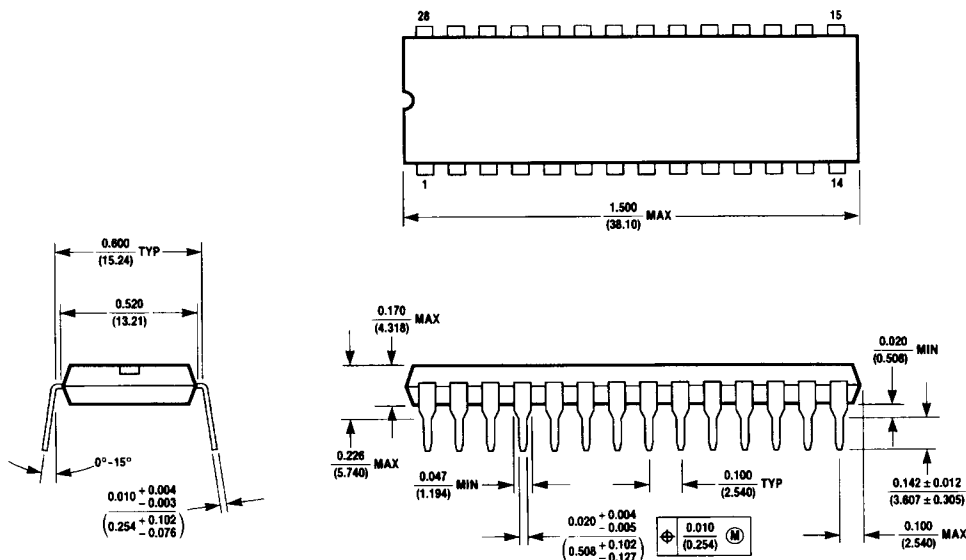


32-Pin Plastic TSOP (600 mil)
Order Number NM43256AMXR

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Package Information (Continued)

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28-Pin Plastic DIP (600 mil)
Order Number NM43256AN

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