

GP2010

GLOBAL POSITIONING SYSTEM RECEIVER RF FRONT END

(Supersedes edition in August 1996 Global Positioning Products Handbook, HB4305-1.0)

The GP2010 is GEC Plessey Semiconductors' second generation RF Front-end for Global Positioning System (GPS) receivers. The GP2010 uses many innovative design techniques and a leading-edge bipolar process to offer a low power, low cost and high reliability RF Front End solution. The GP2010 is designed to operate from either 3 or 5 Volt power supplies.

The input to the device is the L1 (1575.42MHz) Coarse-Acquisition (C/A) code Global Positioning signal from an antenna (via a low-noise pre-amplifier). The output is 2-bit quantised for subsequent signal processing in the digital domain. The GP2010 contains an on-chip synthesiser, mixers, AGC and a quantiser which provides Sign and Magnitude digital outputs. A minimum of external components is required to make a complete GPS front-end.

The device has been designed to operate with the GP2021 12-channel Global Positioning Correlator, and DW9255 SAW filter, both also available from GEC Plessey Semiconductors.

FEATURES

- Low Voltage Operation (3V - 5V)
- Low Power - 200mW typ. (3V supply)
- C/A Code Compatible
- On-chip PLL Including Complete VCO
- Triple Conversion Receiver
- 44-Lead Surface Mount Quad Flat-Pack Package
- Sign and Magnitude Digital Outputs
- Compatible with GP2021 CMOS Correlator

APPLICATIONS

- C/A Code Global Positioning by Satellite Receivers
- Time Standards
- Navigation
- Surveying

ORDERING INFORMATION

The GP2010 is available in 44 pin Quad Flat pack (gullwing formed leads) to Industrial (-40°C to +85°C) grade.

ORDERING CODE

GP2010 IG GPBR Industrial - Plastic 44-pin PQFP

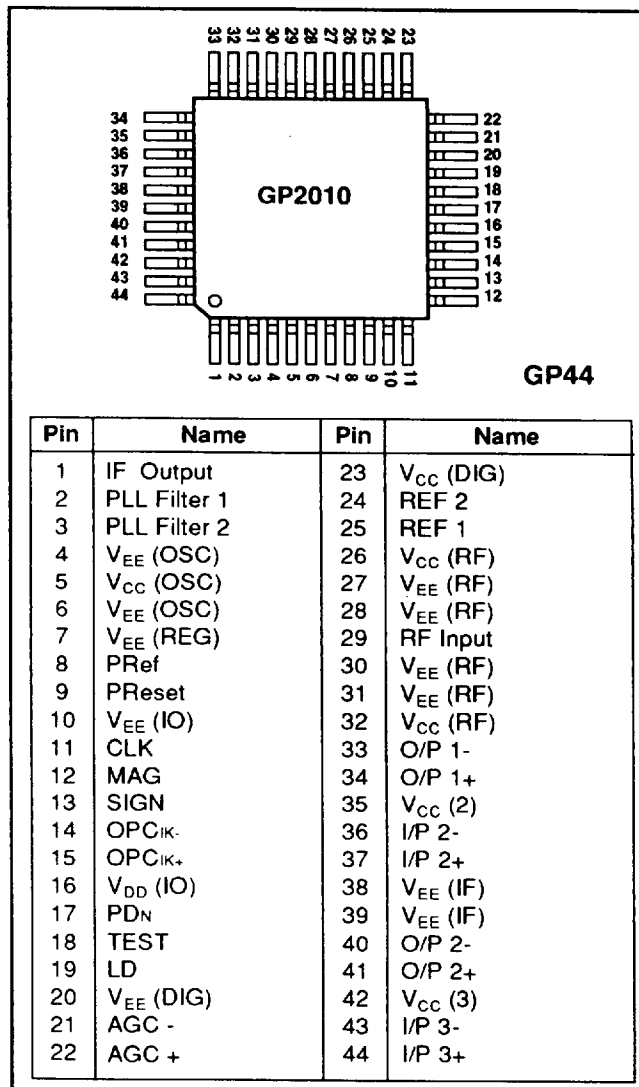


Fig. 1 Pin connections - top view

RELATED PRODUCTS AND PUBLICATIONS

| Part | Description | Data Reference |
|-------------|--|----------------|
| DW9255 | 35.42MHz SAW Filter | DS3861 |
| GP2021 | Twelve-Channel Correlator | DS4057 |
| GPBuilder-2 | Twelve-Channel GPS receiver development system | DS4004 |
| GP2010 | Design with the GP2010 | AN4364 |
| GP2015 | Small RF Format Front End | DS4374 |
| GP2015 | Design with the GP2015 | AN4533 |

ABSOLUTE MAXIMUM RATINGS (Non-simultaneous)

| | |
|---|------------------------|
| Max. Supply Voltage | 7V |
| Max. RF Input | +15dBm |
| Max. voltage on any pin except LD (pin 19) and PReset (pin 9), which are 5.5V | $V_{CC}/V_{DD} + 0.5V$ |
| Min. voltage on any pin | $V_{EE} - 0.5V$ |
| Storage Temperature | -65°C to +150°C |
| Operation Junction Temperature | -40°C to +150°C |
| 10MHz Reference Input | 1.5V pk -pk |

ESD PROTECTION

The GP2010 device is static sensitive. The most sensitive pins withstand a 750V test by the human body model. Therefore, ESD handling precautions are essential to avoid degradation of performance or permanent damage to this device.

PRODUCT DESCRIPTION

The GP2010 receives the 1575.42MHz signal transmitted by GPS satellites and converts it to a 4.309MHz IF, using a triple down-conversion. The 4.309MHz IF is sampled to produce a 2-bit digital output. If the GP2010 is used in conjunction with the GP2021 correlator, then the GP2021 provides a sampling clock of 5.714MHz. This converts the IF to a 1.405MHz 2-bit digital output at TTL levels.

The GP2010 can operate from a single supply from +3V (nominal) to +5V (nominal).

A block diagram of the circuit is shown in figure 2.

IF STRIP

The input signal to the GP2010 is the GPS L1 signal received via an antenna and a suitable LNA. The L1 input is a spread spectrum signal at 1575.42MHz with 1.023Mbps BPSK modulation. The signal level at the antenna is about -130dBm, spread over a 2.046MHz bandwidth, so the wanted signal is actually buried in noise. The high RF input compression point of the GP2010 means that with subsequent IF filtering it is possible to reject large out of band jamming signals, in particular 900MHz as used by mobile telephones. The on-chip PLL generates the first local-oscillator frequency at 1400MHz. The output of the front-end mixer (Stage 1) at 175.42 MHz can then be filtered before being applied to the second stage. The double-balanced stage 1 mixer outputs are open-collectors, and require external dc bias to V_{CC} .

The second stage contains further gain and a mixer with a local oscillator signal at 140 MHz giving a second IF at 35.42 MHz. The second stage mixer is also double-balanced with open-collector outputs requiring external dc bias to V_{CC} .

The signal from stage 2 is passed through an external filter with a 1dB bandwidth of 1.9MHz. The performance of this filter is critical to system performance and it is recommended that a SAW filter is used (part number DW9255, also available from GEC Plessey Semiconductors). The output of the filter then feeds the main IF amplifier. This includes 2 AGC amplifiers and a third mixer with a local oscillator signal at 31.111 MHz giving a final IF at 4.309 MHz. There is an on-chip filter after the third mixer which provides filtering centred on 4.309 MHz. The IF output, which has 1k Ω output impedance, is provided for test purposes. All of the signals within the IF amplifier are differential including the filter inputs and outputs, except the IF output (pin 1), to reduce any common mode interference.

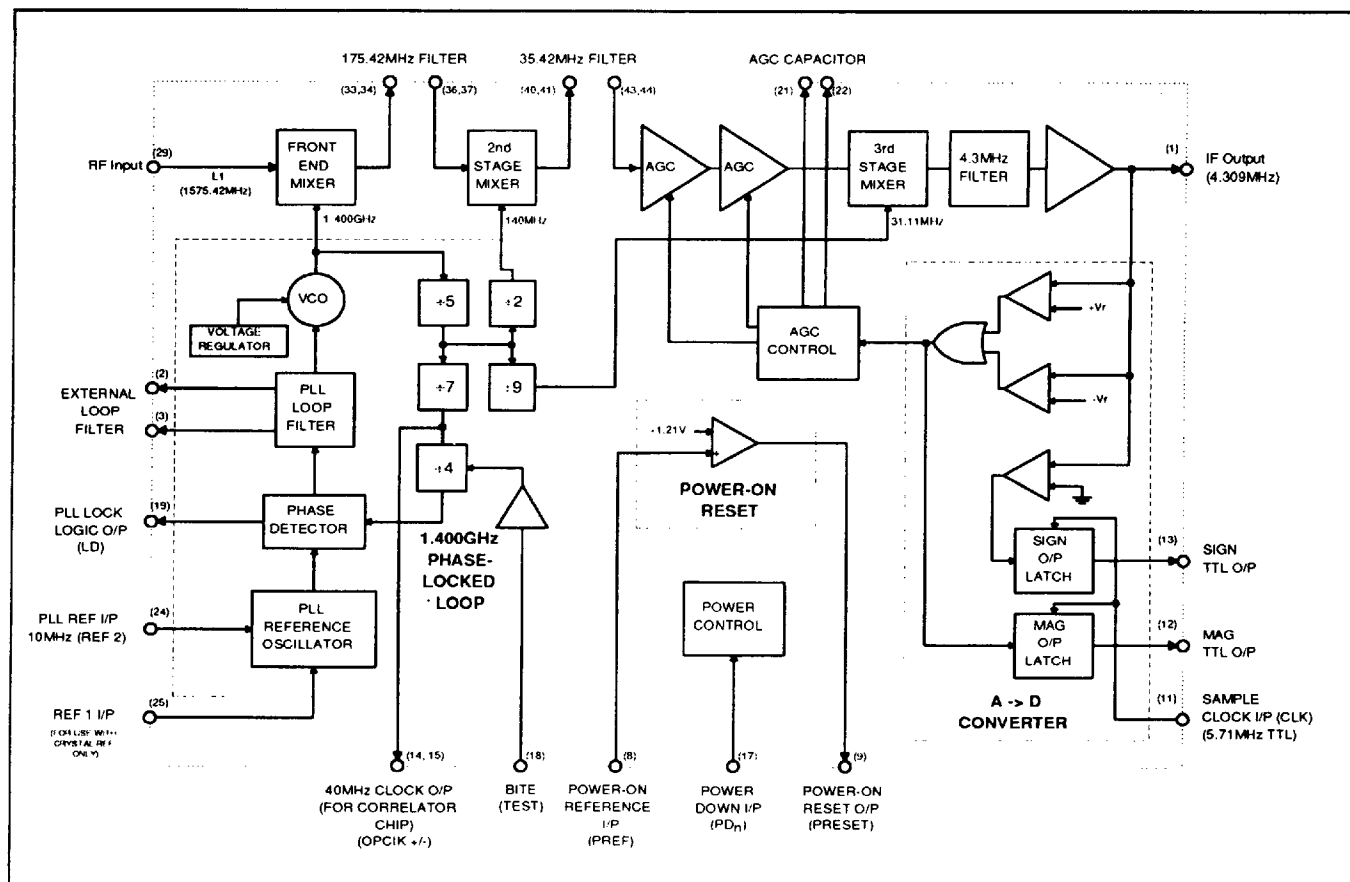


Fig. 2 Block diagram of GP2010

The IF output is fed to a 2-bit quantiser which provides sign and magnitude (MSB and LSB) outputs. The magnitude data controls the AGC loop, such that on average the magnitude bit is set (high) 30% of the time. The AGC time constant is set by an external capacitor.

The sign and magnitude data, SIGN (pin 13) and MAG (pin 12), are latched by the rising edge of the sample clock, CLK (pin 11), which is normally derived from the correlator; the GP2021 provides a 5.714MHz (=40/7) clock, giving a sampled IF centred on 1.405MHz.

The Digital Interface circuits use a separate power-supply, $V_{DD}(IO)$, which would normally be shared with the correlator to minimise crosstalk between the analog and digital sections of the device.

ON-CHIP PHASE-LOCKED LOOP SYNTHESISER

All of the local oscillator signals are derived from an on chip phase locked loop synthesiser. This includes a 1400MHz VCO complete with on-chip tank circuit, dividers and phase detector, with external loop filter components. A 10.000MHz reference frequency is required for the PLL. This can be achieved by attaching an external 10.000MHz crystal to the on-chip PLL reference oscillator (see figure 5). However in most applications the user will need an external source, such as a TCXO, to provide greater frequency stability (see figure 6). An external reference should be ac coupled to REF2 (pin 24); REF 1 (pin 25) should be left open circuit.

The three local oscillator signals 1400MHz, 140.0MHz and 31.11MHz are derived from the 1400MHz synthesiser output. The synthesiser also provides a 40 MHz balanced differential output clock (pins 14 & 15) which can be used to clock the GP2021 correlator. The clock is a low level differential signal which helps minimise interference with the analog areas of the circuit. A PLL lock-detect output, LD (pin 19), is also provided, which is logic high when the PLL is phase-locked to the 10.000MHz reference signal.

The VCO power-supply incorporates an on-chip regulator to improve the noise-immunity of the PLL. This feature is only available when operating with a 5 volt (nominal) supply which is regulated to 3.3 volts internally. This internal regulated supply is referenced to $V_{CC}(OSC)$ (pin 5). Figure 7 shows the required connections for both 3 volt and 5 volt operation.

A further feature of the circuit is the TEST input (pin 18). When this input is held high the PLL is unlocked with the VCO at its maximum frequency.

POWER-DOWN CAPABILITY

A power down function is provided on the GP2010, to limit power consumption. This powers down the majority of the circuit except the "power-on reset" function (see below).

If the power down feature is not required, the Power-down input, PD_n (pin 17), should be connected to 0V dc (=Vee/Ground).

POWER-ON RESET FUNCTION

The GP2010 includes a voltage detector which operates from the digital interface supply. This circuit is used to produce a TTL logic low output while the GPS receiver power supply is switching on, and produces a logic high output when the power supply voltage has achieved a nominal value. This output can be used to disable the GP2021 correlator while the power supply is switching on. An internal bandgap reference of approximately +1.21V is compared with the voltage on a sense pin, PRef (pin 8); when the voltage on this pin exceeds the reference, a TTL logic high level appears at the Power-on Reset output, PReset (pin 9). Thus, if the sense input voltage is derived from an external resistive divider from the Digital Interface supply, $V_{DD}(IO)$ (pin 16), such that the sense voltage at nominal V_{CC} is V_S , then the supply threshold, $V_{CC}(thresh)$, at which the PReset output goes to logic high is:-

$$V_S = \frac{V_{CC} (nom) \times 1.21}{V_{CC} (thresh)}$$

For a $V_{CC} (nom)$ of 5.0V, $V_{CC} (thresh)$ may be set to approx. 4.0V, giving V_S of 1.5V.

For a $V_{CC} (nom)$ of 3.0V, $V_{CC} (thresh)$ may be set to approx. 2.4V, giving V_S of 1.5V.

ADDITIONAL INFORMATION

All the digital inputs and outputs can use a separate power supply to help prevent digital switching transitions interacting with the analog sections of the device, and as an additional precaution, the digital inputs and outputs are on the opposite side of the device to the critical analog pins.

ELECTRICAL CHARACTERISTICS

The Electrical Characteristics are guaranteed over the following range of operating conditions (see Fig. 3 for test circuit):

Industrial (I) grade: $T_{AMB} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Supply voltage: V_{CC} and $V_{DD} = +2.7\text{V}$ to $+5.5\text{V}$

Test conditions (unless otherwise stated):

Supply voltages: $V_{CC} = +2.7\text{V}$ and $+5.5\text{V}$, $V_{DD} = +2.7\text{V}$ and $+5.5\text{V}$

Test temperature: Industrial (I) grade product: $+25^{\circ}\text{C}$

| Characteristic | Value | | | Units | Conditions |
|-------------------------------------|-----------|------|------|--------|---|
| | Min. | Typ. | Max. | | |
| SUPPLY CURRENT | | | | | |
| Normal mode - Analog interface | | 55 | 77 | mA | Pins 5, 23, 26, 32, 35, 42 |
| - Digital interface | | 9 | 14.5 | mA | Pin 16 |
| Power down mode - Analog interface | | 3 | 6 | mA | Pins 5, 23, 26, 32, 35, 42 |
| - Digital interface | | 3 | 5 | mA | Pin 16 |
| Power Supply Differential | | | 100 | mV | Between any V _{CC} /V _{DD} pins (Note 7) |
| Power down Response time | | 3 | | µs | (Note 7) |
| IF STRIP | | | | | |
| Front End/Mixer 1 | | | | | |
| Conversion Gain (G1) | 11 | 18 | 25 | dB | R _O = 600Ω (Note 2) F _{IN} = 1575.42MHz Z _S = 50Ω (Note 7) |
| Noise Figure | | 9 | | dB | |
| Input Compression (1dB) | -22 | -16 | | dBm | |
| Input Impedance | | 15 | | Ω | Pin 29 (Notes 1 and 7) |
| | | 3.6 | | nH | (Notes 1 and 7) |
| Differential Output Impedance | | 700 | | Ω | Pins 33 & 34 (Note 8) |
| RF Input Image Rejection | | 8 | | dB | F _{IN} = 1224.58MHz (Note 7) |
| Stage 2/Mixer 2 | | | | | |
| Conversion Gain (G2) | 22 | 27 | 33 | dB | F _{IN} = 175.42MHz |
| Input Compression (1dB) | 5 | 14 | | mV rms | |
| Differential Input Impedance | | 700 | | Ω | Pins 36 & 37 (Note 8) |
| Differential Output Impedance | | 500 | | Ω | Pins 40 & 41 (Note 8) |
| Stage 3 | | | | | |
| High Gain (In terms of total strip) | 106-G1-G2 | | | dB | (Note 6) |
| High Gain (G3) | | 75 | | dB | F _{IN} = 35.42MHz |
| Gain Control Range | | 60 | | dB | (Note 3) |
| Differential Input Impedance | | 1 | | kΩ | Pins 43 & 44 (Note 8) |
| IF Output amplitude | 60 | 85 | 120 | mV rms | CW input (Note 3) |
| IF Output impedance | | 1 | | kΩ | Pin 1 (Note 8) |
| 4.3MHz Filter Response | | | | | |
| Flatness 4.3 ± 1MHz | -1.5 | | +1.0 | dB | |
| Rejection @ 0.5MHz | | 14 | | dB | (Note 7 and 9) |
| @ 50MHz | 45 | 70 | | dB | |
| 2 BIT QUANTISER | | | | | |
| Sign Duty Cycle | 40 | 50 | 60 | % | } (Note 10) C _{AGC} = 100nF |
| Mag Duty Cycle | 20 | 30 | 40 | % | |
| AGC Time Constant | | 2 | | ms | |
| ON-CHIP PLL SYNTHESISER | | | | | |
| Phase Noise | | | | | |
| ± 1kHz | | -68 | | dBc/Hz | } (Note 7) 15kHz Loop Bandwidth |
| ± 10kHz | | -75 | | dBc/Hz | |
| ± 100kHz | | -88 | | dBc/Hz | |
| ± 1MHz | | -110 | | dBc/Hz | |
| ± 5MHz | | -120 | | dBc/Hz | |
| ± 50MHz | | -120 | | dBc/Hz | |
| PLL Spurs | | -50 | | dBc | (Note 7) |

| Characteristic | Value | | | Units | Conditions |
|--|-----------------------|----------------------|----------------------|------------|---------------------------------------|
| | Min. | Typ. | Max. | | |
| VCO Maximum Lock Frequency | 1414 | | | MHz | |
| VCO Minimum Lock Frequency | | | 1386 | MHz | |
| VCO regulator output voltage | 3 | 3.3 | 3.5 | V | (Note 4) |
| VCO Gain | 50 | 150 | 240 | MHz/V | |
| Phase Detector Gain | | 5.3 | | V/rad | (Note 7) |
| 10MHz Reference Input | 0.1 | 0.6 | 1.2 | V pk-pk | Pin 24 |
| 10MHz Reference Input Impedance | | 5 | | k Ω | (Note 11) |
| PLL Lockup Time | | 6 | | ms | From Power up (Note 7) |
| PLL Loop Gain | | 150 | | dB | (Note 7) |
| DIGITAL INTERFACES Sample Clock, Power Down, Test Inputs. | | | | | Pins 11, 17, 18 |
| V _{IH} | 2 | | V _{DD} | V | |
| V _{IL} | 0 | | 0.5 | V | |
| Input Current High I _{IH} | | | 10 | μ A | V _{IH} = V _{DD} |
| Input Current Low I _{IL} | -300 | | | μ A | V _{IL} = V _{EE} |
| Sign/Mag Outputs | | | | | Pins 13, 12 |
| V _{OH} | V _{DD} -1 | | | V | I _O = -0.5mA |
| V _{OL} | | | 0.5 | V | I _O = 0.5mA |
| Sample Clock to Sign/Mag Delay | | 20 | | ns | CL = 15pF, RL = 15k Ω (Note 7) |
| 40MHz Clock Output | | | | | |
| High Level (V _{OH}) | V _{DD} -1.25 | V _{DD} -1 | V _{DD} -0.8 | V | Pins 14 & 15 |
| Low Level (V _{OL}) | | V _{OH} -0.1 | | V | (Note 5) |
| Output (differential) | | 220 | | mV p-p | CL = 15pF (GND) (Note 7) |
| | | | | | CL = 5pF (Diff) (Note 7) |
| Duty Cycle | | 43 | | % | (Note 7) |
| LD (PLL Lock)/PReset Outputs | | | | | Pins 19 and 9 |
| Low Level (V _{OL}) | | 0.2 | 0.5 | V | I _O = 0.5mA |
| High Level (V _{OH}) | V _{DD} -1 | V _{DD} | | V | I _O = -10 μ A |
| Power-on Reset comparator input | | | | | Pin 8 |
| Power Reset Reference Level | 1.1 | | 1.35 | V | |
| Power Reset Reference Input Current | -10 | | 10 | μ A | |

Notes On Electrical Characteristics:- All RF measurements are made with appropriate matching to the input or output impedances, such as balun transformers, and levels refer to matched 50ohm ports (see figure 3 for test circuit)

1. RF input impedance (series) without input matching components connected - expressed as Real impedance with reactive inductor value. Measured at 1575.42MHz.
2. Input matched to 50ohm, output loaded with 600ohms differential
3. Maximum Stage 3 input signal amplitude for correct AGC operation = 20mV rms.
4. VCO regulator voltage measured with respect to Vcc (OSC) - pin 5.
5. OPCLK outputs are differential and are referenced to V_{DD}.
6. Minimum gain requirement expressions:

$$-7\text{dBm} < -174\text{dBm/Hz} + 19\text{dB} + G1 + G2 + G3 - 21\text{dB} + 63\text{dB}$$

where -7dBm = typical IF Output level with AGC active (equivalent to 100mV rms)

-174dBm/Hz = background noise level at RF input

19dB = sum of LNA gain and noise figure

-21dB = total loss in 175MHz and 35MHz filters

63dB = summation of noise over a 2MHz bandwidth

Rearranging the above expression gives $G1 + G2 + G3 > 106\text{dB}$.

7. This parameter is not production tested.
8. This impedance is toleranced at +/-30% and is not production tested.
9. Roll off occurs in on-chip capacitive coupling IF Output to input of ADC circuit. Not measurable at IF Output.
10. CW input on pins 43 & 44 of 35.42MHz at 7mV rms.
11. This input impedance applies to the typical input level. The impedance is level dependent and is not tested or guaranteed.

PIN DESCRIPTIONS

All V_{EE} and V_{CC}/V_{DD} pins should be connected to ensure reliable operation

| Pin No. | Signal Name | Input/Output | Description |
|---------|----------------|--------------|---|
| 1 | IFOutput | Output | IF Test output. Connected to output of Stage 3 prior to the A to D converter. A series 1k Ω resistor is incorporated for buffering purposes. |
| 2 | PLL Filt1 | Output | PLL Filter 1. Connected to the bias network within the on-chip VCO. An external PLL loop filter network should be connected between this pin and PLL Filt 2 (see below). |
| 3 | PLL Filt2 | Output | PLL Filter 2. Connected to the varactor diodes within the on-chip VCO. An external PLL loop filter network should be connected between this pin and PLL Filt 1 (see above). |
| 4,6 | V_{EE} (OSC) | Input | Negative supply to the on-chip VCO. (See Note 1) |
| 5 | V_{CC} (OSC) | Input | Positive supply to the on-chip VCO. |
| 7 | V_{EE} (REG) | Input | Negative supply to the VCO regulator. This must be connected to GND. |
| 8 | PRef | Input | Power-on Reset Reference input. An on-chip comparator produces a logic HI when the PRef input voltage exceeds +1.21V. (Nom) (See Page 3). |
| 9 | PReset | Output | Power-on Reset Output. A TTL compatible output controlled by the Power-on reset comparator (See above). This output remains active even when the chip is powered down. (See pin 17 - PDn). |
| 10 | V_{EE} (IO) | Input | Negative supply to the Digital Interface. (See Note 2) |
| 11 | CLK | Input | Sample Clock input from the correlator chip. A TTL compatible input (which operates at 5.714MHz if used with GP2021 correlator device) used to clock the MAG & SIGN output latches, on the rising edge of the CLK signal. |
| 12 | MAG | Output | Magnitude bit data output. A TTL compatible signal, representing the <i>magnitude</i> of the mixed down IF signal. Derived from the on-chip 2-bit A to D converter, synchronised to the CLK input clock signal. |
| 13 | SIGN | Output | Sign bit data output. A TTL compatible signal, representing the <i>polarity</i> of the mixed down IF signal. Derived from the on-chip 2-bit A to D converter, synchronised to the CLK input clock signal. |
| 14 | OPClk- | Output | 40MHz Clock output - inverse phase. One side of a balanced differential output clock, with opposite polarity to Pin 15 - OPClk+. Used to drive a master-clock signal within the correlator chip. |
| 15 | OPClk+ | Output | 40MHz Clock output - true phase. Other side of a balanced differential output clock set, with opposite polarity to Pin 14 - OPClk-. Used to drive a master-clock signal within the correlator chip. |
| 16 | V_{DD} (IO) | Input | Positive supply to the Digital Interface. (See Note 2) |

| Pin No. | Signal Name | Input/Output | Description |
|----------------|----------------|--------------|---|
| 17 | PDn | Input | Power-Down control input. A TTL compatible input, which when set to logic high, will disable ALL of the GP2010 functions, except the power-on reset block. Useful to reduce the total power consumption of the GP2010. If this feature is not required, the pin should be connected to 0V (V_{EE}/GND). |
| 18 | TEST | Input | Test control input - Disable PLL. A TTL compatible input, which when set to logic high, will disable the on-chip PLL, by disconnecting the divided-down VCO signal to the phase-detector. The VCO will free run at its upper range of frequency operation. If this feature is not required, the pin should be connected to 0V (V_{EE}/GND). |
| 19 | LD | Output | PLL Lock Detect output. A TTL compatible output, which indicates if the PLL is phase-locked to the PLL reference oscillator. Will become logic high only when phase-lock is achieved. |
| 20 | V_{EE} (DIG) | Input | Negative supply to the PLL and A to D converter. |
| 21 | AGC- | Output | AGC Capacitor output - inverse phase. One side of a balanced output from the AGC block within IF Stage 3, to which an external capacitor is connected to set the AGC time-constant. |
| 22 | AGC+ | Output | AGC Capacitor output - true phase. One side of a balanced output from the AGC block within IF Stage 3, to which an external capacitor is connected to set the AGC time-constant. |
| 23 | V_{CC} (DIG) | Input | Positive supply to the PLL and A to D converter. |
| 24 | REF 2 | Input | 10.000MHz PLL Reference signal input . Input to which an externally generated 10.000MHz PLL reference signal should be ac coupled, if an external PLL reference frequency source (e.g TCXO) is used (see fig. 6). If no external reference is used, this pin forms part of the on-chip PLL reference oscillator, in conjunction with an external 10.000MHz crystal (see fig. 5). |
| 25 | REF 1 | Input | PLL reference oscillator auxillary connection. Used in conjunction with Pin 24 (REF 2) to allow a 10.000MHz external crystal to provide the PLL reference signal if no external PLL reference frequency source (e.g TCXO) is used. This pin should NOT be connected if an external TCXO is being used (see fig. 5). |
| 26, 32 | V_{CC} (RF) | Input | Positive supply to the RF input and Stage 1 IF mixer. Both pins 26 & 32 (V_{CC} (RF)) are connected internally, but must both be connected to V_{CC} externally, to keep series inductance to a minimum. |
| 27, 28, 30, 31 | V_{EE} (RF) | Input | Negative supply to the RF input and Stage 1 IF mixer. Pins 27, 28, 30 & 31 are all connected internally, but must ALL be connected to 0V (V_{EE}/GND) externally, to keep series inductance to a minimum. |

| Pin No. | Signal Name | Input/Output | Description |
|---------|---------------|--------------|---|
| 29 | RF Input | Input | RF input. The GPS RF input signal @ 1575.42MHz from an external antenna with LNA and filter is connected to this pin via an input-matching network (see fig.4). |
| 33 | O/P 1- | Output | Stage 1 mixer output @ 175.42MHz - inverse phase. One of a balanced output from first stage IF mixer, to which one input of an external balanced 175MHz bandpass filter is connected. External dc biasing is required via an inductor connected to $V_{CC}(RF)$ - the value of which is dependent on the filter used. |
| 34 | O/P 1+ | Output | Stage 1 mixer output @ 175.42MHz - true phase. Second of a balanced output from first stage IF mixer, to which the second input of an external balanced 175MHz bandpass filter is connected. External dc biasing is required via an inductor connected to $V_{CC}(RF)$ - the value of which is dependent on the filter used. |
| 35 | V_{CC} (2) | Input | Positive supply to the Stage 2 IF mixer. |
| 36 | I/P 2- | Input | Stage 2 mixer input @ 175.42MHz - inverse phase. One of a balanced input to the second stage IF mixer, to which one of the balanced signal outputs from the external 175MHz bandpass filter is connected. |
| 37 | I/P 2+ | Input | Stage 2 mixer input @ 175.42MHz - true phase. Second of a balanced input to the second stage IF mixer, to which the second of the balanced signal outputs from the external 175MHz bandpass filter is connected. |
| 38,39 | V_{EE} (IF) | Input | Negative supply to the Stage 2 IF mixer, and Stage 3 IF block. |
| 40 | O/P 2- | Output | Stage 2 mixer output @ 35.42MHz - inverse phase. One of a balanced output from second stage IF mixer, to which one input of an external balanced 35.42MHz bandpass filter is connected. External dc biasing is required via an Inductor connected to V_{CC} . (See Note 3) |
| 41 | O/P 2+ | Output | Stage 2 mixer output @ 35.42MHz - true phase. Second of a balanced output from second stage IF mixer, to which the second input of an external balanced 35.42MHz bandpass filter is connected. External dc biasing is required via an Inductor connected to V_{CC} . (See Note 3) |
| 42 | V_{CC} (3) | Input | Positive supply to the Stage 3 IF mixer. |
| 43 | I/P 3- | Input | Stage 3 mixer input @ 35.42MHz - inverse phase. One of a balanced input to the third stage IF mixer, to which one of the balanced signal outputs from the external 35.42MHz bandpass filter is connected. (See Note 3) |
| 44 | I/P 3+ | Input | Stage 3 mixer input @ 35.42MHz - true phase. Second of a balanced input to the third stage IF mixer, to which the second of the balanced signal outputs from the external 35.42MHz bandpass filter is connected. (See Note 3) |

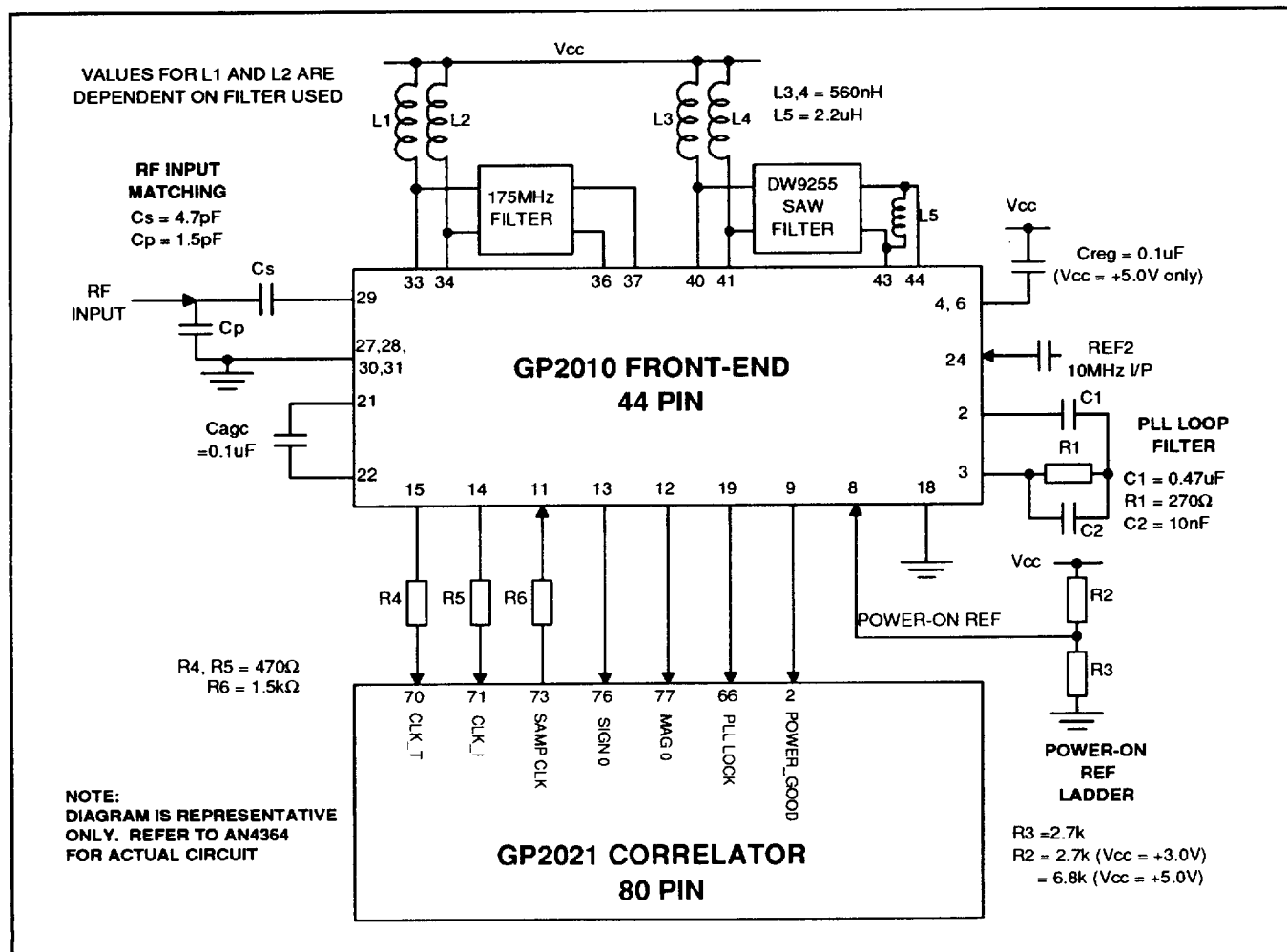


Fig. 4 GP2010 typical application

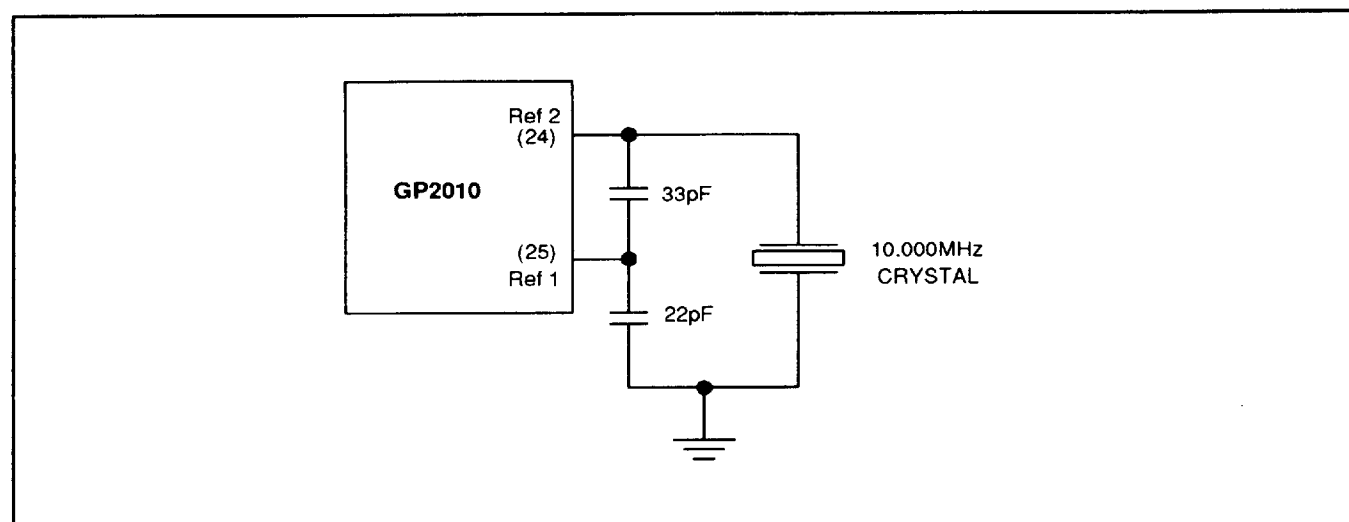


Fig. 5 Crystal Reference connections

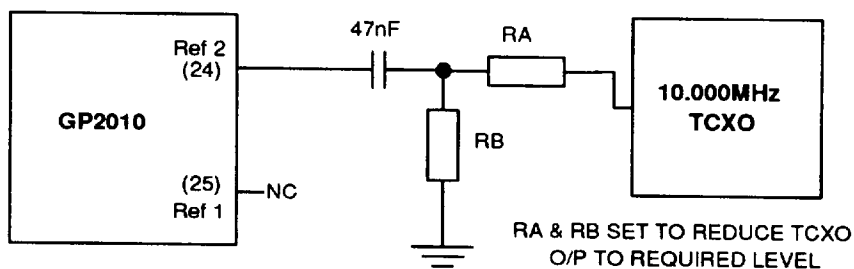


Fig. 6 TCXO Reference connections

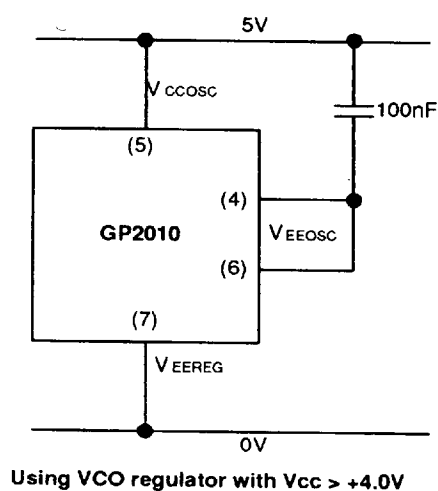
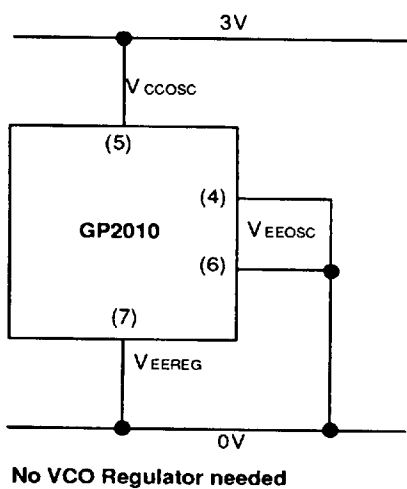


Fig. 7 VCO power-supply connections

TYPICAL CHARACTERISTICS OF THE GP2010 GPS RECEIVER RF FRONT-END

The GP2010 has been characterised to guarantee reliable operation over the Industrial Temperature range (-40°C \rightarrow $+85^{\circ}\text{C}$ ambient). This was achieved by setting the device case temperature to extremes of $+110^{\circ}\text{C}$ and -50°C . The following charts show the typical variation of key parameters across the extended case temperature range.

NOTE:- ALL Measurements at $V_{CC} = +2.65\text{V}$ made with VCO voltage-regulator *DISABLED*.

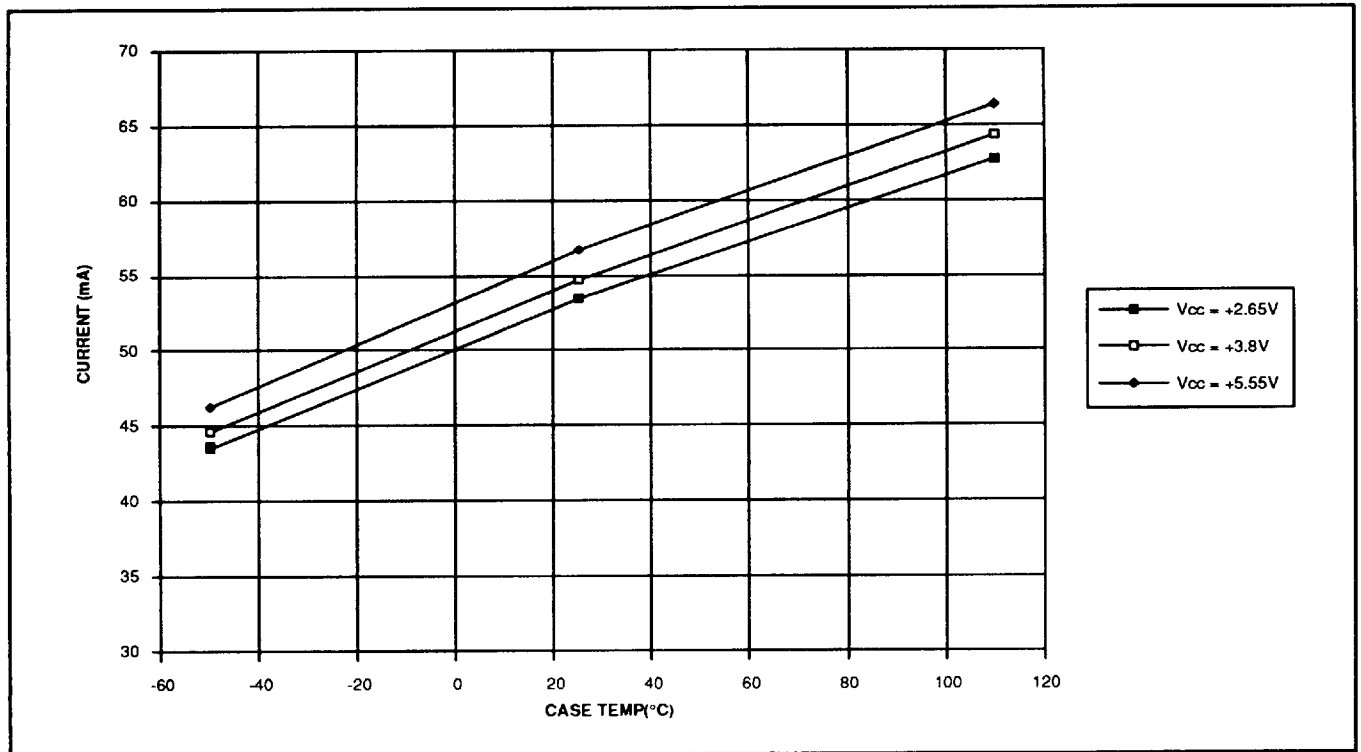


Fig. 8 Supply Current - Analog interface - normal mode

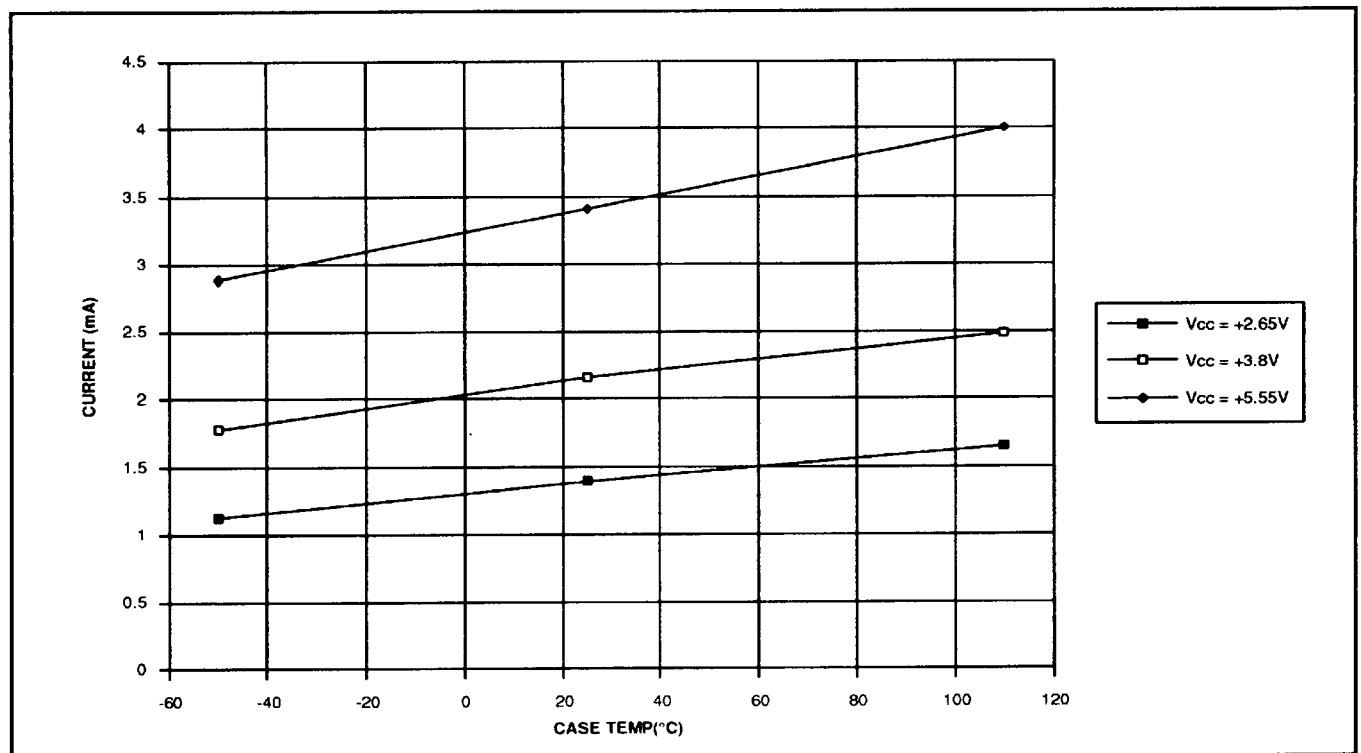


Fig. 9 Supply Current - Analog interface - power-down mode

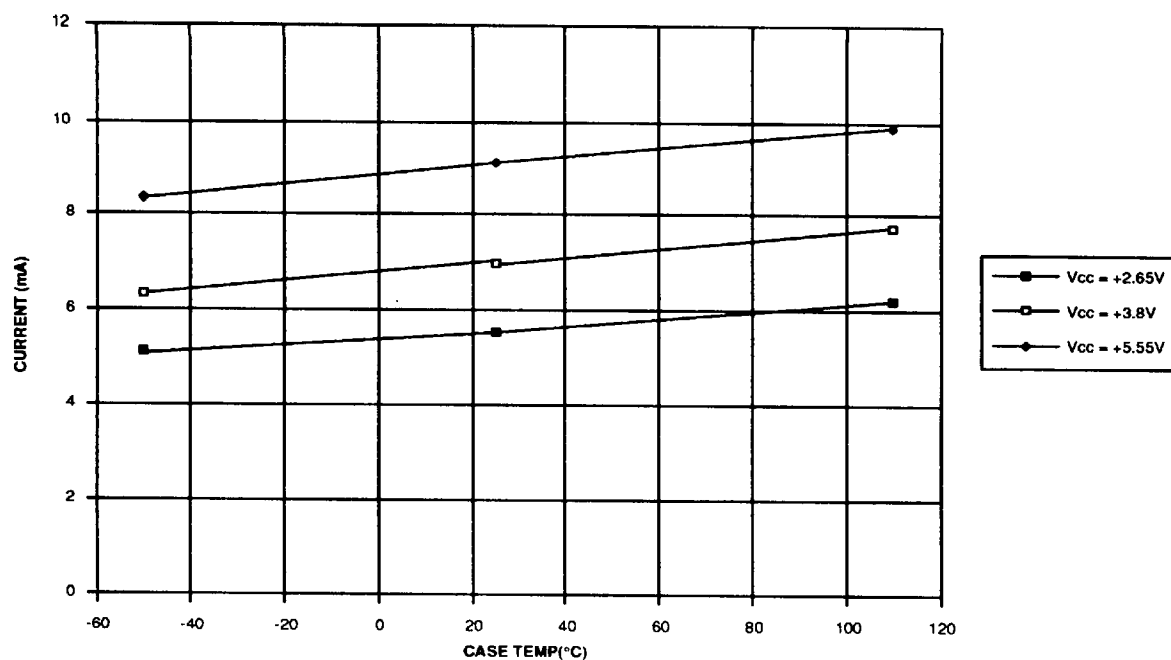


Fig. 10 Supply Current - Digital interface - normal mode

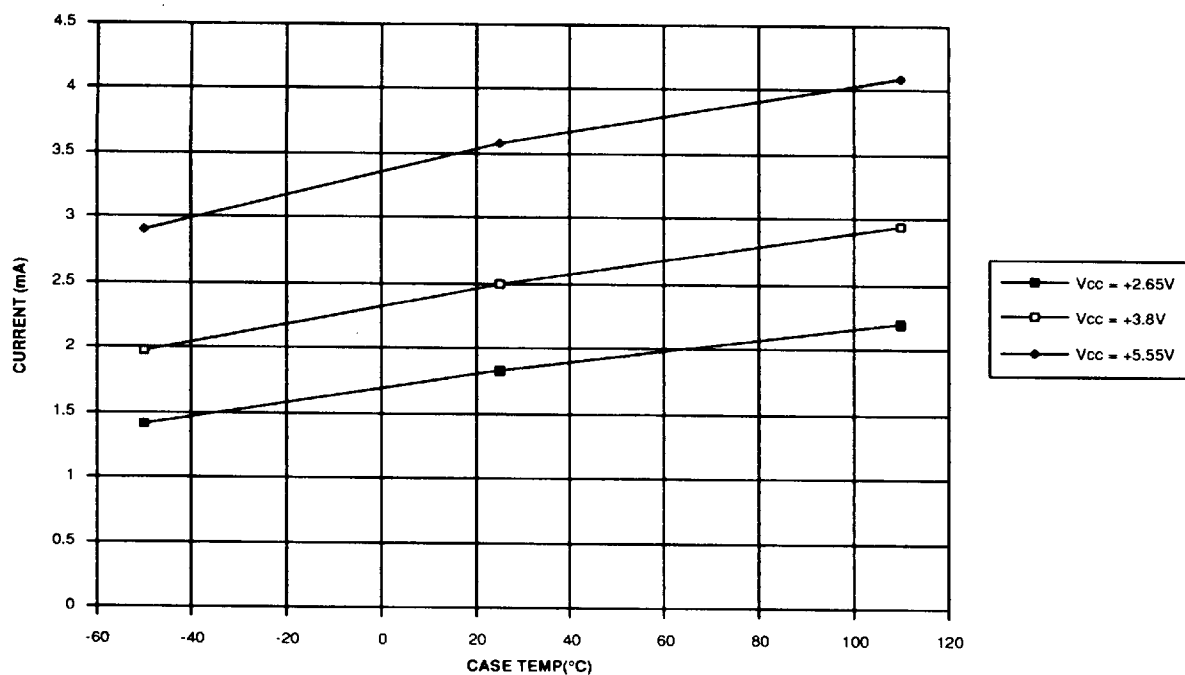


Fig. 11 Supply Current - Digital interface - power-down mode

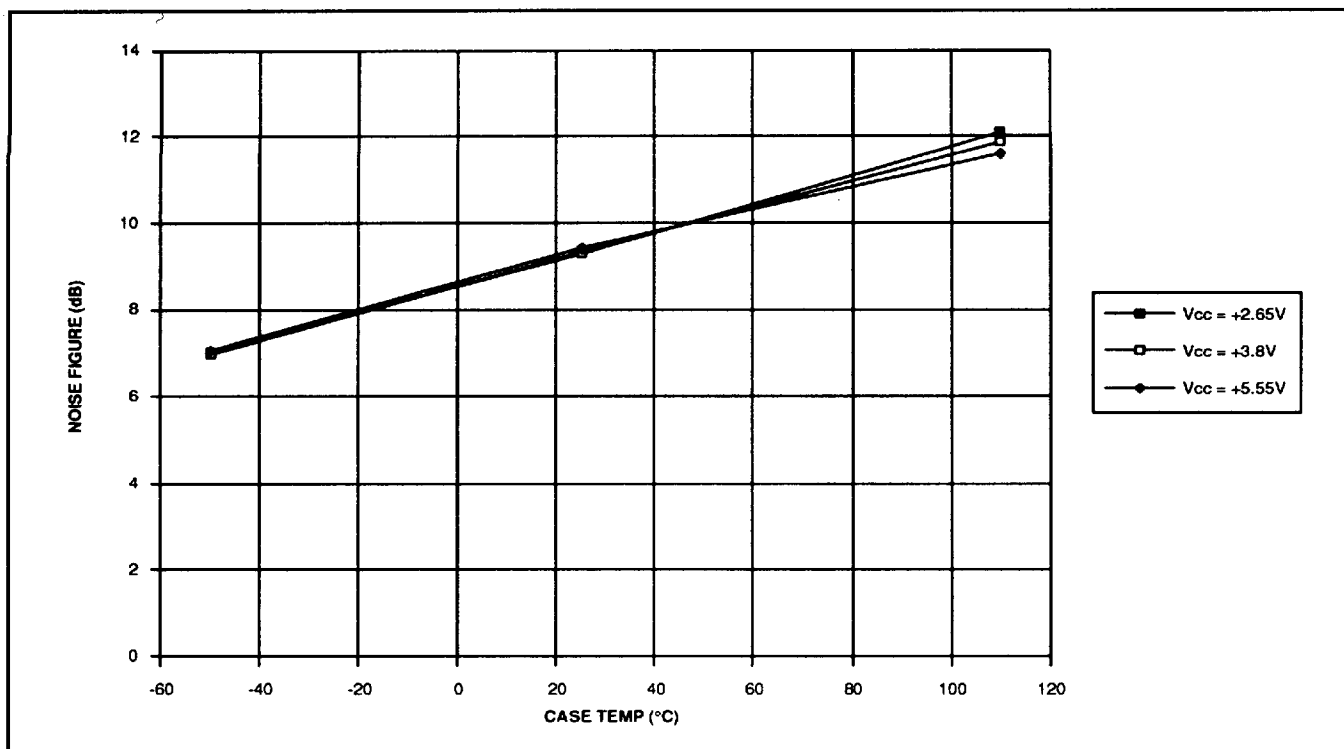


Fig. 12 Noise figure of IF chain in a typical application circuit

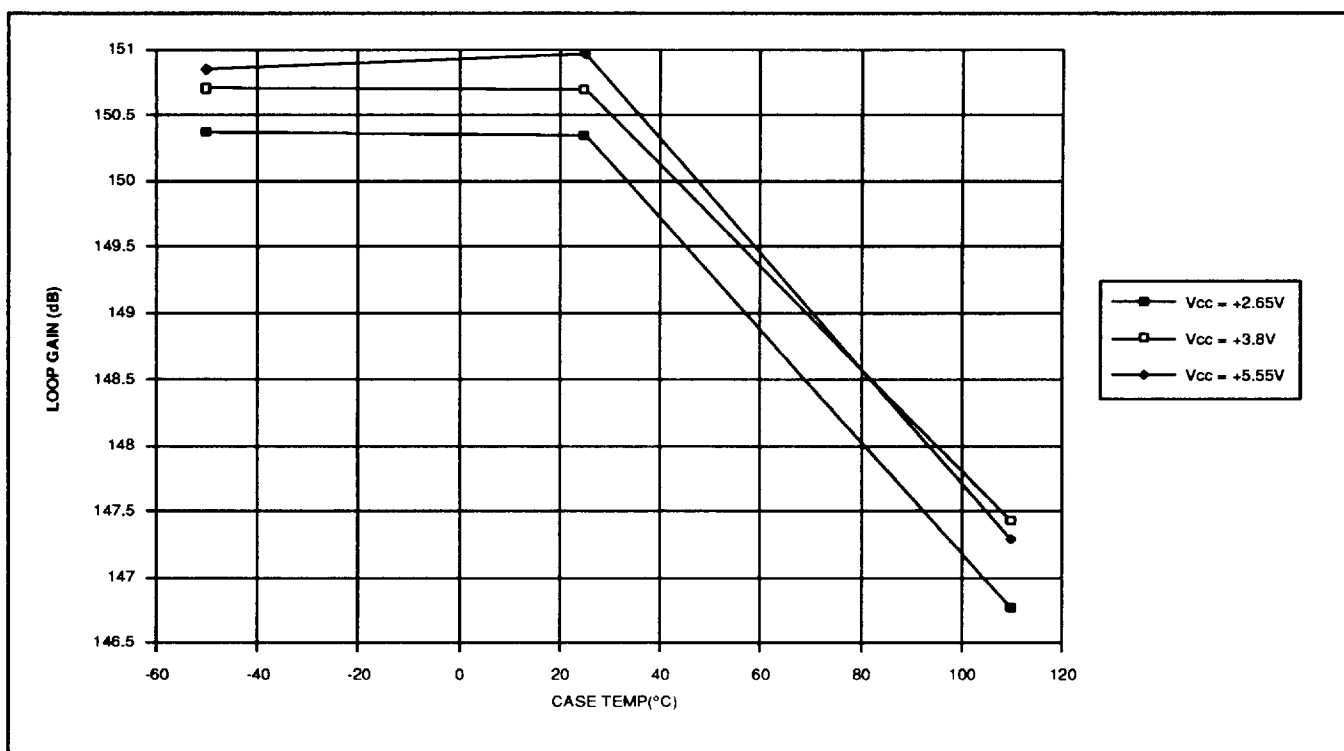


Fig. 13 On-chip Phase-locked-loop Synthesiser Loop gain

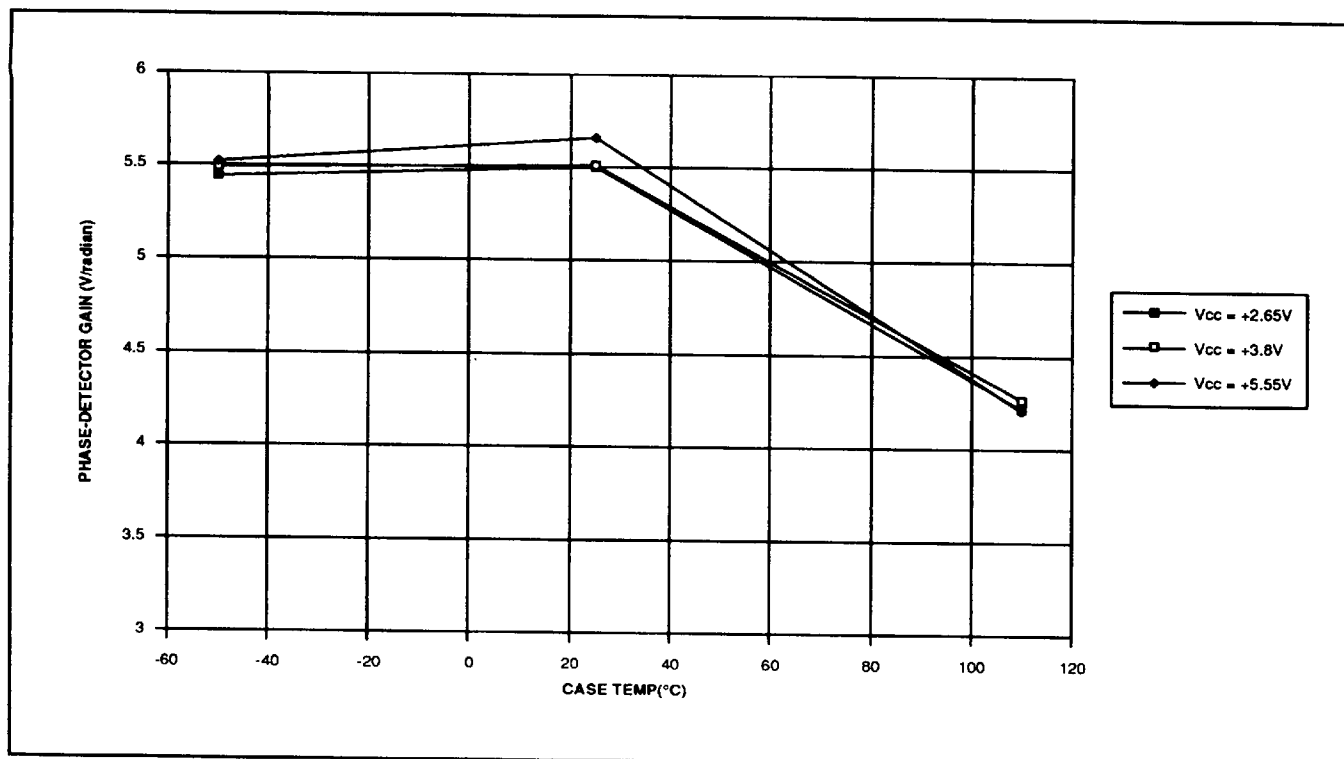


Fig. 14 On-chip Phase-locked-loop Synthesiser Phase-detector gain

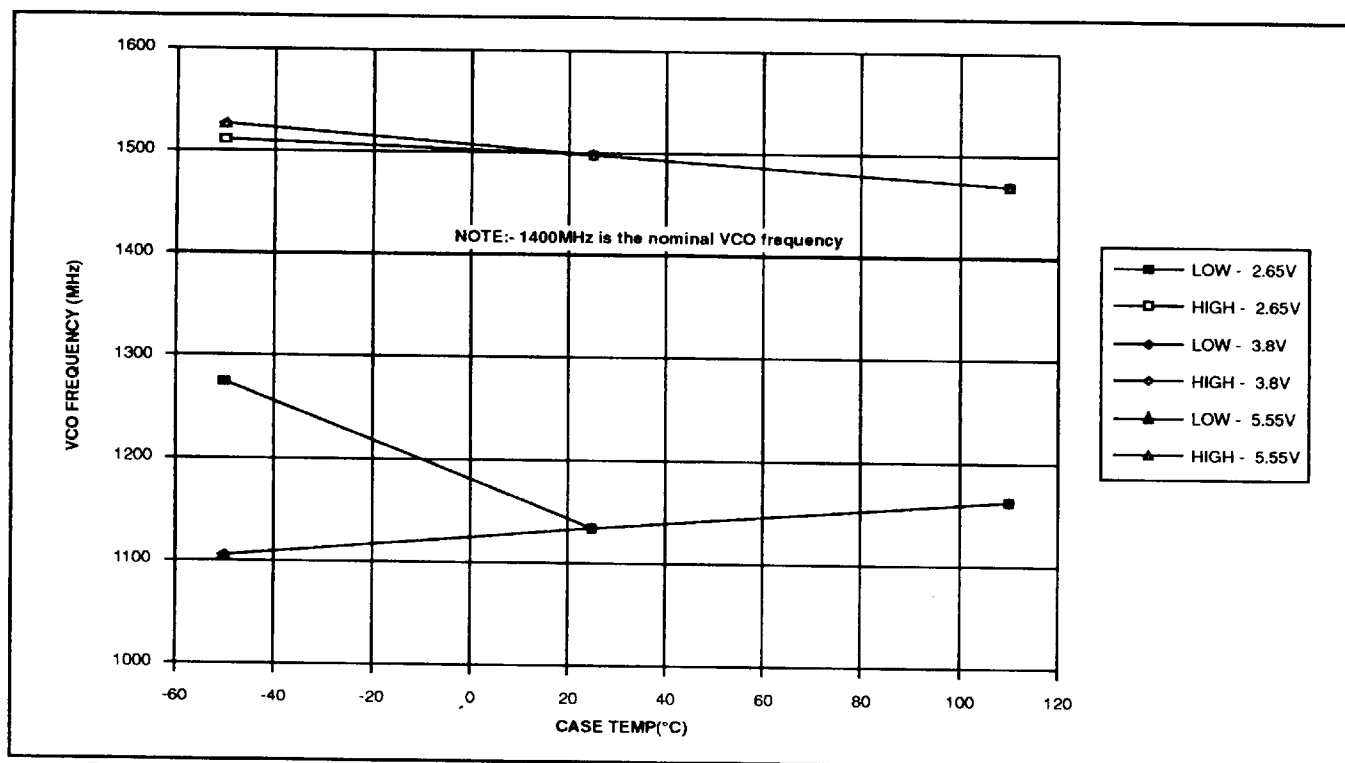


Fig. 15 On-chip Phase-locked-loop Synthesiser - LOW and HIGH limits of VCO frequency for PLL to be locked
(Note that this a typical characteristic and cannot be guaranteed)

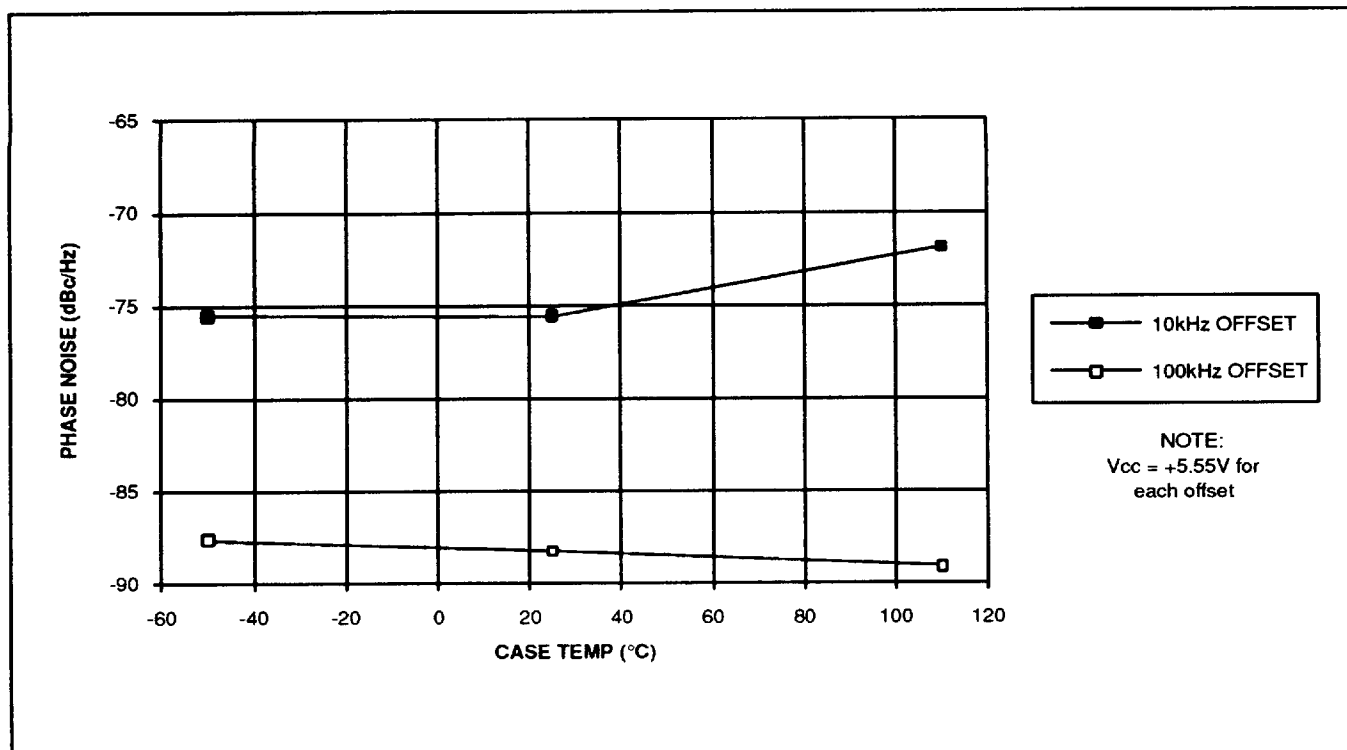


Fig. 16 On-chip Phase-locked-loop Synthesiser - Phase-noise of VCO producing 1400MHz CW signal at 10kHz offset (15kHz PLL loop bandwidth)

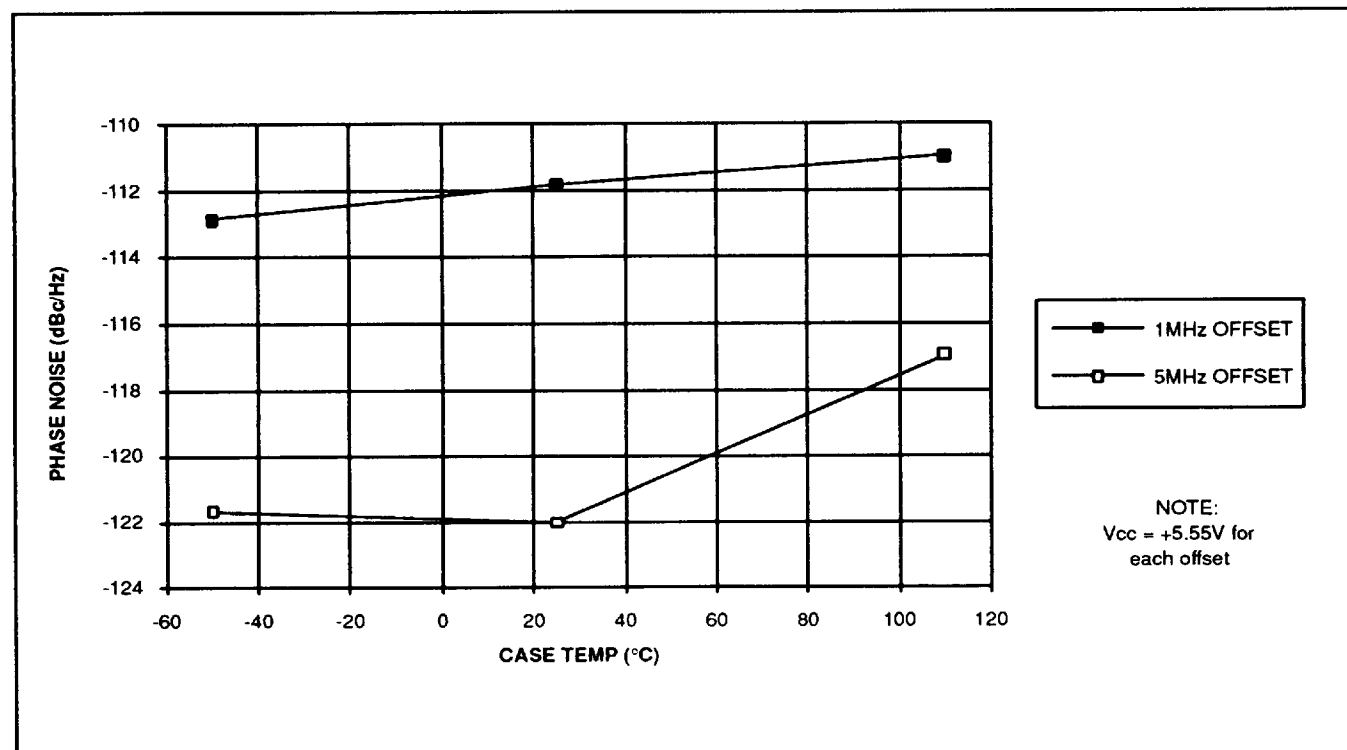


Fig. 17 On-chip Phase-locked-loop Synthesiser - Phase-noise of VCO producing 1400MHz CW signal at 100kHz offset (15kHz PLL loop bandwidth)

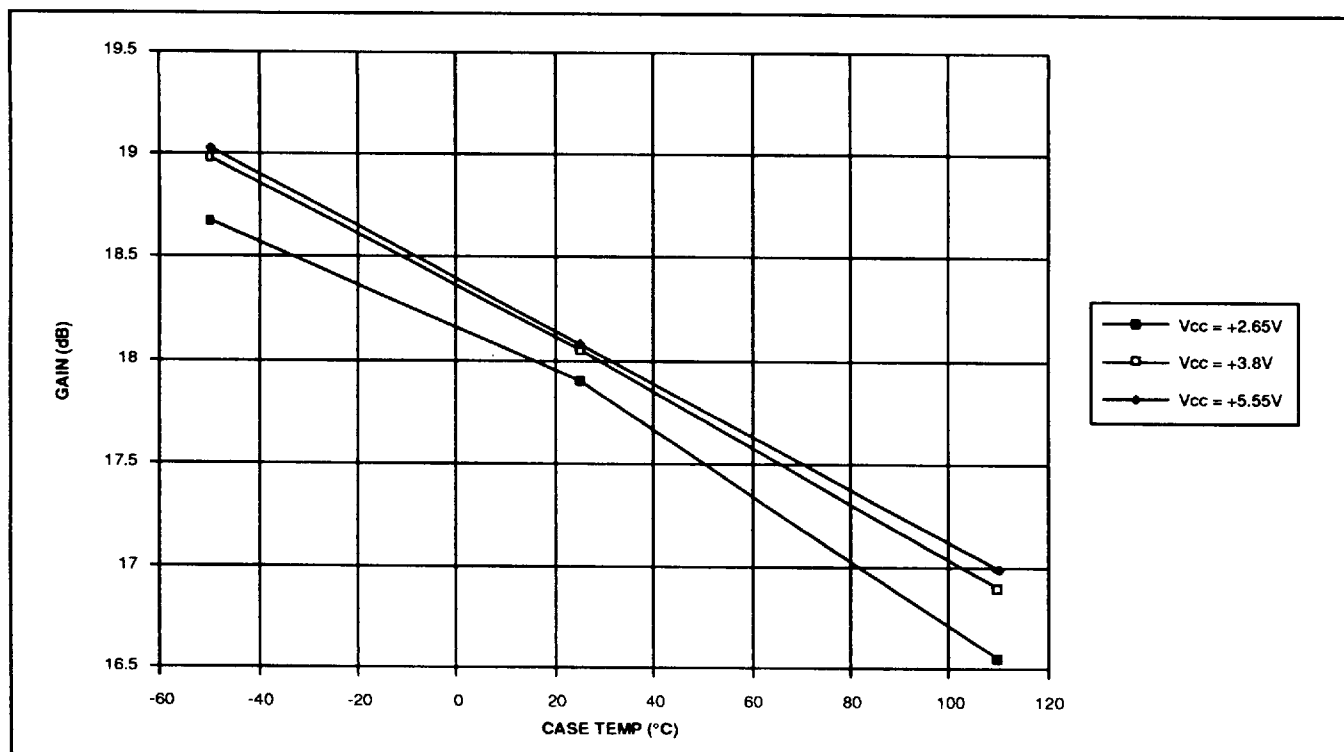


Fig. 18 Frontend/Mixer 1 Small-signal Conversion Gain - RF I/P frequency at 1575.42MHz

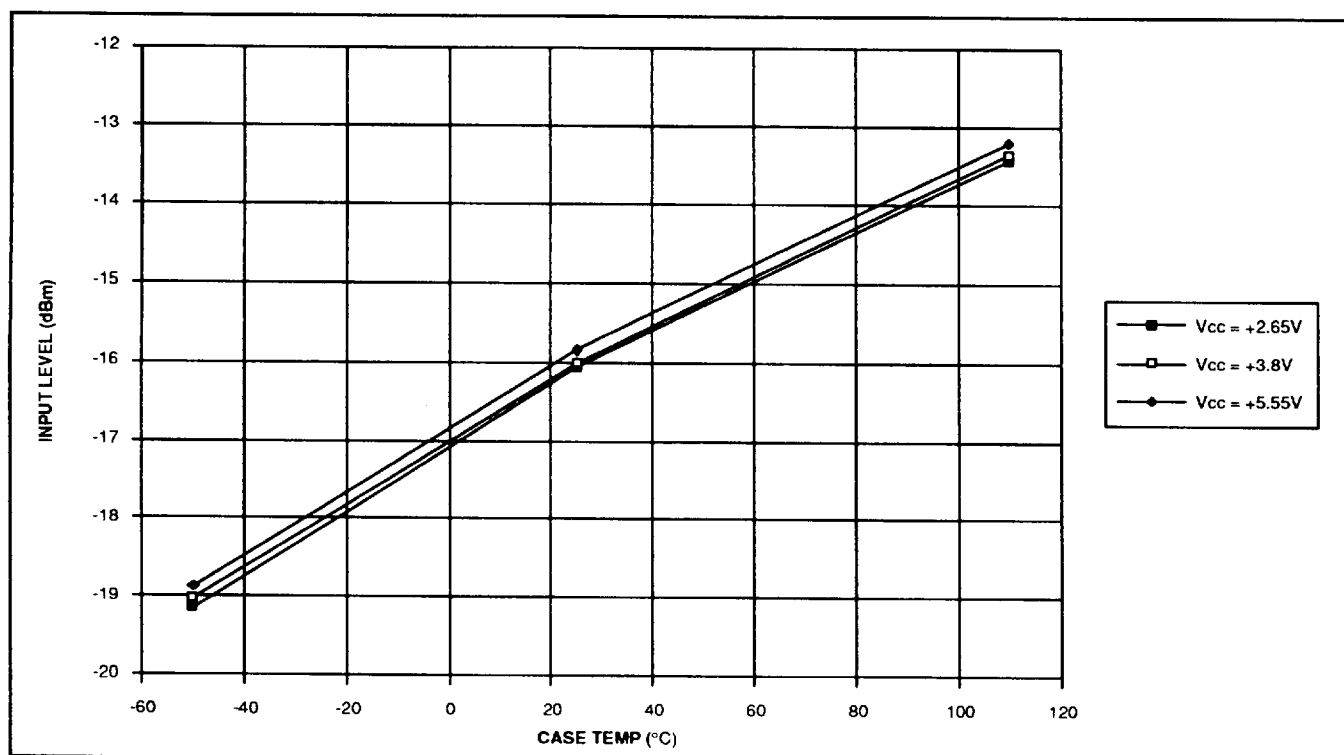


Fig. 19 Frontend/Mixer 1 Input level for 1dB Conversion Gain-compression - RF I/P frequency at 1575.42MHz

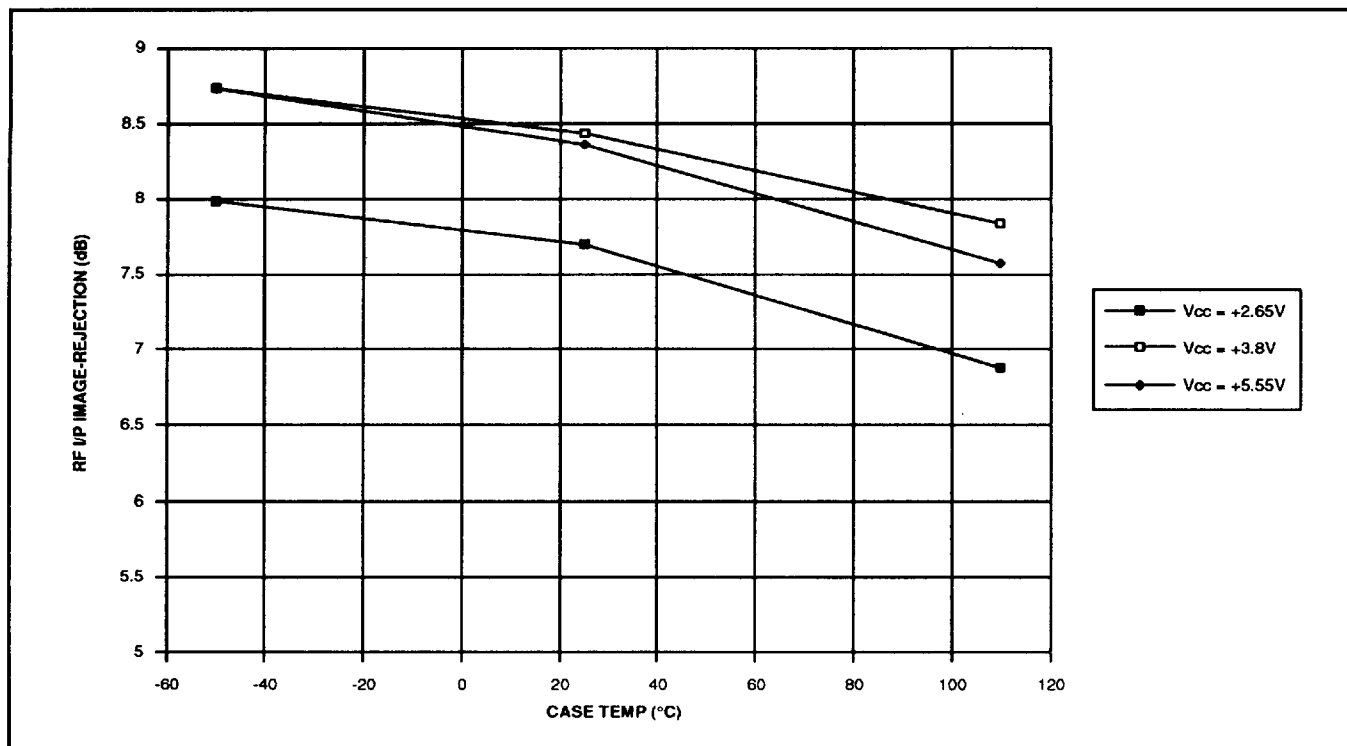


Fig. 20 Frontend/Mixer 1 Image rejection - RF I/P frequency at 1224.58MHz

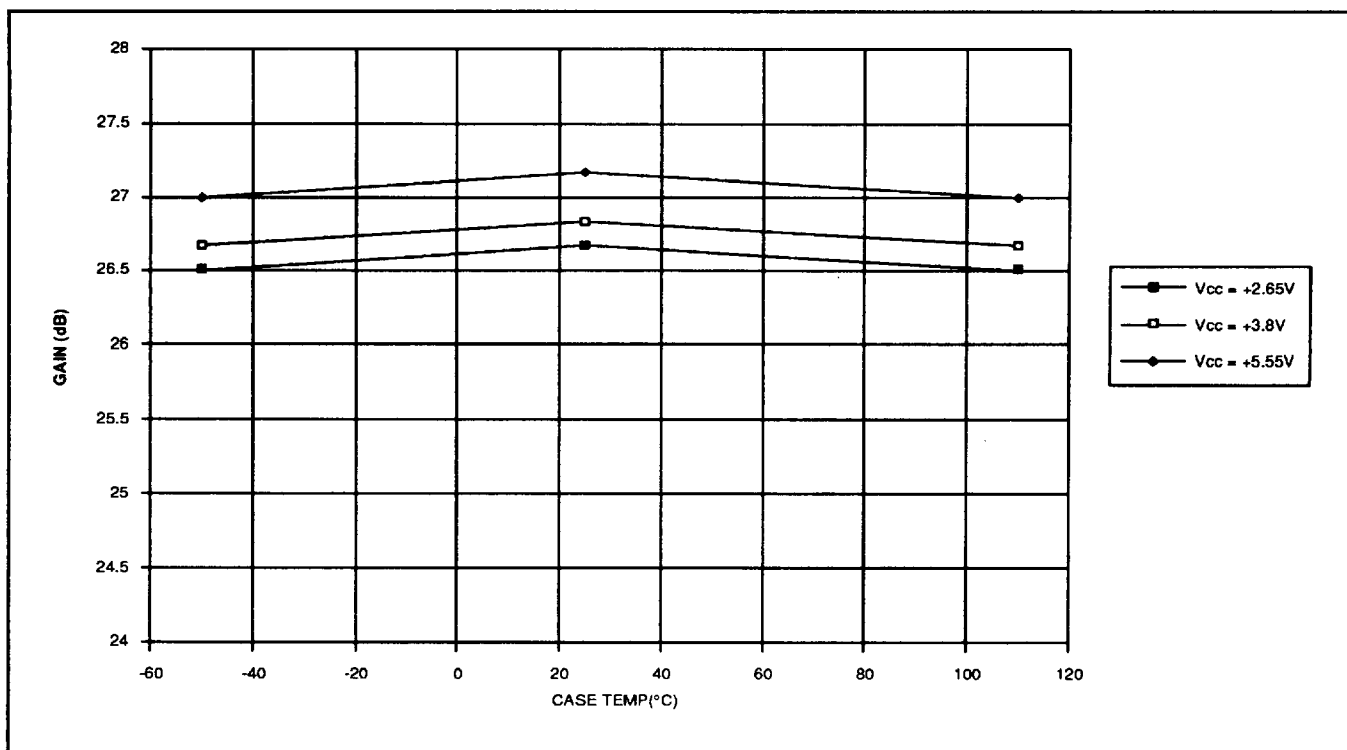


Fig. 21 Stage 2/Mixer 2 Small-signal Conversion Gain - Stage 2 I/P frequency at 175.42MHz

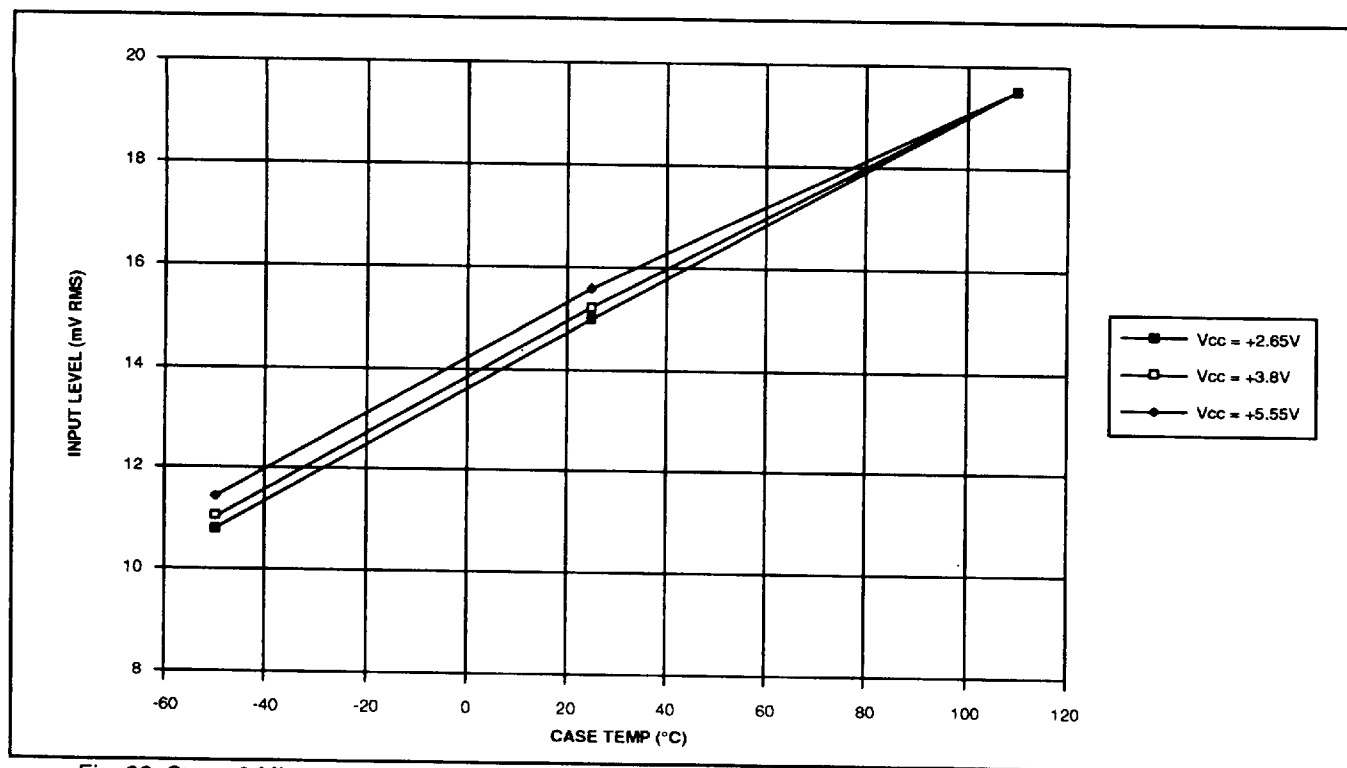


Fig. 22 Stage 2/Mixer 2 Input level for 1dB Conversion Gain-compression - Stage 2 I/P frequency at 175.42MHz

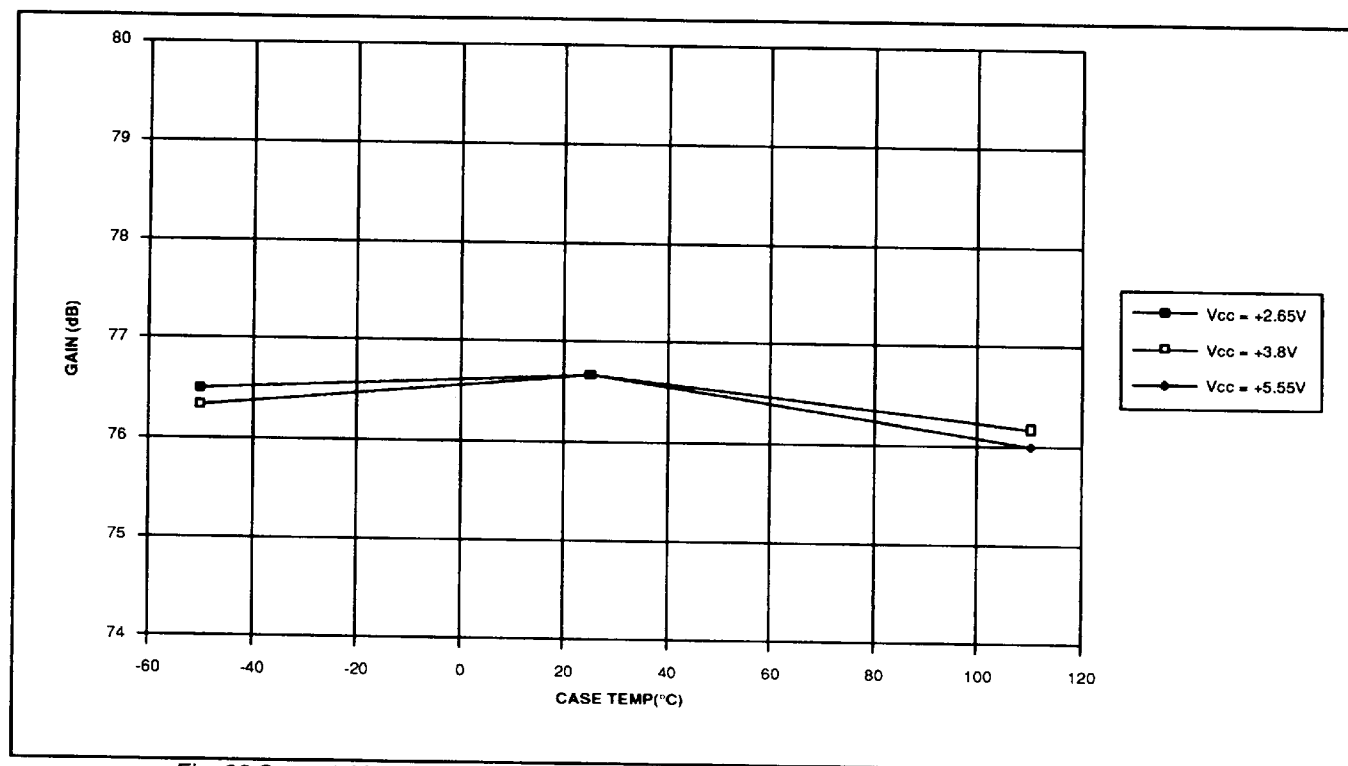


Fig. 23 Stage 3 MAXIMUM Small-signal Conversion Gain - Stage 3 I/P frequency at 35.42MHz

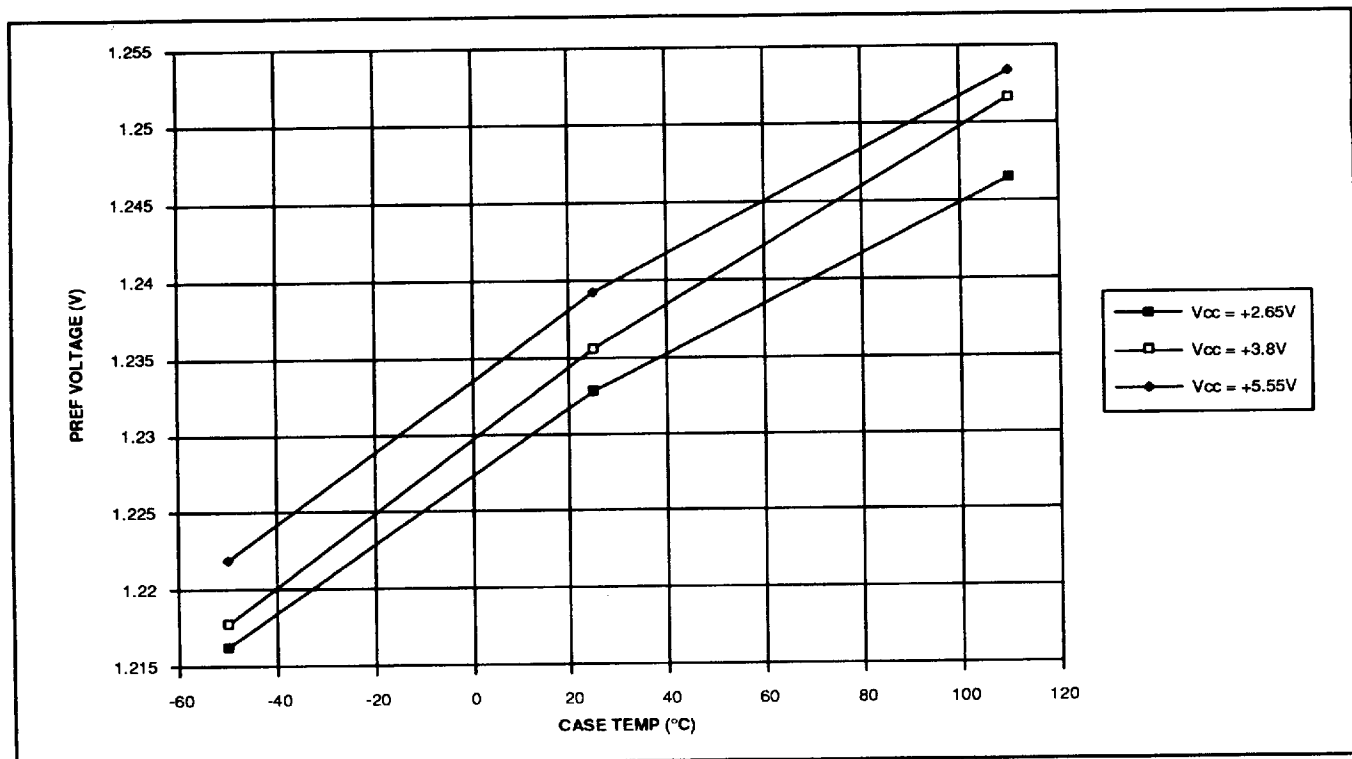


Fig. 24 Power-on Reset Threshold level

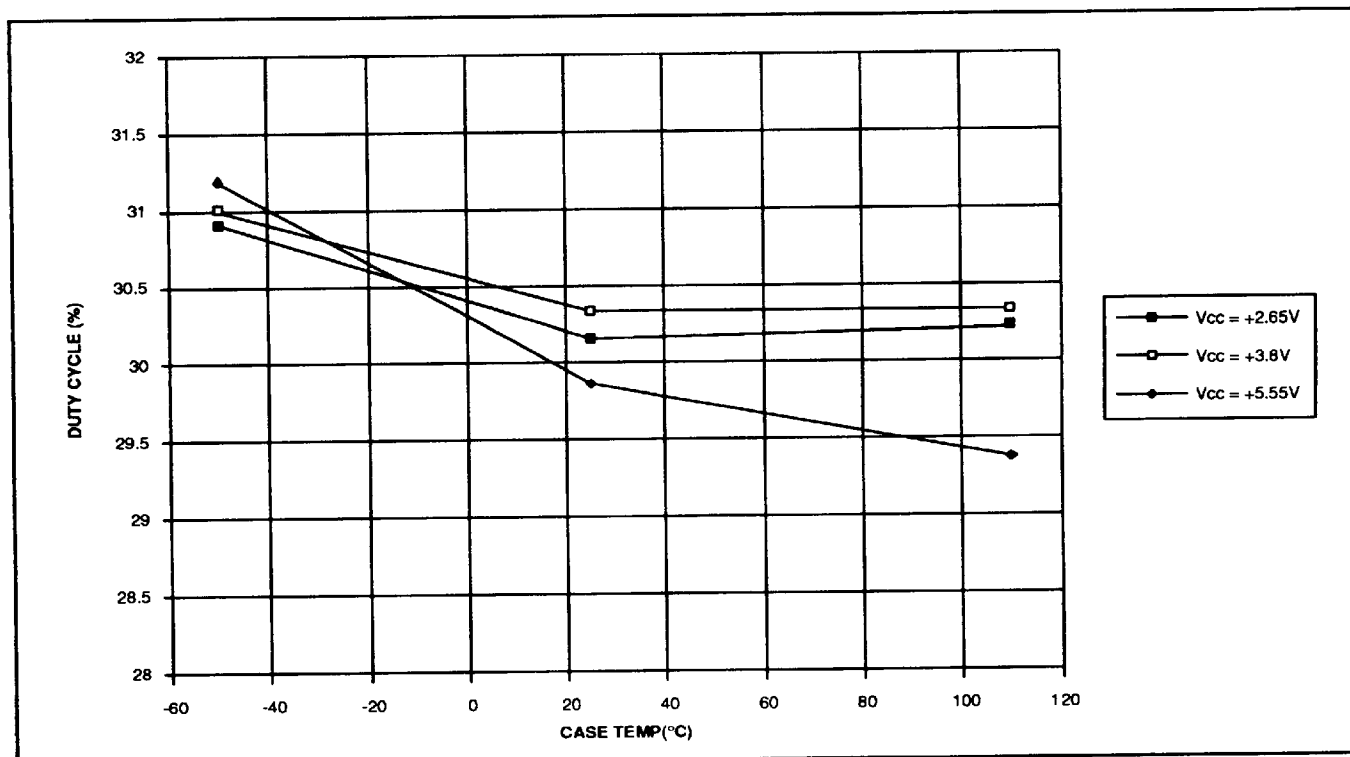


Fig. 25 Duty-cycle of MAG digital output (pin 12), sampled at 5.71MHz in a typical application circuit -
 RF I/P signal = 1575.42MHz CW, -85dBm - equivalent to 26dB
 excess noise from a typical GPS antenna

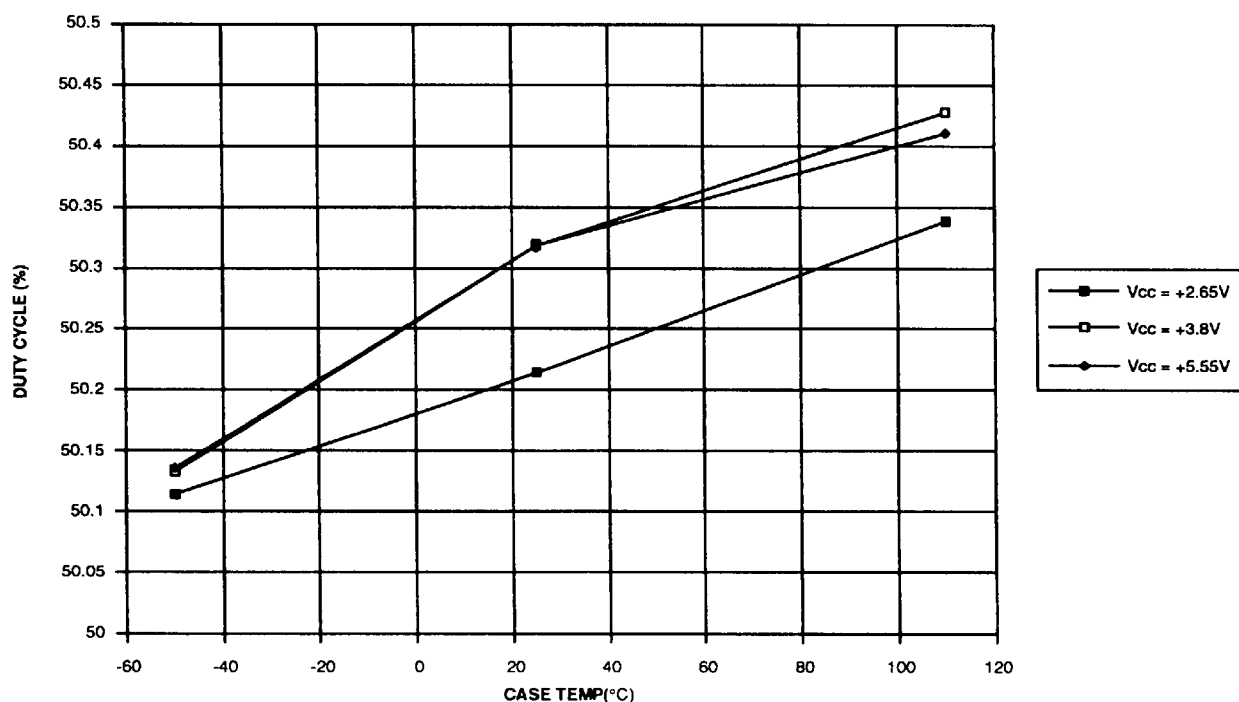


Fig. 26 Duty-cycle of SIGN digital output (pin 13), sampled at 5.71MHz in a typical application circuit
 - RF I/P signal = 1575.42MHz CW, -85dBm - equivalent to
 26dB excess noise from a typical GPS antenna

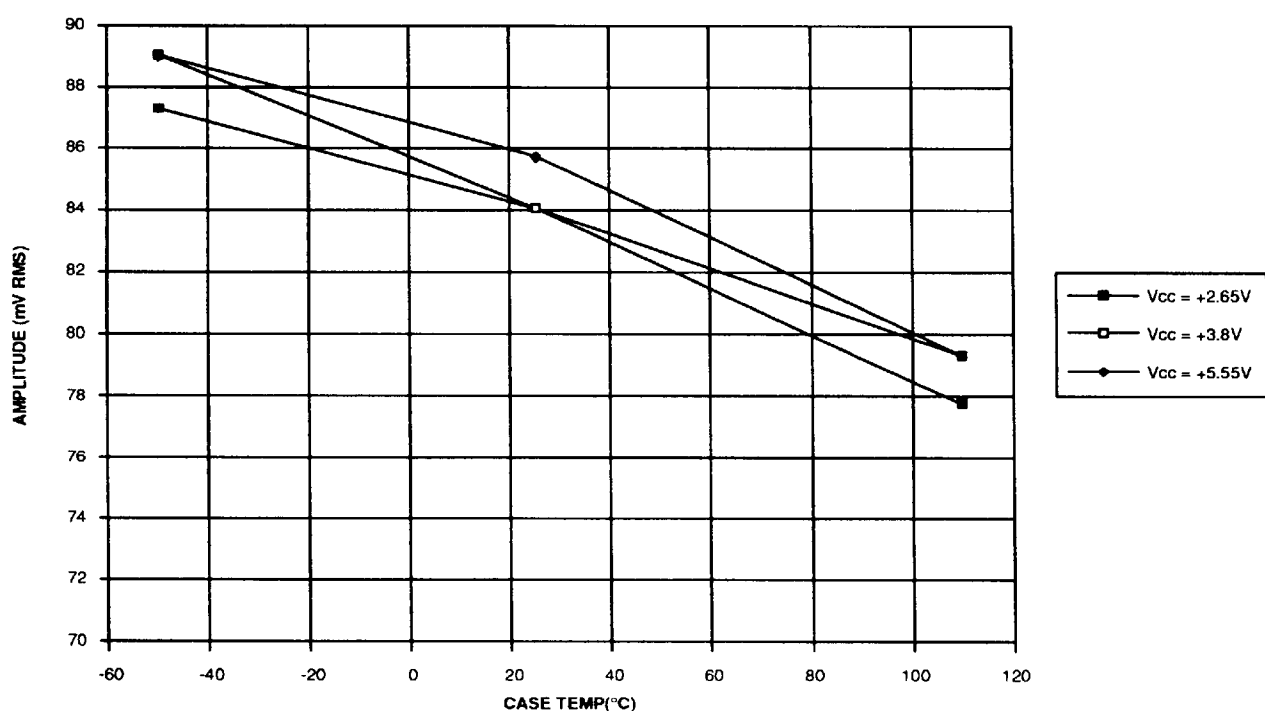
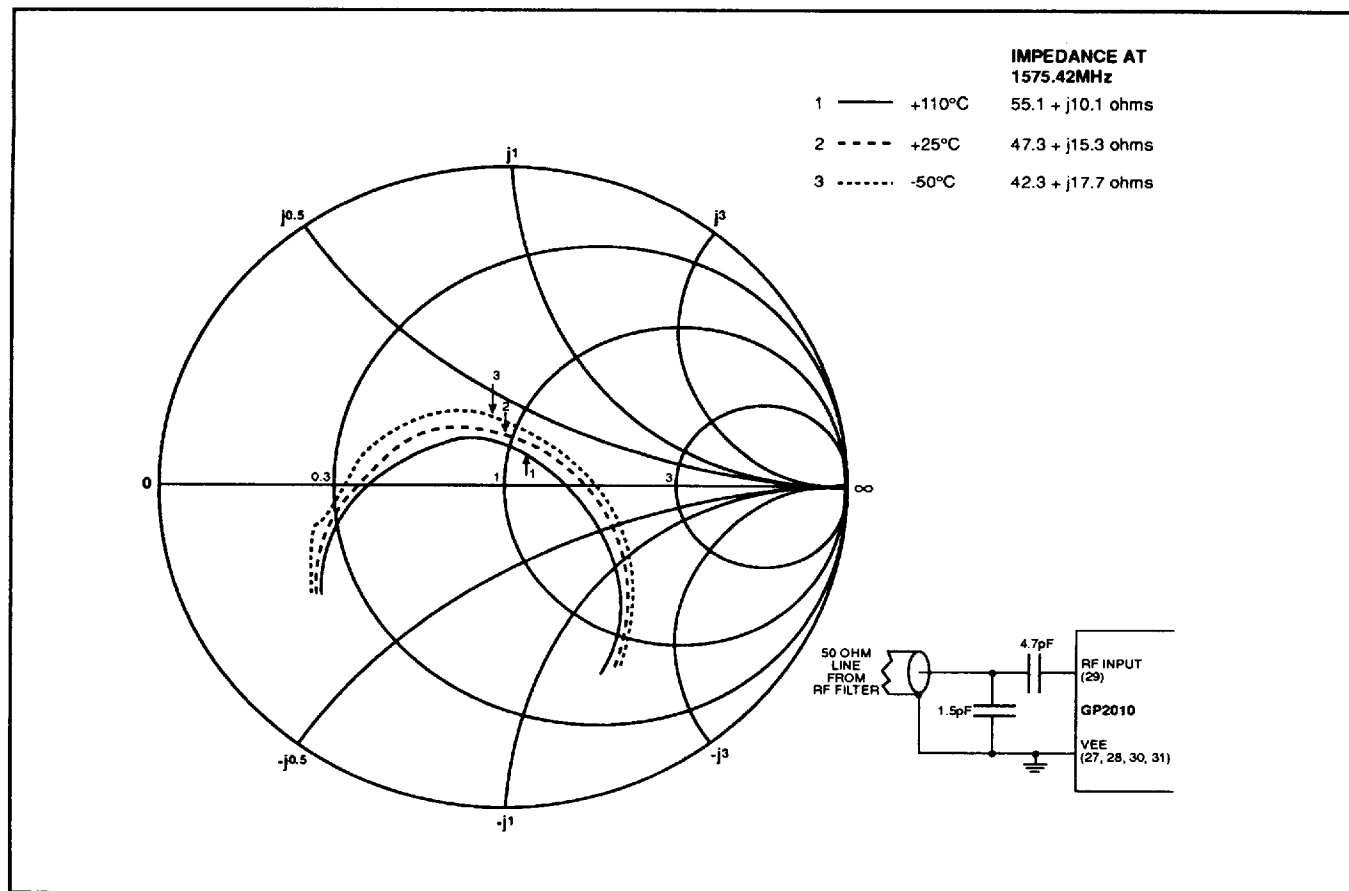
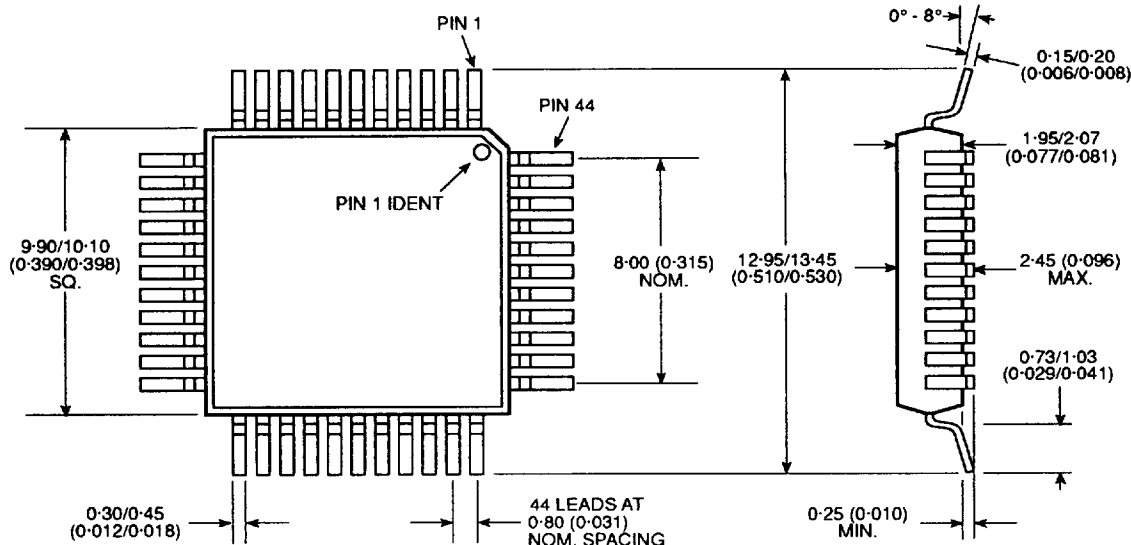


Fig. 27 Amplitude of IFOUT (pin 1) at 4.3MHz (± 1.0 MHz) in a typical application circuit
 - RF I/P signal = 1575.42MHz CW, -85dBm - equivalent to
 26dB excess noise from a typical GPS antenna





NOTES

2. This package outline diagram is for guidance only. Please contact your GEC Plessey Semiconductors Customer Service Centre for further information.

44-LEAD PLASTIC QUAD FLATPACK – GP44



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