National Semiconductor

NM93C46A
1,024-Bit Serial Interface, Standard Voltage CMOS EEPROM (MICROWIRE™ Synchronous Bus)

General Description

The NM93C46A is 1,024 bits of CMOS nonvolatile, electrically erasable memory available as either 64 16-bit registers or 128 8-bit registers. The user organization is determined by the status of the ORG input. The memory device is fabricated using National Semiconductor's floating gate CMOS process for high reliability, high endurance, and low power consumption. The NM93C46A is available in both 8-pin SO and TSSOP packages for space considerations.

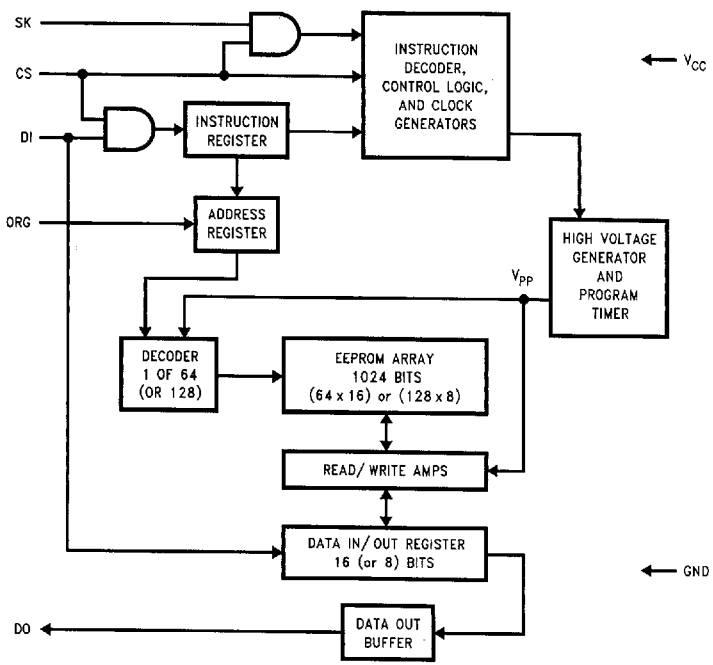
The EEPROM is MICROWIRE compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C46A: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All.

The NM93C46A defaults to the 64 x 16 configuration if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_{CC}.

Features

- 4.5V to 5.5V operation in all modes
- Typical active current of 200 μA; typical standby current of 10 μA
- Self-timed programming cycle
- Device status indication during programming mode
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin TSSOP, 8-pin SO, 8-pin DIP

Block Diagram



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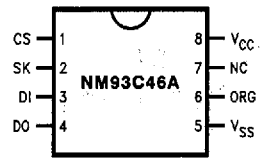
Connection Diagrams

**Dual-In-Line Package (N),
8-Pin SO Package (M8)
and 8-Pin TSSOP Package (MT8)**



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Top View

**See NS Package Number
N08E, M08A and MTC08**

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{SS}	Ground
ORG	Memory Organizational Select
NC	No Connect
V_{CC}	Positive Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C46AN
NM93C46AM8
NM93C46AMT8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C46AEN
NM93C46AEM8
NM93C46AEMT8

Automotive Temp. Range (−40°C to +125°C)

Order Number
NM93C46AVN
NM93C46AVM8
NM93C46AVMT8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	V_{CC} + 1 to −0.3V
Lead Temperature (Soldering, 10 Seconds)	+300°C
EDS Rating	2000V

Operating Range

Ambient Operating Temperature	
NM93C46A	0°C to +70°C
NM93C46AE	−40°C to +85°C
NM93C46AV	−40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics $4.5V \leq V_{CC} \leq 5.5V$

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current	NM93C46A NM93C46AE/V	CS = V_{IH}, SK = 1 MHz SK = 1 MHz		1	mA
I_{CCS}	Standby Current		CS = 0V, ORG = V_{CC} or NC		50	μA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC} (Note 2)	−1	1	μA
I_{ILO}	Input Leakage ORG Pin		ORG tied to V_{CC} ORG tied to V_{SS} (Note 3)	−1 −2.5	1 2.5	μA
I_{OL}	Output Leakage		V_{IN} = 0V to V_{CC}	−1	1	μA
V_{IL}	Input Low Voltage			−0.1	0.8	V
V_{IH}	Input High Voltage			2	V_{CC} + 1	V
V_{OL1}	Output Low Voltage		I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage		I_{OL} = 10 μA		0.2	V
V_{OH2}	Output High Voltage		I_{OL} = −10 μA	V_{CC} − 0.2		V
f_{SK}	SK Clock Frequency	NM93C46A NM93C46AE/V	(Note 4)	0 0	1 1	MHz
t_{SKH}	SK High Time	NM93C46A NM93C46AE/V		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{CS}	Minimum CS Low Time	NM93C46A NM93C46AE/V	(Note 5)	250 250		ns

DC and AC Electrical Characteristics $4.5V \leq V_{CC} \leq 5.5V$ (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C46A NM93C46AE/V		50 50		ns
t_{DH}	DO Hold Time			70		ns
t_{DIS}	DI Setup Time	NM93C46A NM93C46AE/V		100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"	NM93C46A NM93C46AE/V			500 500	ns
t_{PD0}	Output Delay to "0"	NM93C46A NM93C46AE/V			500 500	ns
t_{SV}	CS to Status Valid	NM93C46A NM93C46AE/V			500 500	ns
t_{DF}	CS to DO in TRI-STATE®	NM93C46A NM93C46AE/V	$CS = V_{IL}$		100 100	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance $T_A = +25°C$, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF
Input Pulse Levels	0.4V and 2.4V
Timing Measurements Reference Level	
Input	1V and 2V
Output	0.8v and 2.0V

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20 nA range.

Note 3: The ORG pin may draw >1 μA when in the x8 mode due to an internal pull-up transistor.

Note 4: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/t_{SK} = t_{SKH\ (minimum)} + t_{SKL\ (minimum)}$ for shorter SK cycle time operation.

Note 5: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages.)

Interface Pin Description

Chip Select (CS):

Chip Select performs several functions. It is used to differentiate between various devices on the same MICROWIRE bus. The rising edge resets the internal circuitry of the device, a function necessary prior to initiating a new cycle. Chip Select (as shown on Block Diagram) also gates the Data Input (DI) and Serial Clock (SK) Input, to disable these functions. In the case of these EEPROMs, Chip Select cannot be tied HIGH even if it is the only device on the bus.

Chip Select must be held HIGH continuously during the course of clocking in the start bit, op-code address, and data-in or data-out. Otherwise the internal circuits will reset and the cycle will have to be started again with a new start bit.

Chip Select initiates the internal programming cycle. The falling edge of Chip Select will start the internal asynchronous programming cycle after a programming op-code has been entered (Erase, Write, Erase All, or Write All). In conjunction with Chip Select, Data-Out (DO) will indicate when programming is complete. If the internal programming is incomplete, then Data-Out pin will be LOW. Then when the internal programming is complete, the Data-Out pin will be HIGH (see Timing Diagrams).

Serial Clock (SK):

The Serial Clock input is used to clock all start bits, op-codes, data, addresses, and data bits into or out of the EEPROMs. The clock's rising edge controls the input and output of bits. The falling edge has no effect on the device. The Serial Clock is not necessary for the asynchronous Ready/Busy polling function.

The Serial Clock is in a "Don't Care" at any time Chip Select is LOW. It is also in a "Don't Care" state prior to clocking in a start bit, or during Ready/Busy polling. During either of these last two conditions, Data-In (DI) must be held at a LOW level, otherwise a new start bit will be interpreted.

Data-In (DI):

The Data-In pin receives the start bit, address, and input data synchronously. Each bit is clocked in on the rising edge of SK. DI is gated by Chip Select to provide a high degree of noise immunity. Data-In is routed to both the instruction shift register and the data shift register. After the start bit is clocked into the last bit of the instruction register, the clock is switched to the data register to receive input data. To avoid false reading of a start bit, it is safer to keep the Data-In pin at LOW level when not in use.

Data-Out (DO):

The Data-Out pin sends Read data onto the MICROWIRE bus and it is clocked out on the rising edge of the Serial Clock. During the Read cycle, the DO output begins to drive actively after the last address bit (A0) is clocked in.

Data-Out also carries the device's status during the asynchronous programming cycle. The Data-Out pin drives LOW while the device is still in its internal programming cycle. After the EEPROM has completed this internal programming, Data-Out will drive HIGH. This is accomplished while Chip Select is held HIGH.

Finally, if Chip Select is pulsed LOW to HIGH, Data-Out pin will again produce a pulse HIGH. Thus indicating the completion of the programming cycle.

To clear the Ready/Busy polling, it is necessary to raise Chip Select and clock in another start bit. Once the start bit is clocked in, Data-Out will return to the HIGH impedance state. It is not necessary to continue with a cycle after this start bit has been clocked in, although it is permissible to start a new cycle with this start bit. This clearing of Ready/Busy status may be necessary if a bidirectional data bus is used (Data-In tied to Data-Out) as the Data-Out output will interfere with the new data being presented on the Data-In pin. This connecting of the two Data pins is used for three-wire interface schemes.

Organization (ORG):

The Organization input (ORG) is available only on the NM93C46A device and it is used to control the internal organization of the memory. The two selectable organizations are 16-bit words and 8-bit words. By connecting the ORG pin to V_{CC}, 16-bit words are selected. In contrast, by connecting the ORG pin to GND, 8-bit words are selected. If the ORG pin is left floating, then default setting is the 16-bit word. When in the 8-bit mode, one additional address bit is required in the instruction sequence since the depth of the memory is doubled.

Instruction Set for the NM93C46A

The NM93C46A has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 2 bits carry the op code, the next 6 (or 7) bits carry the address for selection of 1 of 64 16-bit registers or 1 of 128 8-bit registers, depending on memory array organization.

1024 by 16-Bit Organization (NM93C46A when ORG = V_{CC} or NC)

Instruction	SB	OP-Code 2 Bits	Address 6 Bits	Data 16 Bits	Comments
READ	1	10	A5–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXXXX		Disables all programming modes.
ERASE	1	11	A5–A0		Erases selected register.
WRITE	1	01	A5–A0	D15–D0	Writes data pattern D15–D0 into selected registers.
ERAL	1	00	10XXXXXXXX		Erases all registers.
WRAL	1	00	01XXXXXXXX	D15–D0	Writes data pattern D15–D0 into all registers.

2048 by 8-Bit Organization (NM93C46A when ORG = GND)

Instruction	SB	OP-Code 2 Bits	Address 7 Bits	Data 8 Bits	Comments
READ	1	10	A6–A0		Read data stored in selected registers.
EWEN	1	00	11XXXXXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXXXXX		Disables all programming modes.
ERASE	1	11	A6–A0		Erases selected register.
WRITE	1	01	A6–A0	D7–D0	Writes data pattern D7–D0 into selected registers.
ERAL	1	00	10XXXXXXXXX		Erases all registers.
WRAL	1	00	01XXXXXXXXX	D7–D0	Writes data pattern D7–D0 into all registers.

Functional Description

Device	ORG Pin Logic	Memory	
		Configuration	# of Address Bits
NM93C46A	0	128 x 8	7 Bits
	1	64 x 16	6 Bits

Programming:

In all programming modes the READY/BUSY status of the device can be determined by polling the DO pin. After clocking in the last bit of the instruction sequence and with the CS held "high", the DO pin will exit the high impedance state and indicate the READY/BUSY status of the device. DO = logical "0" indicates that programming is still in progress and no other instruction can be executed. DO = logical "1" indicates that the device is READY for another instruction. If CS is forced "low" the DO pin will return to the high impedance state. After the programming cycle has been completed and DO = logical "1", the DO pin can be reset back to the high impedance state by clocking a logical "1" into the DI pin. (This is also performed with the start bit on all op codes, thus clocking an instruction has the same effect.)

Read (READ):

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical 0) precedes the serial data output string. Output data changes are initiated by a low to high transition of SK after the last address bit (A0) is clocked in.

Erase/Write Enable (EWEN):

When V_{CC} is applied to the part, it "powers up" in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Erase/Write Disable (EWDS):

To protect against accidental data overwrites, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EVEN and EWDS instructions.

Functional Description (Continued)

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical "1" state. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last address bit (A0) is clocked in. At this point CS, SK, and DI become don't care states. After starting an ERASE cycle the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased.

Write (WRITE):

The WRITE instruction is followed by 16 bits of data (or 8 bits of data when using the NM93C46A in the x8 organization) to be written into the specified address. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last data bit (D0) is clocked in. At this point, CS, SK and DI become don't care states. No separate ERASE cycle is required before a WRITE instruction.

As in the ERASE instruction, after starting a WRITE cycle, the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been written and that the part is ready for another instruction.

Erase All (ERAL):

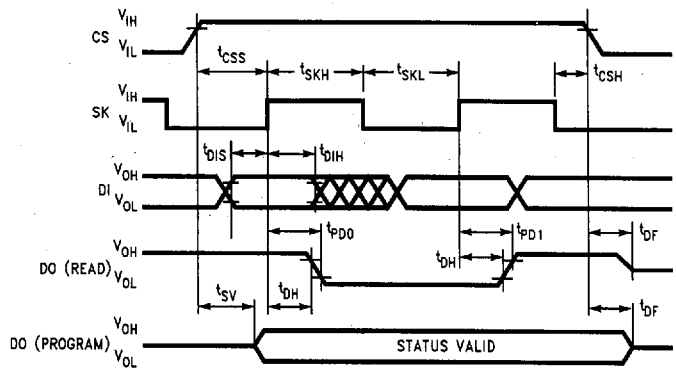
The ERAL instruction will simultaneously program all registers in the memory array to the logical "1" state.

Write All (WRAL):

The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction.

Timing Diagrams for the NM93C46A

Synchronous Data Timing



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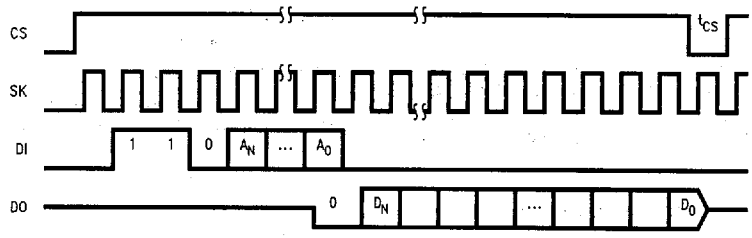
Timing Diagrams (Continued)

Organization of Address and Data Fields for NM93C46A

ORG Pin	Organization	A_N	D_N
V_{CC} or NC	64 x 16	A5	D15
V_{SS}	128 x 8	A6	D7

READ



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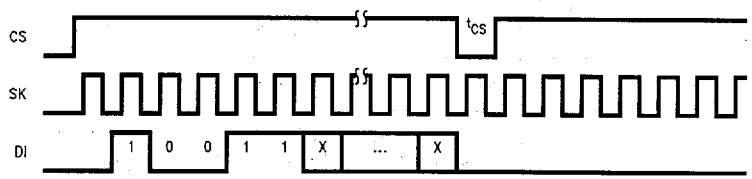
EWEN
DO = TRI-STATE



ORG = V_{CC}, 4 X's
ORG = V_{SS}, 5 X's

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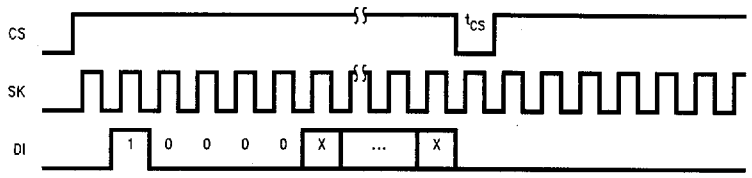
EWDS
DO = TRI-STATE



ORG = V_{CC}, 4 X's
ORG = V_{SS}, 5 X's

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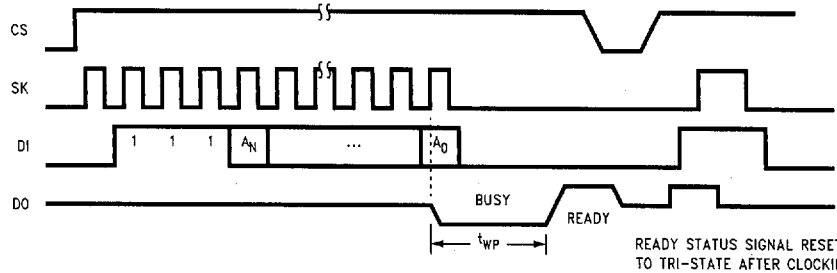
Timing Diagrams (Continued)

ERASE



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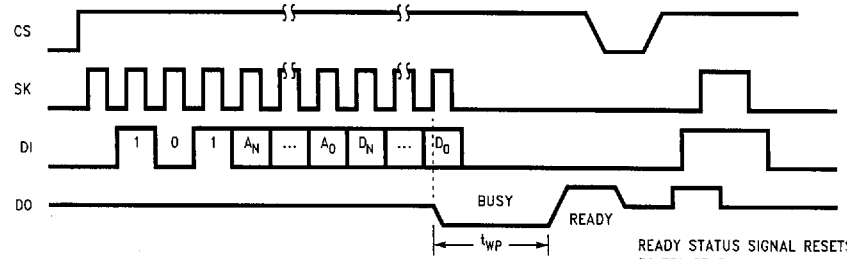
WRITE



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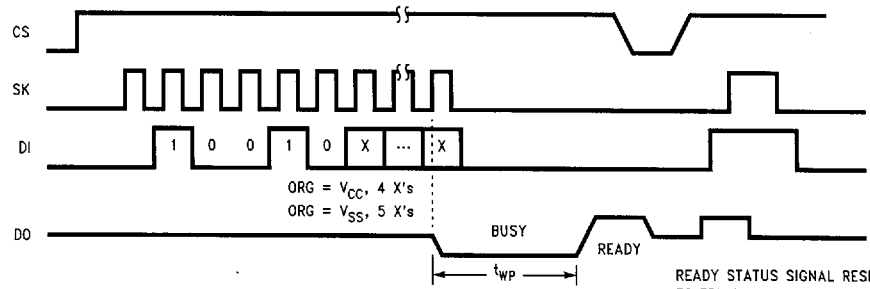
ERAL



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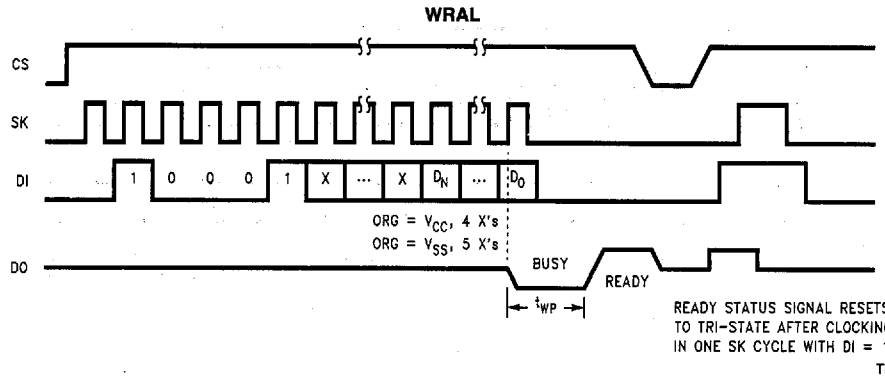
Timing Diagrams (Continued)



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Functional Description (Continued)

Mode 2: Master Reset

Sequence of Operation

1. Input and Output Ready, HF and FULL can be in any state before the reset sequence with Master Reset ($\overline{MR}$) HIGH.
2. Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width t_{MRW} before rising again.
3. Master Reset rises.
4. IR rises (if not HIGH already) to indicate ready to write state recovery time t_{MRIRH} after the falling edge of $\overline{MR}$. Both HF and FULL will go LOW indicating an empty FIFO, occurring recovery times t_{MRE} and t_{MRO} respectively after the falling edge of $\overline{MR}$. OR falls recovery time t_{MRORL} after $\overline{MR}$ falls. Data at outputs goes LOW recovery time t_{MRONL} after $\overline{MR}$ goes LOW.
5. Shift-In can be taken HIGH after a minimum recovery time t_{MRSIH} after $\overline{MR}$ goes HIGH.

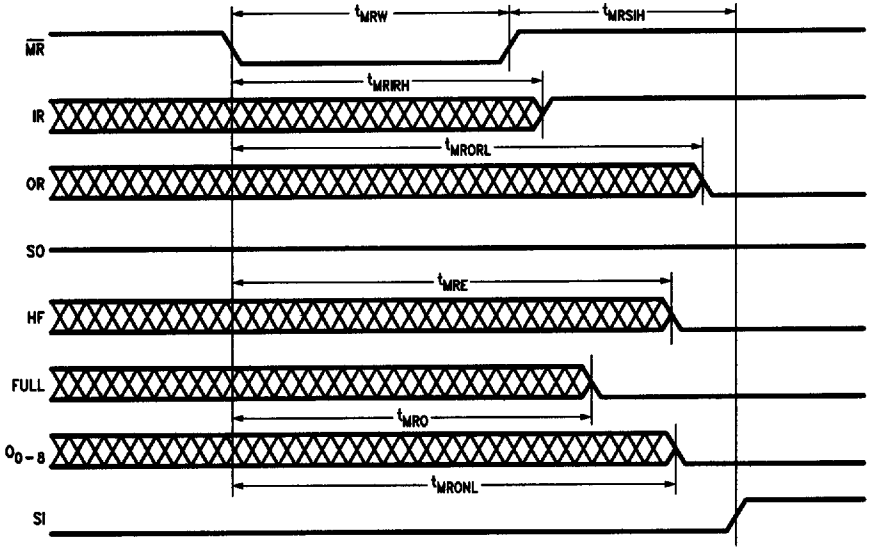

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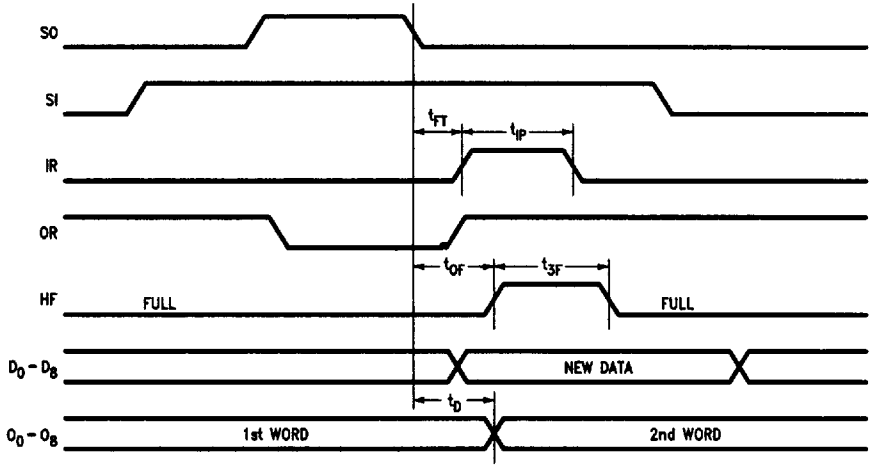
FIGURE 2. Mode of Operation Mode 2

Functional Description (Continued)

Mode 3: With FIFO Full, Shift-In is Held HIGH In Anticipation of an Empty Location

Sequence of Operation

1. The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. Shift-Out is LOW. IR is LOW.
2. Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after propagation delay t_D. New data is written into the FIFO after SO goes LOW.
3. Input Ready goes HIGH one fall-through time, t_{FT}, after the falling edge of SO. Also, HF goes HIGH one t_{OF} after SO falls, indicating that the FIFO is no longer full.
4. IR returns LOW pulse width t_{IP} after rising and shifting new data in. Also, HF returns LOW pulse width t_{3F} after rising, indicating the FIFO is once more full.
5. Shift-In is brought LOW to complete the shift-in process and maintain normal operation



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Note: $\overline{MR}$ and FULL are HIGH; $\overline{OE}$ is LOW.

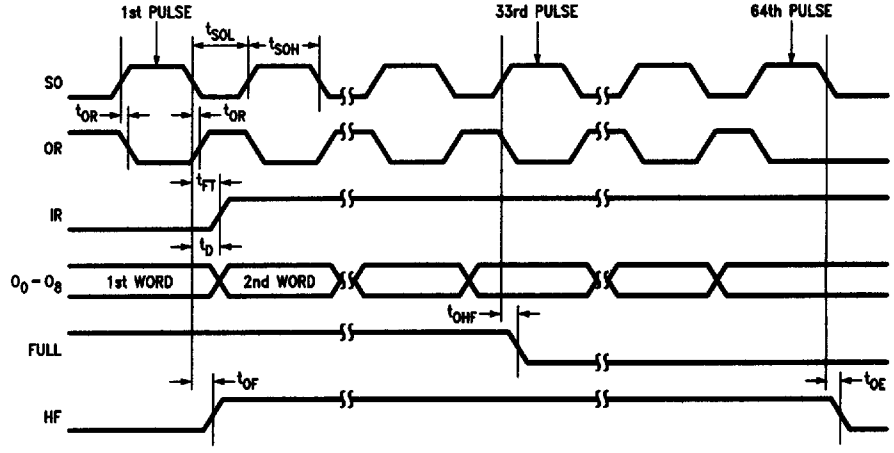
FIGURE 3. Modes of Operation Mode 3

Functional Description (Continued)

Mode 4: Shift-Out Sequence, FIFO Full to Empty

Sequence of Operation

1. FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.
2. SO goes HIGH, resulting in OR going LOW one propagation delay, t_{OR}, after SO rises. OR LOW indicates output stage is busy.
3. SO goes LOW, new data reaches output one propagation delay, t_D, after SO falls; OR goes HIGH one propagation delay, t_{OR}, after SO falls and HF rises one propagation delay, t_{OF}, after SO falls. IR rises one fall-through time, t_{FT}, after SO falls.
4. Repeat process through the 64th SO pulse. FULL flag goes LOW one propagation delay, t_{OHF}, after the rising edge of 33rd SO, indicating that the FIFO is less than half full. On the falling edge of the 64th SO, HF goes LOW one propagation delay, t_{OE}, after SO, indicating the FIFO is empty. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.



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Note: SI and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH; D_0–D_8 are immaterial.

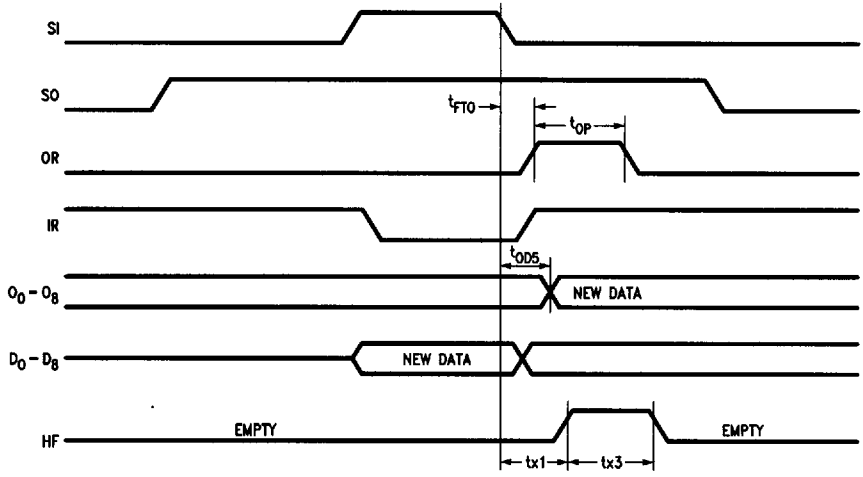
FIGURE 4. Modes of Operation Mode 4

Functional Description (Continued)

Mode 5: With FIFO Empty, Shift-Out is Held HIGH in Anticipation of Data

Sequence of Operation

1. FIFO is initially empty; Shift-Out goes HIGH.
2. Shift-In pulse loads data into the FIFO and IR falls. HF rises propagation delay t_{X1} after the falling edge of SI.
3. OR rises a fall-through time of t_{FTO} after the falling edge of Shift-In, indicating that new data is ready to be output.
4. Data arrives at output one propagation delay, t_{OD5}, after the falling edge of Shift-In.
5. OR goes LOW pulse width t_{OP} after rising and HF goes LOW pulse width t_{X3} after rising, indicating that the FIFO is empty once more.
6. Shift-Out goes LOW, necessary to complete the Shift-Out process.



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Note: FULL is LOW; $\overline{MR}$ is HIGH; $\overline{OE}$ is LOW; $t_{DOF} = t_{FTO} - t_{OD5}$. Data output transition—valid data arrives at output stage t_{DOF} after OR is HIGH.

FIGURE 5. Modes of Operation Mode 5