National Semiconductor

March 1994

NM93C46XLZ
1024-Bit Serial EEPROM for Extra Low Voltage Operation (MICROWIRE™ Bus Interface)

General Description

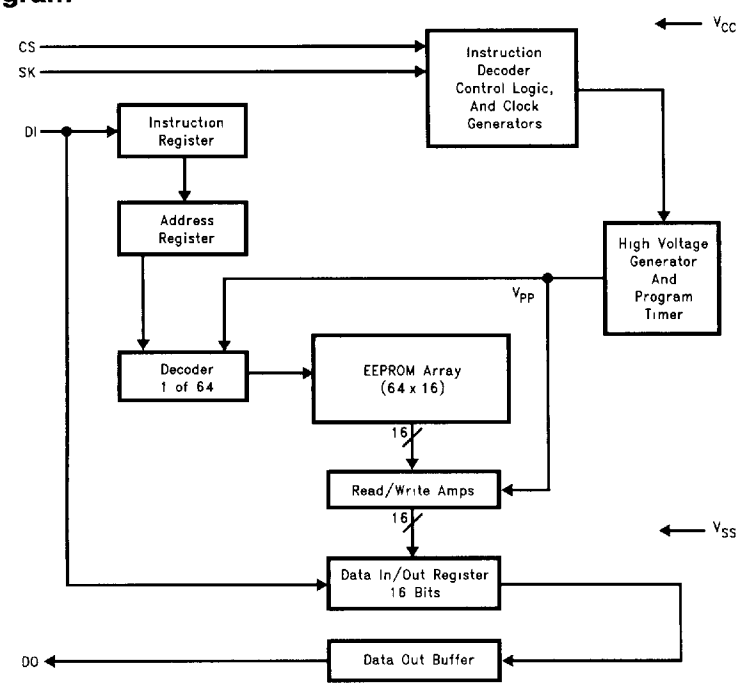
The NM93C46XLZ device is 1024 bits of CMOS non-volatile electrically erasable memory divided into 64 16-bit registers. It is fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. These memory devices are available in an SO package for small space considerations.

The serial interface that operates these EEPROMs is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin during programming.

Features

- Less than 1.0 μA standby current
- 1.8V to 4.0V operation in read/write mode
- Typical active current of 400 μA
- Direct write: No erase before program
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status indication during programming mode
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



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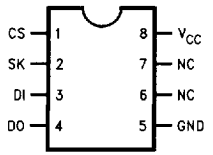
Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



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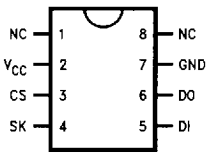
Top View
See NS Package Number N08E and M08A

Alternate SO Pinout (TM8)



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See NS Package Number M08A

Pin Names

Pin	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C46XLZN NM93C46XLZM8/NM93C46XLZTM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C46XL	0°C to +70°C
Power Supply (V_{CC}) Range	
ERAL/WRALL Operation	3.0V to 4.0V
All Other Modes (Note 6)	1.8V to 4.0V

DC and AC Electrical Characteristics: $1.8V < V_{CC} < 4.0V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK = 250 kHz		0.4	1	mA
I_{CCS}	Standby Current	CS = 0V		0.5	1	μA
I_{IL} I_{OL}	Input Leakage Output Leakage	V_{IN} = 0V to V_{CC} (Note 3)			±200	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		−0.1 0.8 V_{CC}		0.15 V_{CC}	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage	I_{OL} = 10 μA I_{OH} = −10 μA	 0.8 V_{CC}		0.2	V
f_{SK}	SK Clock Frequency	(Note 4)	0		250	kHz
t_{SKH}	SK High Time		1			μs
t_{SKL}	SK Low Time		1			μs
t_{SKS}	SK Setup Time		0.4			μs
t_{CS}	Minimum CS Low Time	(Note 2)	1			μs
t_{CSS}	CS Setup Time		0.2			μs
t_{DH}	DO Hold Time		70			ns
t_{DIS}	DI Setup Time		0.4			μs
t_{CSH}	CS Hold Time		0			μs
t_{DIH}	DI Hold Time		0.4			μs
t_{PD1}	Output Delay to "1"				2	μs
t_{PD0}	Output Delay to "0"				2	μs
t_{SV}	CS to Status Valid				1	μs
t_{DF}	CS to DO in TRI-STATE®	CS = V_{IL}			0.4	μs
t_{WP}	Write Cycle Time			100	150	ms

AC Test Conditions

Output Load: 1 TTL Gate and C_L = 100 pF

V_{CC} Range	AC Test Conditions	
1.8V < V_{CC} < 4.0V	Input Pulse Levels	0.3V and 1.8V
	Timing Measurement Level (V_{IL}/V_{IH})	1.0V
	Timing Measurement Level (V_{OL}/V_{OH})	0.8V and 1.5V
	(CMOS Load Condition: I_{OL} = 10 μA, I_{OH} = −10 μA)	

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (This is shown in the opcode diagrams on the following pages).

Note 3: Typical leakage values are in the 20 nA range.

Note 4: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 5: LOW VOLTAGE OPERATION: All functional codes are guaranteed over the specified V_{CC} range (as shown in the **Operating Conditions** and **DC/AC Electrical Characteristics**) EXCEPT the ERAL and WRALL bulk programming modes. These bulk programming commands, which reprogram the entire array, are only guaranteed for the operating range shown on page 3.

Functional Description

The NM93C46XLZ device has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bits in the interface sequence. The next 8 bits carry the op code and the 6-bit address for register selection.

All Data-In signals are clocked into the device on the low-to-high SK transition.

Read (READ): The READ instruction outputs serial data on the DO pin. After the READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (WEN): When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (WEN) instruction. Once an Erase/Write Enable instruction is executed programming remains enabled until an Erase/Write Disable (WDS) instruction is executed or until V_{CC} is completely removed from the part.

Erase (ERASE): The ERASE instruction will program all bits in the specified register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after an interval of t_{CS}. DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE): The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after an interval of t_{CS}. DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL): The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after an interval of t_{CS}.

Write All (WRALL): The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after an interval of t_{CS}.

Erase/Write Disable (WDS): To protect against accidental data disturb, the (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

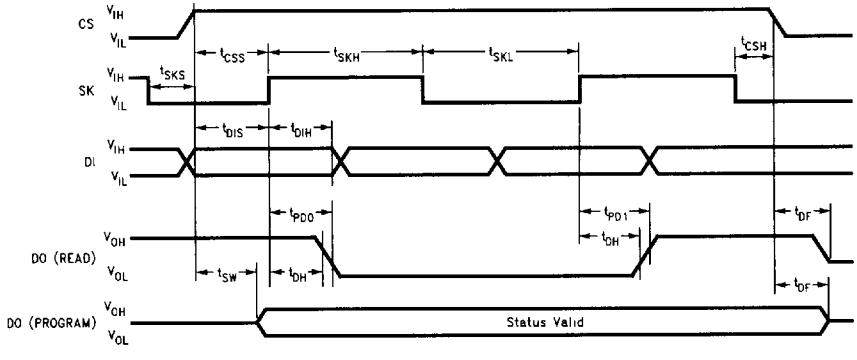
Note: The NM93C46XLZ devices do not require an "ERASE" or "ERASE ALL" prior to the "WRITE" or "WRITE ALL" instructions.

Instruction Set for the NM93C46XLZ

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Read data stored in memory, at specified address
WEN	1	00	11XXXX		Enables all programming modes
WDS	1	00	00XXXX		Disables all programming modes
ERASE	1	11	A5–A0		Erase selected register
WRITE	1	01	A5–A0	D15–D0	Writes selected register
ERAL	1	00	10XXXX		Erases all registers
WRALL	1	00	01XXXX	D15–D0	Writes all registers

Timing Diagrams

Synchronous Data Timing



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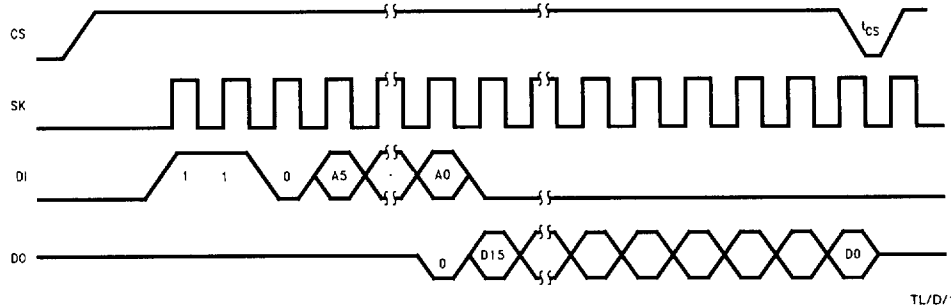
READ



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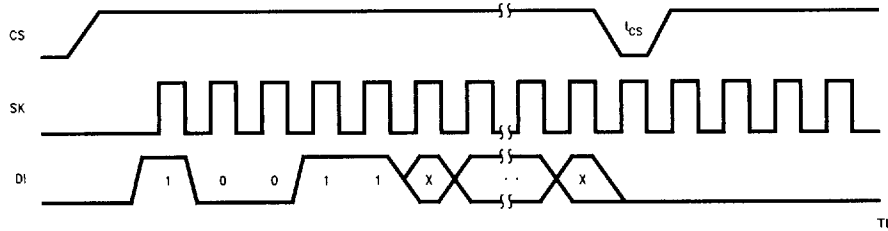
WEN



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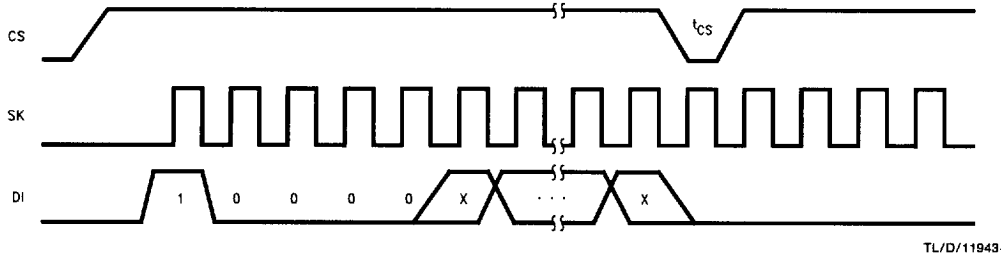
Timing Diagrams (Continued)

WDS



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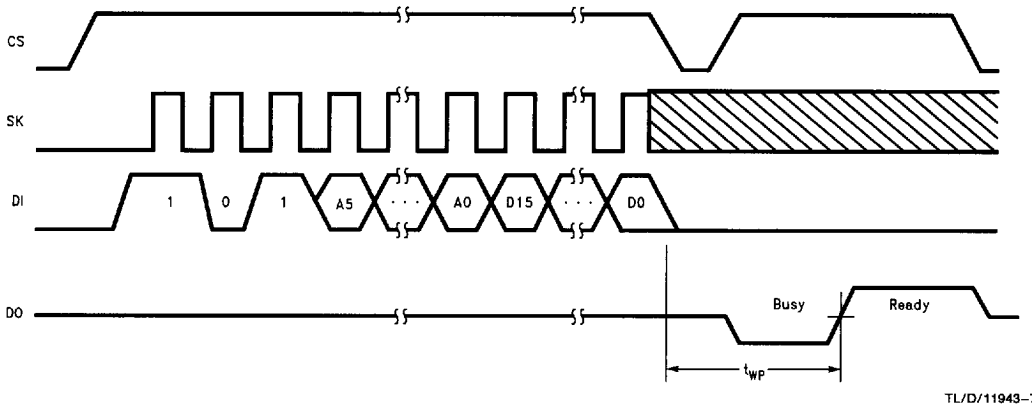
WRITE



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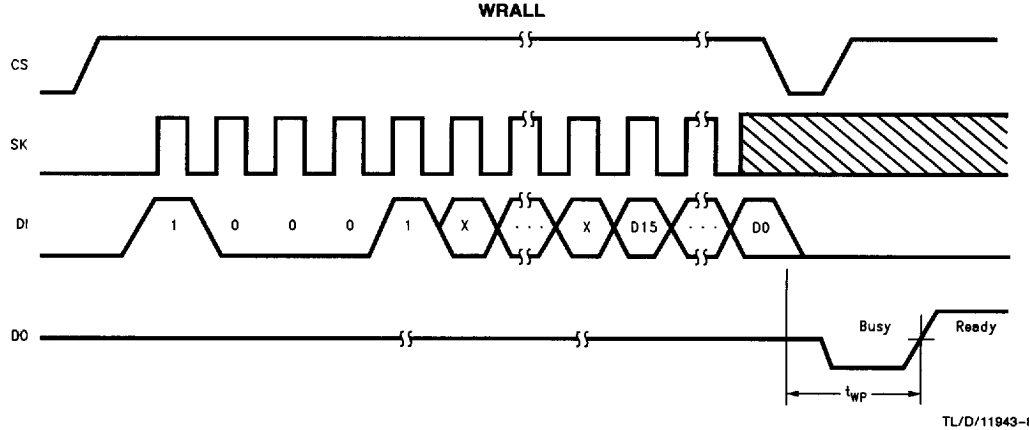
WRALL



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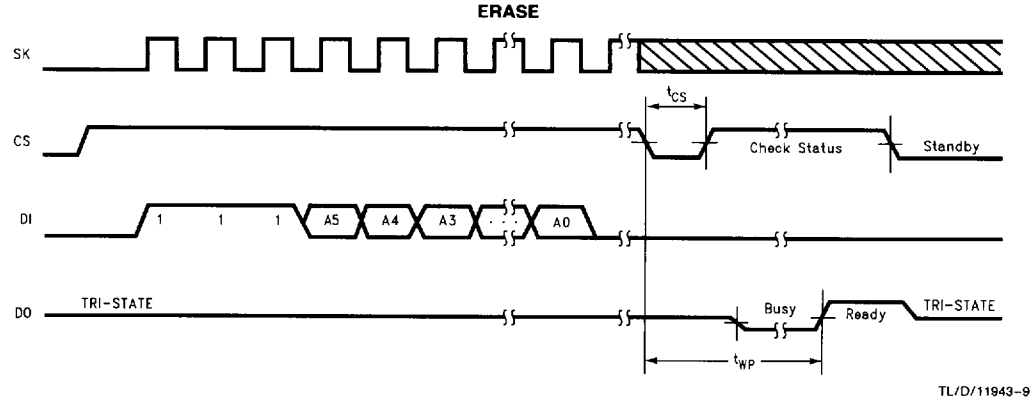
Timing Diagrams (Continued)



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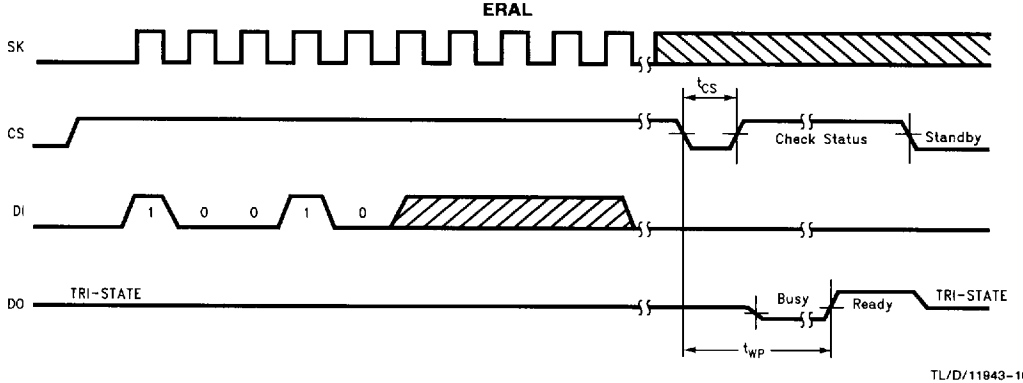

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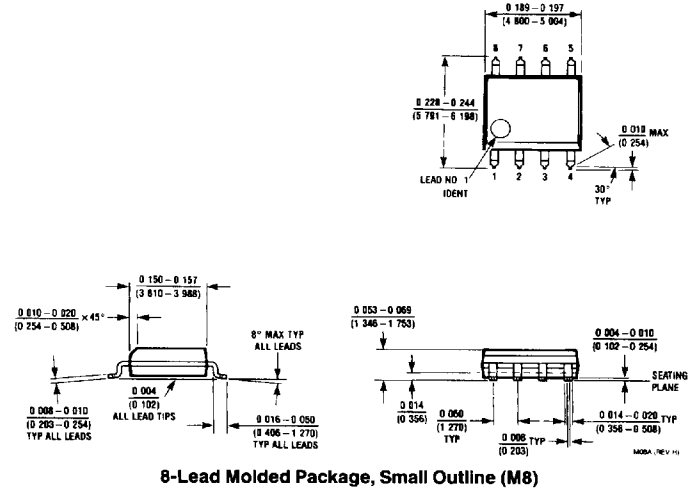
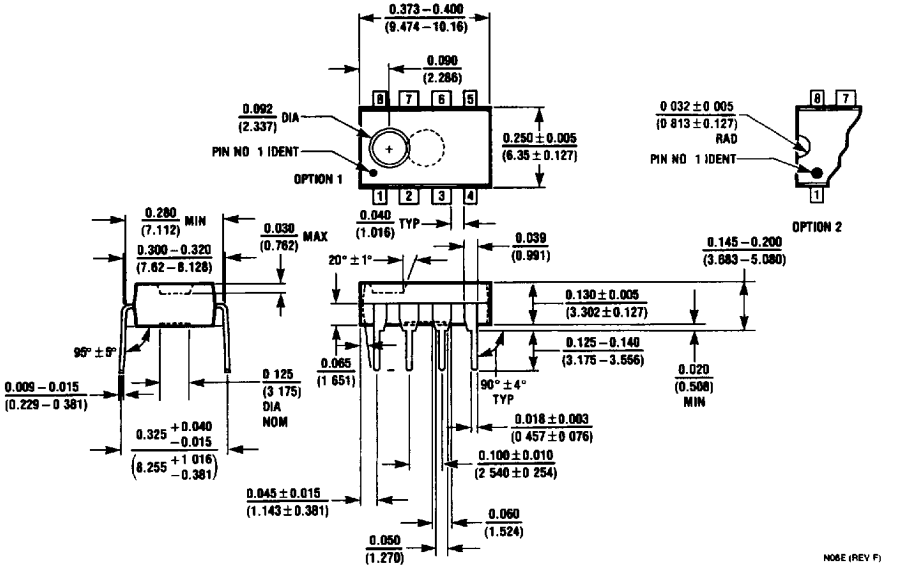
Physical Dimensions inches (millimeters)



8-Lead Molded Package, Small Outline (M8)
Order Number NM93C46XLZM8
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)



8-Lead Molded Dual-In-Line Package (N)
Order Number NM93C46XLZN
NS Package Number N08E

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