GS1881, GS4881, GS4981
Monolithic Video Sync Separators

DATA SHEET

FEATURES

- **noise tolerant odd/even flag, back porch and horizontal sync pulse**
- **fast recovery from impulse noise**
- **excellent temperature stability**
- **0.5 V to 4 Vpp input signal amplitude with 5 V supply**
- **well-controlled clamp discharge current and slicing level**
- **programmable horizontal scan rate (up to 130 kHz)**
- **composite, vertical, back porch, odd/even (GS1881, GS4881), horizontal (GS4981) outputs**
- **predictable vertical output pulse width with default trigger for non-standard video signals**
- **5 V to 12 V supply voltage range**
- **pin compatible with LM1881 sync separator**

SELECTION CHART

APPLICATION	CHOOSE DEVICE:
Direct LM1881 Replacement with Improved Performance	GS1881
New Applications Substitution for LM1881	GS4881
New Applications Requiring Horizontal Sync Output	GS4981

DESCRIPTION

The GS1881, GS4881 and GS4981 are general purpose sync separators for use in a wide variety of video applications. The devices extract the timing information from composite video signals with scan rates from 15 to 130 kHz.

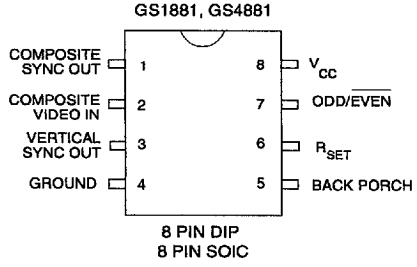
The GS1881 is a drop-in replacement for the industry standard LM1881 with much improved performance. The device generates composite sync, vertical sync, back porch and odd/even field signals. The GS4881 is identical to the GS1881 but features a noise immune back porch pulse which maintains a constant H rate during the vertical interval. The GS4981 is identical to the GS4881, except that it provides horizontal sync in place of the odd/even output.

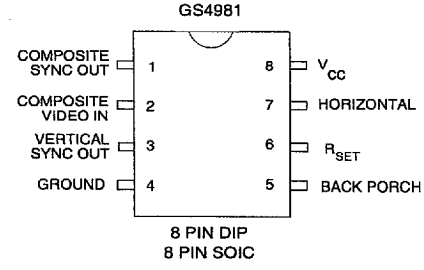
All three devices feature a self-adjusting windowing circuit for noise immunity, which synchronizes to H rate. This windowing circuit determines the odd or even field in the GS1881 and GS4881, gates the back porch pulse in the GS4881 and GS4981, and generates the horizontal sync output in the GS4981.

The devices feature an improved input stage which ensures that the input signal is sliced at a predictable point due to well-controlled input clamp discharge current and sync slicing level. A missing pulse detector enables the devices to recover quickly from impulse noise disturbances by temporarily increasing the clamp discharge current by roughly ten times. The input stage will operate with signals from 0.5 to 4 volts peak to peak with a 5 volt supply.

The GS1881, GS4881 and GS4981 also feature a predictable vertical output pulse width with a default trigger for non-standard video signals. All three are available in commercial and industrial temperature ranges and are packaged in both DIP and SOIC.

PIN CONNECTIONS





Patent No. 5,432,559
Revision Date: October 1995

GS1881 ELECTRICAL CHARACTERISTICS (V_{CC}= 5 V, R_{SET} = 680 kΩ, T_A = 25° C, unless otherwise specified)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage			4.5	5	13.2	V
Supply Current	Outputs at Logic 1	V_{CC} = 5 V	-	4.6	6.5	mA
		V_{CC} = 12 V	-	5.0	7.0	mA
Video Input (Pin 2)						
(a) Signal Level	V_{CC} = 5 V		0.5	-	4	Vp-p
(b) Clamp Current	Charge		500	650	850	µA
	Discharge - normal		9	11	13	µA
	- Nosync flag raised		65	95	115	µA
(c) Delay to raising of Nosync flag	Video input held high		64	95	130	µs
(d) Sync Tip Clamp Voltage			-	1.55	-	V
Sync Slice Level	Relative to sync tip clamp voltage		70	77	84	mV
R_{SET} Pin Reference Voltage (Pin 6)	See Note 1		1.14	1.24	1.34	V
Composite Sync Out (Pin 1)	See Note 2		40	60	80	ns
Delay from Video	C_L = 15p					
Back Porch Pulse Out (Pin 5)	C_L = 15p					
(a) Delay from Rising						
Edge of Sync			400	500	650	ns
(b) Pulse Width			2.0	2.5	3.2	µs
Vertical Sync Out (Pin 3)						
(a) Pulse Width	Serrations during vertical interval		197.7	197.7	197.7	µs
(b) Default Starting Time	No serrations during the vertical interval		48	65	82	µs
Horizontal Scan Rate	Modified R_{SET}		15	-	130	kHz
Logic Outputs						
(a) V_{OH}	I_{OH} = 40 µA	V_{CC} = 5 V	4.2	4.6	-	V
		V_{CC} = 12 V	11.2	11.6	-	V
	I_{OH} = 1.6 mA	V_{CC} = 5 V	2.4	3.4	-	V
		V_{CC} = 12 V	9.4	10.4	-	V
(b) V_{OL}	I_{OL} = -1.6 mA		-	0.3	0.6	V

Note 1: When placing the R_{SET} resistor and the 0.1µF decoupling capacitor careful attention should be made to ensure that they are as close as possible to pin 6. Care should also be taken to avoid parasitic capacitive coupling from any output pin (pins 1, 3, 5 and 7) to pin 6.

Note 2: Measured from slicing point of input falling edge to 50% point of composite sync falling edge.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GS1881 - CDA	8 PDIP	0° to 70° C
GS1881 - CKA	8 SOIC	0° to 70° C
GS1881 - CTA	8 TAPE	0° to 70° C
GS1881 - IDA	8 PDIP	-25° to 85° C
GS1881 - IKA	8 SOIC	-25° to 85° C
GS1881 - ITA	8 TAPE	-25° to 85° C

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

GS4881 ELECTRICAL CHARACTERISTICS (V_{CC}= 5 V, R_{SET} = 680 kΩ, T_A = 25° C, unless otherwise specified)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage			4.5	5	13.2	V
Supply Current	Outputs at Logic 1	V_{CC} = 5 V	-	4.6	6.5	mA
		V_{CC} = 12 V	-	5.0	7.0	mA
Video Input (Pin 2)						
(a) Signal Level	V_{CC} = 5 V		0.5	-	4	Vp-p
(b) Clamp Current	Charge		500	650	850	µA
	Discharge - normal		9	11	13	µA
	- Nosync flag raised		65	95	115	µA
(c) Delay to raising of Nosync flag	Video input held high		64	95	130	µs
(d) Sync Tip Clamp Voltage			-	1.55	-	V
Sync Slice Level	Relative to sync tip clamp voltage		70	77	84	mV
R_{SET} Pin Reference Voltage (Pin 6)	See Note 1		1.14	1.24	1.34	V
Composite Sync Out (Pin 1) Delay from Video	See Note 2 C_L = 15p		40	60	80	ns
Back Porch Pulse Out (Pin 5)	C_L = 15p					
(a) Delay from Rising Edge of Sync			400	500	650	ns
(b) Pulse Width			2.0	2.5	3.2	µs
(c) Occurence Rate			H	H	H	
Vertical Sync Out (Pin 3)						
(a) Pulse Width	Serrations during vertical interval		197.7	197.7	197.7	µs
(b) Default Starting Time	No serrations during the vertical interval		48	65	82	µs
Horizontal Scan Rate	Modified R_{SET}		15	-	130	kHz
Logic Outputs						
(a) V_{OH}	I_{OH} = 40 µA	V_{CC} = 5 V	4.2	4.6	-	V
		V_{CC} = 12 V	11.2	11.6	-	V
	I_{OH} = 1.6 mA	V_{CC} = 5 V	2.4	3.4	-	V
		V_{CC} = 12 V	9.4	10.4	-	V
(b) V_{OL}	I_{OL} = -1.6 mA		-	0.3	0.6	V

Note 1: When placing the R_{SET} resistor and the 0.1µF decoupling capacitor careful attention should be made to ensure that they are as close as possible to pin 6. Care should also be taken to avoid parasitic capacitive coupling from any output pin (pins 1, 3, 5 and 7) to pin 6.

Note 2: Measured from slicing point of input falling edge to 50% point of composite sync falling edge.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GS4881 - CDA	8 PDIP	0° to 70° C
GS4881 - CKA	8 SOIC	0° to 70° C
GS4881 - CTA	8 TAPE	0° to 70° C
GS4881 - IDA	8 PDIP	-25° to 85° C
GS4881 - IKA	8 SOIC	-25° to 85° C
GS4881 - ITA	8 TAPE	-25° to 85° C

GS4981 ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, R_{SET} = 680 kΩ, T_A = 25° C, unless otherwise specified)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage			4.5	5	13.2	V
Supply Current	Outputs at Logic 1	V_{CC} = 5 V	-	4.6	6.5	mA
		V_{CC} = 12 V	-	5.0	7.0	mA
Video Input (Pin 2)						
(a) Signal Level	V_{CC} = 5 V		0.5	-	4	Vp-p
(b) Clamp Current	Charge		500	650	850	µA
	Discharge - normal		9	11	13	µA
	- Nosync flag raised		65	95	115	µA
(c) Delay to raising of Nosync flag	Video input held high		64	95	130	µs
(d) Sync Tip Clamp Voltage			-	1.55	-	V
Sync Slice Level	Relative to sync tip clamp voltage		70	77	84	mV
R_{SET} Pin Reference Voltage (Pin 6)	See Note 1		1.14	1.24	1.34	V
Composite Sync Out (Pin 1)	See Note 2		40	60	80	ns
Delay from Video	C_L = 15p					
Back Porch Pulse Out (Pin 5)	C_L = 15p					
(a) Delay from Rising						
Edge of Sync			400	500	650	ns
(b) Pulse Width			2.0	2.5	3.2	µs
(c) Occurence Rate			H	H	H	
Vertical Sync Out (Pin 3)						
(a) Pulse Width	Serrations during vertical interval		197.7	197.7	197.7	µs
(b) Default Starting Time	No serrations during the vertical interval		48	65	82	µs
Horizontal Sync Out (Pin 7)	C_L = 15p					
(a) Delay from Video			90	190	290	ns
(b) Pulse Width			5.0	7.0	9.0	µs
Horizontal Scan Rate	Modified R_{SET}		15	-	130	kHz
Logic Outputs						
(a) V_{OH}	I_{OH} = 40 µA	V_{CC} = 5 V	4.2	4.6	-	V
		V_{CC} = 12 V	11.2	11.6	-	V
	I_{OH} = 1.6 mA	V_{CC} = 5 V	2.4	3.4	-	V
	Note 3	V_{CC} = 12 V	9.4	10.4	-	V
(b) V_{OL}	I_{OL} = -1.6 mA		-	0.3	0.6	V

Note 1: When placing the R_{SET} resistor and the 0.1µF decoupling capacitor careful attention should be made to ensure that they are as close as possible to pin 6. Care should also be taken to avoid parasitic capacitive coupling from any output pin (pins 1, 3, 5 and 7) to pin 6.

Note 2: Measured from slicing point of input falling edge to 50% point of composite sync falling edge.

Note 3: Applies only to composite sync, vertical sync, and back porch outputs. Horizontal sync has a passive 10 kΩ pull-up to V_{CC}.

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GS4981 - CDA	8 PDIP	0° to 70° C
GS4981 - CKA	8 SOIC	0° to 70° C
GS4981 - CTA	8 TAPE	0° to 70° C
GS4981 - IDA	8 PDIP	-25° to 85° C
GS4981 - IKA	8 SOIC	-25° to 85° C
GS4981 - ITA	8 TAPE	-25° to 85° C

TYPICAL PERFORMANCE CHARACTERISTICS (V_S = 5V, T_A = 25° C unless otherwise shown)

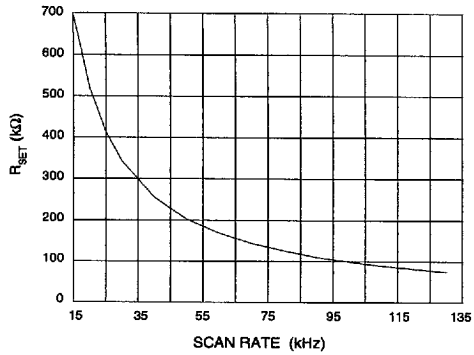


Fig. 1 R_{SET} vs Scan Rate

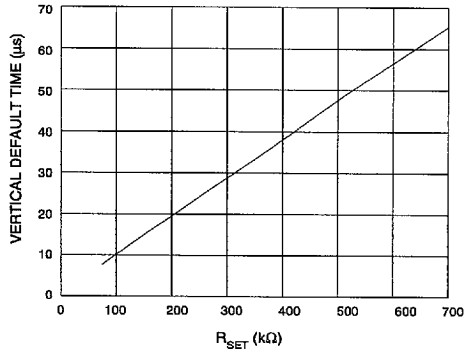


Fig. 2 Vertical Sync Default Starting Time vs R_{SET}

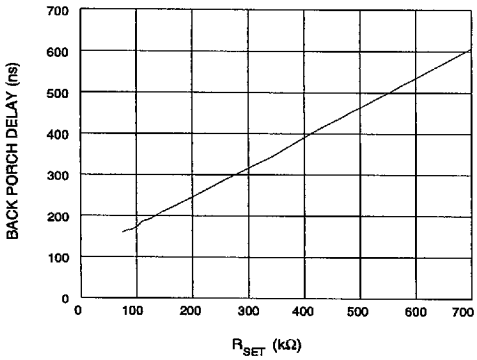


Fig. 3 Back Porch Delay vs R_{SET}

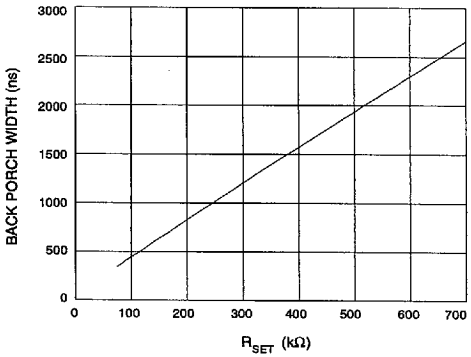


Fig. 4 Back Porch Width vs R_{SET}

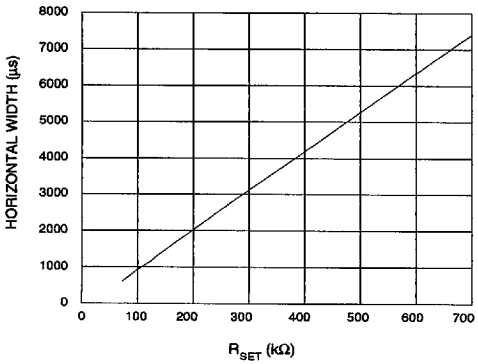


Fig. 5 Horizontal Width vs R_{SET}

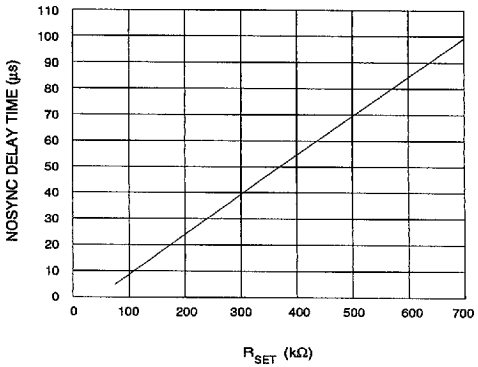


Fig. 6 Nosync Delay Time vs R_{SET}

GS1881/4881/4981

TEMPERATURE CHARACTERISTICS (V_S = 5V, R_{SET} = 680 kΩ unless otherwise shown)

Commercial Temperature Range (0 - 70 °C)

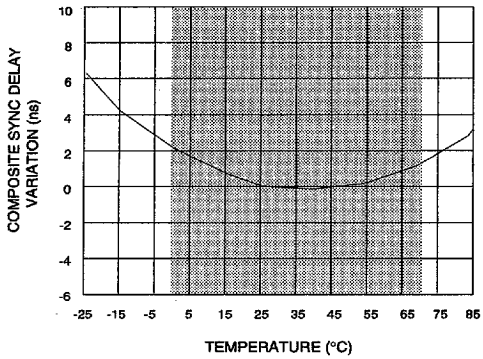


Fig. 7 Composite Sync Delay Variation vs Temperature

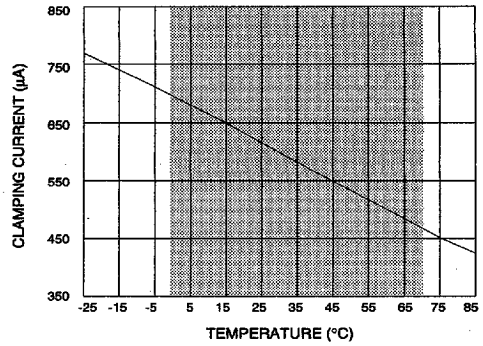


Fig. 8 Clamping Current vs Temperature

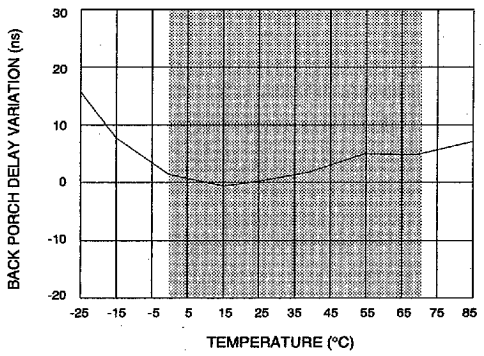


Fig. 9 Back Porch Delay Variation vs Temperature

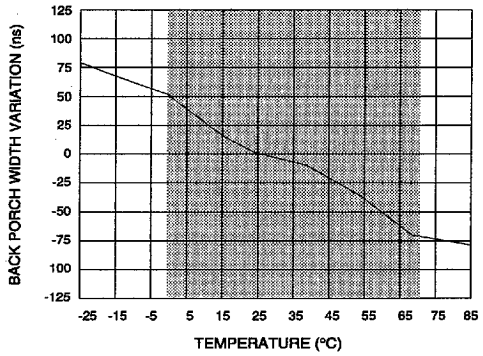


Fig. 10 Back Porch Width Variation vs Temperature

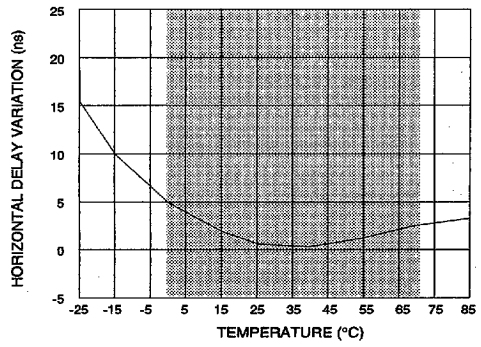


Fig. 11 Horizontal Delay Variation vs Temperature

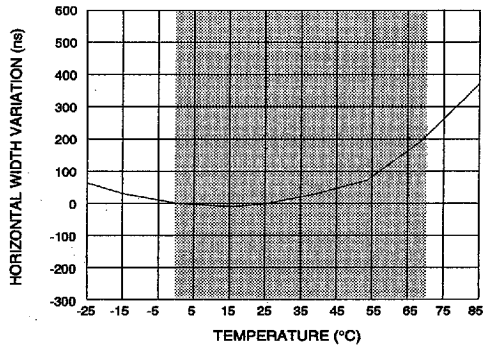


Fig. 12 Horizontal Width Variation vs Temperature

CIRCUIT DESPCRIPTION

The block diagrams for the GS1881, GS4881 and GS4981, are shown in Figures 17 through 19, with timing diagrams for the devices shown in Figure 20.

When stimulated by a composite input signal, the GS1881 and GS4881 sync separators output composite sync, vertical sync, back porch, and odd/even field information. The GS4981 substitutes the odd/even output of the GS4881 with a horizontal output. An external resistor on pin 6 is used to define internal currents allowing the devices to accommodate horizontal scan rates from 15 kHz to 130 kHz.

COMPOSITE VIDEO INPUT (pin 2) and COMPOSITE SYNC OUTPUT (pin 1)

Composite video is AC coupled via an external coupling capacitor to pin 2. The device clamps the sync tip of the input video to 1.5 V (V_{clamp}) and then slices at 77 mV above the clamp voltage (V_{slice}). The resultant signal, provided at pin 1, is a reproduction of the input signal with the active video portion removed. As V_{clamp} and V_{slice} are supply and input signal independent, for 0.5 V p-p signals (sync height of 143 mV) slicing will occur at just above the 50% point and for 2 V p-p signals (sync height of 572 mV) slicing will occur at approximately 13% of sync height.

The video signal path and composite sync slicing circuitry have been optimized and compensated to achieve a low propagation delay that is stable over temperature. The typical delay is 60 ns with less than 3 ns drift over the commercial temperature range.

The typical input clamp discharge current is 11µA. This current is optimal under normal operating circumstances but needs to be increased when the clamp is trying to recover from negative going impulse noise. The device improves the recovery time by raising a NOSYNC flag when there has not been a sync pulse for approximately $1^1/_2$ horizontal lines. When this flag is raised the discharge current is increased by 85 µA so that the recovery time is sped up by nearly 10 times. Figure 13 shows a comparison between the recovery times with and without the increased discharge current.

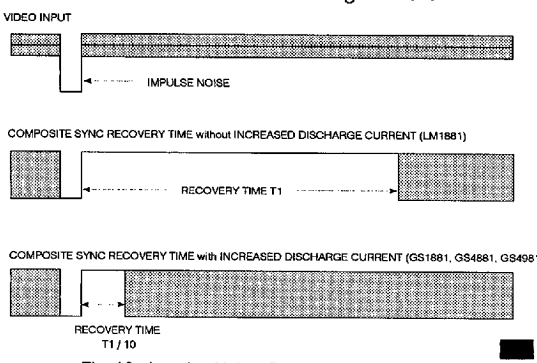


Fig. 13 Impulse Noise: Recovery Time Comparison

BACK PORCH OUTPUT (pin 5)

In an NTSC composite video signal, horizontal sync pulses are followed by the back porch interval. The device generates a negative going pulse on pin 5 during this time. It is delayed typically 500 ns from the rising edge of sync and has a typical width of 2.5 µs. Both of these times are set by the external R_{SET} resistor.

During the pre-equalizing, vertical sync, and post-equalizing periods, composite sync doubles in frequency. The GS4881 and GS4981 maintain the back porch output at the horizontal rate due to Back Porch Enable (BPEN), generated by the internal windowing circuit, which forces back porch to be asserted at the horizontal rate. This gating circuit is also the reason for the excellent impulse noise immunity of the back porch output as shown in Figure 14.

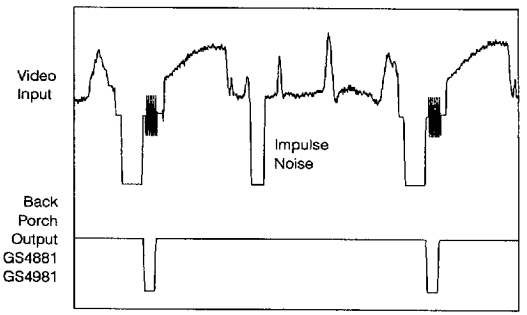


Fig. 14 Back Porch Noise Immunity

The GS1881 does not gate the Back Porch which allows for total pin compatibility with the LM1881.

VERTICAL SYNC OUTPUT (pin 3)

The vertical sync interval is detected by integrating the composite sync pulses. The first broad vertical sync pulse causes an internal capacitor to charge past a fixed threshold and raises an internal vertical flag. Once the vertical flag is raised, the positive edge of the next serration clocks out the vertical output. When the vertical sync interval ends, the first post equalizing pulse is unable to charge the capacitor sufficiently, causing the internal vertical flag to go high. The rising edge of the second post-equalizing pulse then clocks out the high flag to end the vertical sync pulse. The vertical output is clocked in and out and therefore is a fixed width of 197.7 µs (3H + 4.7 µs + 2.3 µs). In the case of a non-standard vertical interval that has no serrations, a second internal capacitor is charged and clocks the vertical pulse out after typically 65 µs. In this case the end of the vertical pulse will still be the rising edge of the second post-equalizing pulse. As the vertical detector is designed as a true integrator, it provides improved noise immunity.

ODD/EVEN FIELD OUTPUT (pin 7 GS1881, GS4881)

NTSC PAL and SECAM composite video standards are interlaced video schemes and therefore have odd and even fields. For odd fields the first broad vertical sync pulse is coincident with the start of horizontal, while for even fields the first broad vertical sync pulse starts in the middle of a horizontal line. Therefore by comparing the vertical sync with an internally generated horizontal sync the odd/even field information is determined. This output is clocked out by the falling edge of vertical sync. The odd/even output is low during even fields and high during odd fields. This method of detecting odd and even fields is very noise tolerant.

Noise during the pre-equalizing pulses does not affect the output since the field decision is made at the beginning of the vertical interval. This noise immunity is displayed in Figure 15 in which an extra pre-equalizing pulse has been added to the video input with no negative effect on the odd/even field information.

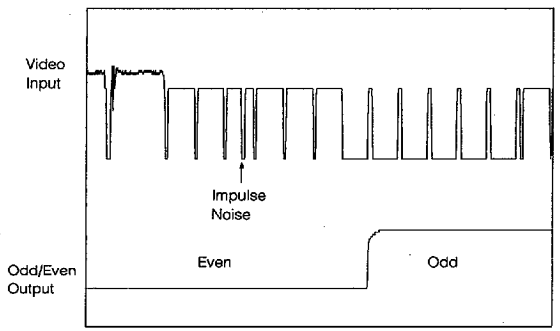


Fig. 15 Odd/Even Output

HORIZONTAL OUTPUT (pin 7 GS4981)

As mentioned above, the odd/even field output of the GS1881 and GS4881 is generated by comparing vertical sync with an internal horizontal sync signal. This horizontal sync signal is a true horizontal signal (i.e. maintained during the vertical interval) and is outputted on pin 7 for the GS4981. A delay of 190 ns from the video input and a width of 6.5 µs are typically characteristics for this signal.

The windowing circuit which generates horizontal provides excellent impulse noise immunity as shown in Figure 16. This output buffer is an open collector stage with an internal 10 kΩ pull up resistor.

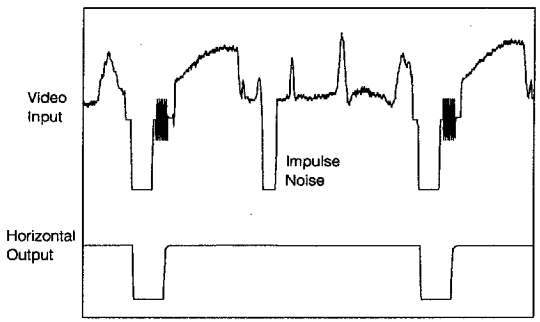


Fig. 16 Horizontal Output

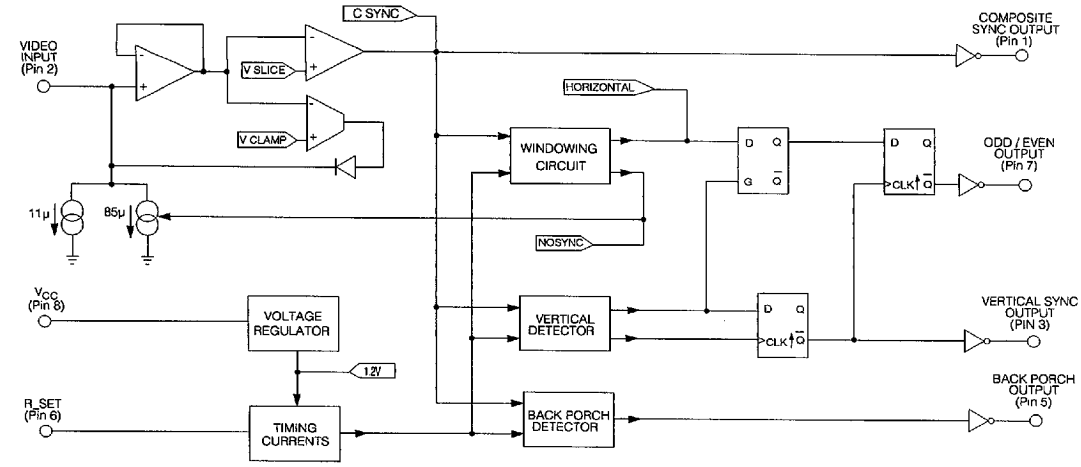


Fig. 17 GS1881 Block Diagram

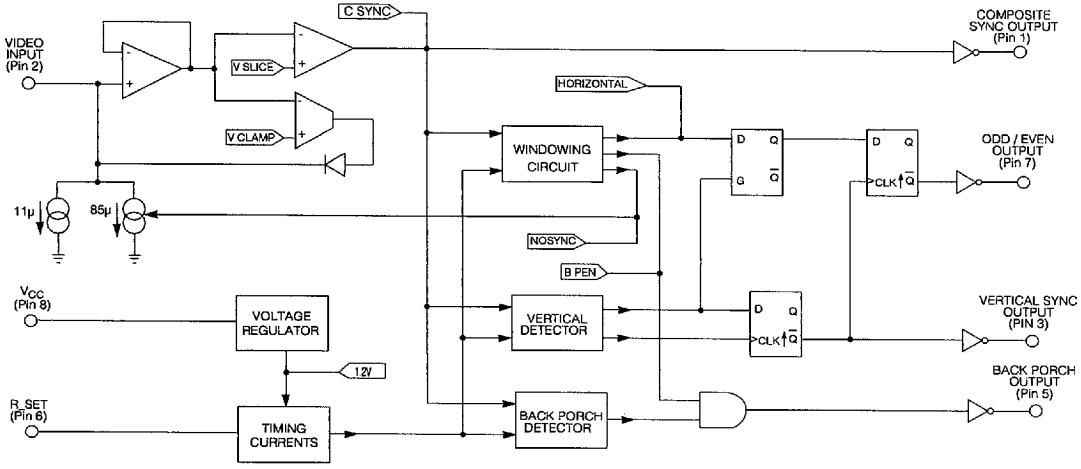


Fig. 18 GS4881 Block Diagram

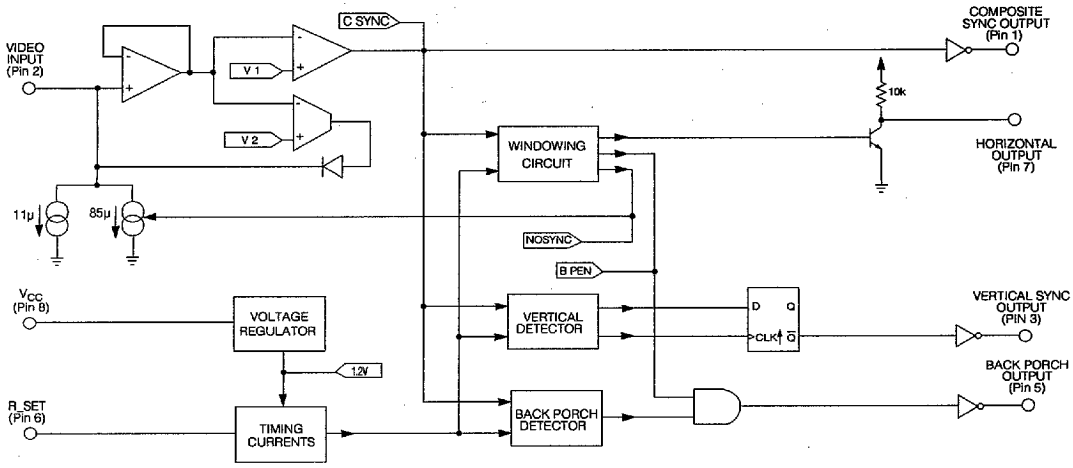


Fig. 19 GS4981 Block Diagram

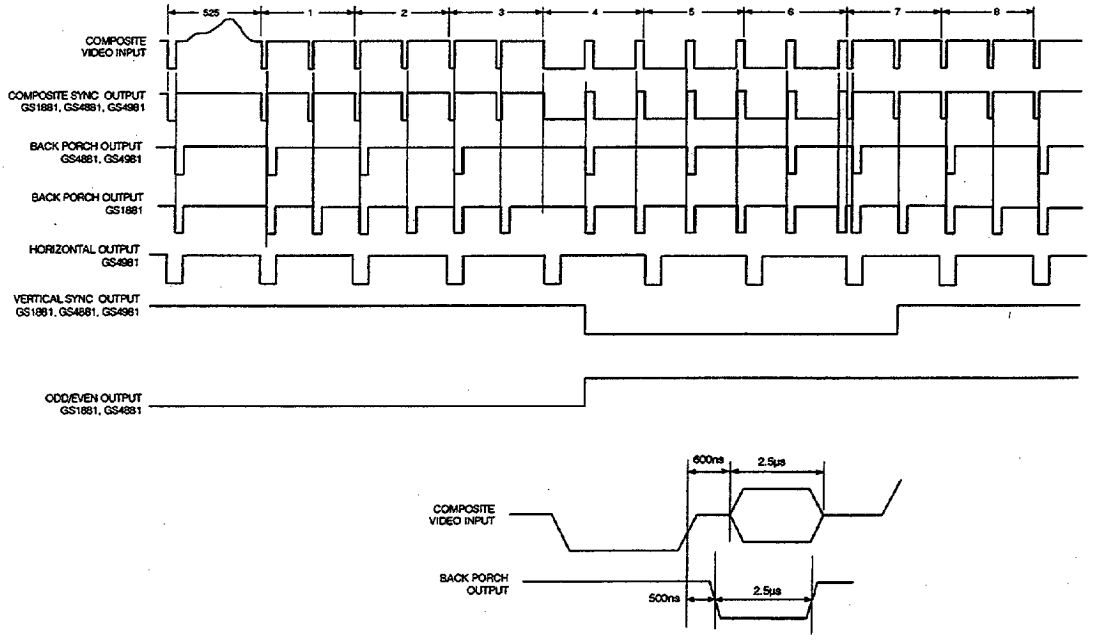


Fig. 20 GS1881, GS4881, GS4981 Video Sync Separator Timing Diagram

APPLICATION NOTES

(1) Choosing the Appropriate Input Coupling Capacitor to Optimize Slicing Level and Hum Rejection

The video designer can adjust the slicing level by choosing the value of the input coupling capacitor. The relationship between slicing level and input coupling capacitor is described by the following equation.

$$\Delta V_{SLICE} = \frac{I_{DIS}}{C_C} \Delta T = V_{DROOP}$$

where: I_{DIS} = clamp discharge current = 11 µA

$\Delta T = T_{LINE} - T_{SYNC}$ = (63.5 µs - 4.7 µs)

C_C = input coupling capacitor

Figure 21 is a graphical representation of this equation and photographs 1 and 2 show the input video waveforms for 0.1 µF and 0.01 µF input capacitors respectively. The advantage in choosing a smaller input coupling capacitor, is increased hum rejection as the following analyses illustrates.

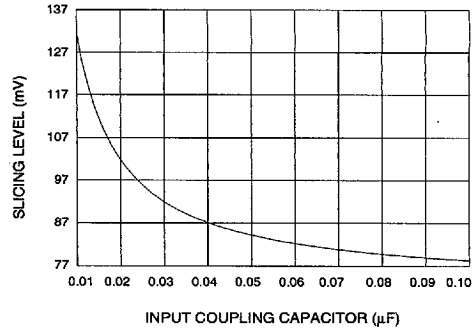
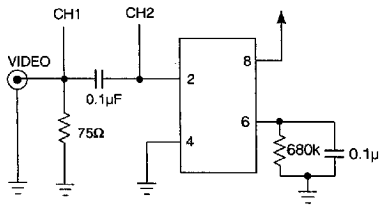
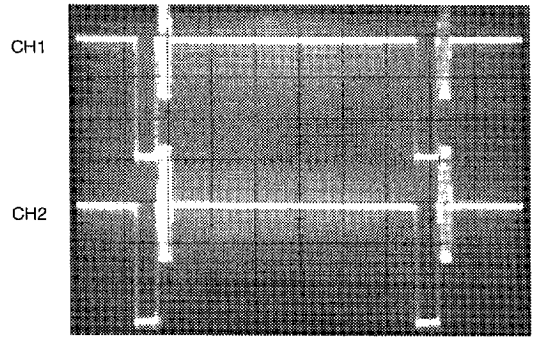


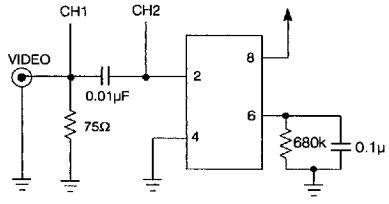
Fig. 21 Slicing Level vs Input Coupling Capacitor



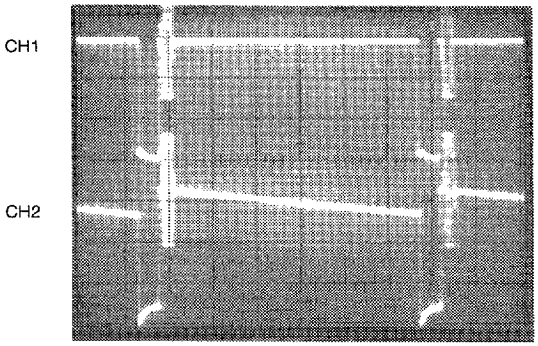
Test Circuit 1



Photograph 1



Test Circuit 2



Photograph 2

The interfering hum component is defined by:

$$V_{HUM}(t) = V_P \cos(2\pi f_{HUM} t)$$

where: V_P = Peak voltage of AC hum

f_{HUM} = Frequency of hum (50 Hz or 60 Hz)

The maximum rate of change of this hum signal occurs at the zero crossing points and is:

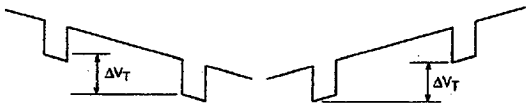
$$\left.\frac{dV_{HUM}}{dt}\right|_{t=\frac{\pi}{2},\frac{3\pi}{2}} = \pm V_P 2\pi f_{HUM}$$

Since the horizontal scan period is much faster than the period of the interference ($63.5\,\mu s << 1/f_{HUM}$) a good approximation is to assume that the maximum line to line voltage change resulting from the interfering hum is:

$$\Delta V_{HUM} = \pm V_P 2\pi f_{HUM}\ T_{LINE}$$

where: $T_{LINE} = 63.5\ \mu s$

The total line to line voltage change (ΔV_T) can then be calculated by adding the hum component (ΔV_{HUM}) and the droop component (V_{DROOP}). This calculation results in two cases:



Case A Case B

$$\Delta V_T = \Delta V_{HUM} + V_{DROOP}$$

To correct for ΔV_T in case A, the input stage must be able to charge the input capacitor ΔV_T volts in 4.7 µs. This is not a constraint as the typical clamping current of 650 µA can accomplish this for practical values of coupling capacitor.

The only way to compensate for ΔV_T in case B is to make $V_{DROOP} > \Delta V_{HUM}$. V_{DROOP} is increased by decreasing the input coupling capacitor value. Therefore the video designer can increase hum rejection by decreasing the value of this capacitor. The following is a numerical example:

$$\text{choosing } C_c = 0.022\ \mu F$$

$$\therefore V_{DROOP} = \frac{11}{0.022}(63.5\ \mu - 4.7\ \mu) = 29.4\ mV$$

the maximum amount of 60 Hz hum that could be rejected would be when:

$$\Delta V_{DROOP} = \Delta V_{HUM} = V_P\, 2\pi f_{HUM}\, T_{LINE}$$

$$\therefore V_P = \frac{\Delta V_{DROOP}}{2\pi f_{HUM} T_{LINE}} = \frac{29.4mV}{2\pi(60)\ (63.5\ \mu)} = 1.23 v_{PEAK\ HUM}$$

verifying that there is enough clamping current

$$\Delta V_t = 29.4\ mV + 29.4\ mV = 58.8\ mV$$

$$\therefore i = 0.022\,\mu \left(\frac{58.8\ mV}{4.7\ \mu}\right) = 275\ \mu A$$

which is less than 650 µA.

(2) Filtering

In order to keep the input to output delay small and temperature stable, no chrominance filtering is done within the device. External filtering may be necessary if the input signal contains large chrominance components (less than 77 mV from sync tip) or has significant amounts of high frequency noise. This filter can be a simple low pass RC network constructed by a resistance (R_S) in series with the source and a capacitor (C_f) to ground. A single pole low pass filter having a corner frequency of approximately 500 kHz will provide ample bandwidth for passing sync pulses with almost 18 dB attenuation at 3.58 MHz. Care should be taken in choosing the value of the series resistor in the filter since the source resistance seen by the sync separator affects its performance.

As the source resistance rises, the video input sync tip starts to be clipped due to the clamping current during the sync. This clamping current is relatively large due to the non-symmetric duty cycle of video. To a good approximation the amount of sync clamp current can be calculated as follows:

$$(I_{CLAMP_{AVG}})(T_{SYNC}) = (I_{DIS})(T_{LINE} - T_{SYNC})$$

$$I_{CLAMP_{AVG}}(4.7\ \mu s) = (11\ \mu A)(63.5\ \mu s - 4.7\ \mu s)$$

$$\therefore I_{CLAMP_{AVG}} = 137.6\ \mu A$$

This clamp current flows in the source resistance causing a voltage drop equal to :

$$V_{CLIP} = (I_{CLAMP_{AVG}})(R_S)$$

$$= (137.6\ \mu)(R_S)$$

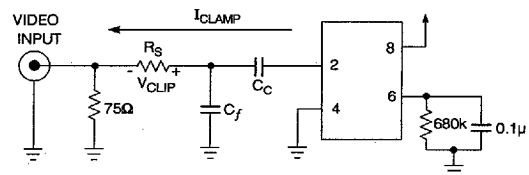
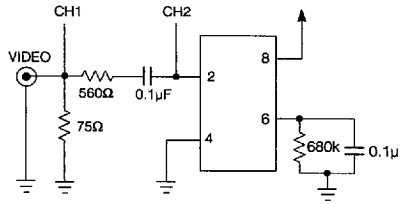


Fig. 22 Simple Chrominance Filtering

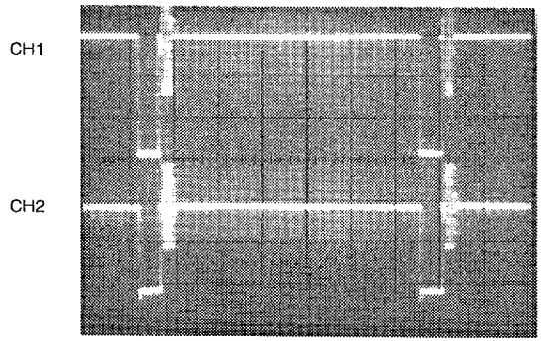
Photograph 3 shows the amount of sync clipping for a 560 Ω source resistor. A graph of V_{CLIP} versus R_S is shown in Figure 23, and Figure 24 shows the corresponding capacitor value for a particular series resistor to provide a corner frequency of 500 kHz.

In applications where signal levels are small the amount of attenuation should be minimized. It follows from Figure 23 and Figure 24 that in order to minimize attenuation a small series resistor and a larger capacitor to ground should be chosen. This however, increases the capacitive loading of the signal source.



Test Circuit 3

Another way to minimize the amount of attenuation is to control the source resistance seen by the sync separator by using a PNP emitter follower (Figure 25). A PNP emitter follower works well to drive the sync separator, and does not require much DC current because the transistor provides the current when it is needed during sync. Figure 26 is a typical application circuit that minimizes sync tip clipping.



Photograph 3

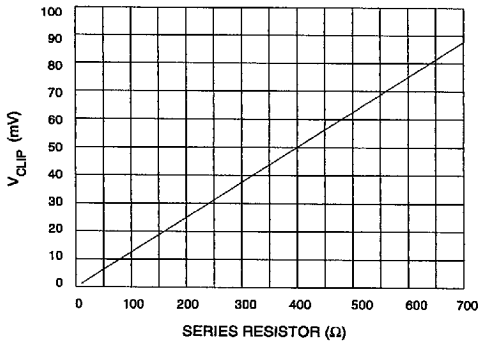


Fig. 23 V_{CLIP} vs Series Resistor

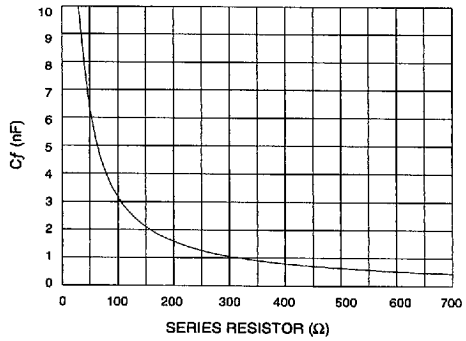


Fig. 24 Cf vs Series Resistor

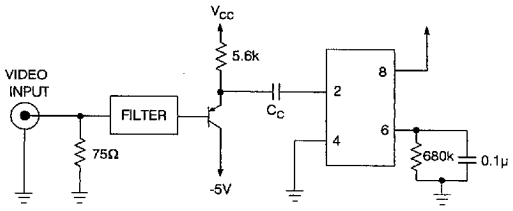


Fig. 25 PNP Emitter Follower Buffer

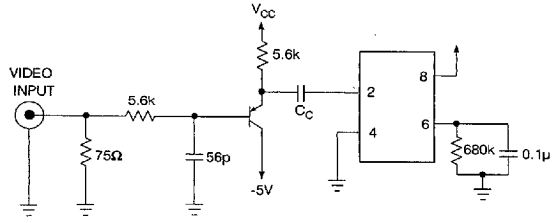


Fig. 26 Typical NTSC Application Circuit

(3) Deriving Odd/Even Using the GS4981

Odd/even field information can be derived using the vertical and horizontal outputs from the GS4981 along with an external positive edge D flip/flop. The horizontal output is used as the D input and the vertical output as the clock, as shown in Figure 27.

At the start of an odd field the vertical output ends in the middle of the horizontal line and a high will be latched. At the start of an even field, the vertical output ends near the beginning of the horizontal line and since the horizontal output is low, a low will be latched. This timing sequence is shown in Figure 28.

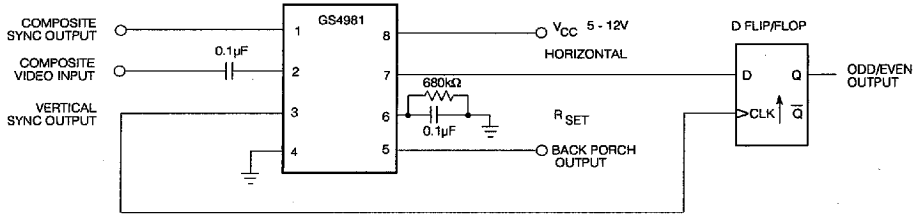


Fig. 27 Derivation of Odd/Even with GS4981

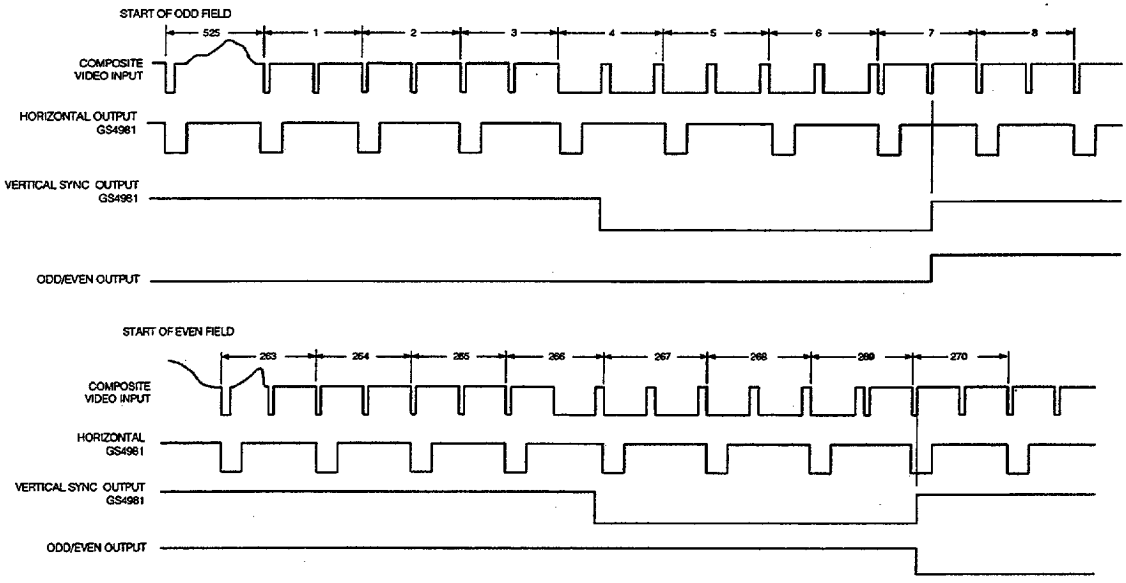


Fig. 28 Timing Diagram

REVISION NOTES
The only change from 520-23-02 to 520-23-03 is that the document has been upgraded to a full DATA SHEET. It is no longer Preliminary.