

**NM93CS06/CS46/CS56/CS66**  
**(MICROWIRE™ Bus Interface) 256-/1024-/2048-/4096-Bit**  
**Serial EEPROM with Data Protect and Sequential Read**

## General Description

The NM93CS06/CS46/CS56/CS66 devices are 256/1024/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. Selected registers can be protected against data modification by programming the Protect Register with the address of the first register to be protected against data modification (all registers greater than, or equal to, the selected address are then protected from further change). Additionally, this address can be "locked" into the device, making all future attempts to change data impossible. These devices are fabricated using National Semiconductor floating-gate CMOS process for high reliability, high endurance and low power consumption. The NM93CSXX Family is offered in both SO and TSSOP packages for small space considerations.

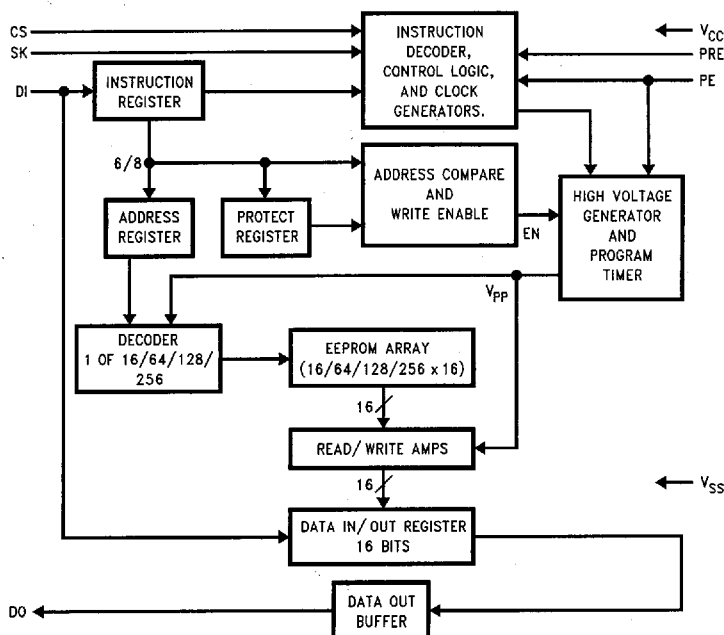
The EEPROM interfacing is MICROWIRE compatible providing simple interfacing to standard microcontrollers and microprocessors. There are a total of 10 instructions, 5 which operate on the EEPROM memory, and 5 which operate on the Protect Register. The memory instructions are

READ, WRITE, WRITE ALL, WRITE ENABLE, and WRITE DISABLE. The Protect register instructions are PRREAD, PRWRITE, PRENABLE, PRCLEAR, and PRDISABLE.

## Features

- Write protection in a user defined section of memory
- Sequential register read
- Typical active current of 200  $\mu$ A and standby current of 10  $\mu$ A
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self timed write cycle
- Device status during programming mode
- 40 year data retention
- Endurance:  $10^6$  data changes
- 4.5V to 5.5V operation in all modes of operation
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

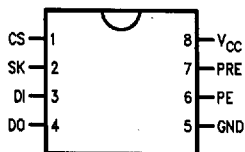
### Block Diagram



TL/D/10750-1

## Connection Diagram

Dual-In-Line Package (N)  
8-Pin SO (M8) and 8-Pin TSSOP (MT8)



NS Package Number  
N08E, M08A and MTC08

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### Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V <sub>CC</sub>	Power Supply

## Ordering Information

### Commercial Temp. Range (0°C to +70°C)

Order Number
NM93CS06N/NM93CS46N/NM93CS56N/NM93CS66N
NM93CS06M8/NM93CS46M8/NM93CS56M8/NM93CS66M8
NM93CS46MT8/NM93CS56MT8/NM93CS66MT8

### Extended Temp. Range (-40°C to +85°C)

Order Number
NM93CS06EN/NM93CS46EN/NM93CS56EN/NM93CS66EN
NM93CS06EM8/NM93CS46EM8/NM93CS56EM8/NM93CS66EM8
NM93CS46EMT8/NM93CS56EMT8/NM93CS66EMT8

### Automotive Temp. Range (-40°C to +125°C)

Order Number
NM93CS06VN/NM93CS46VN/NM93CS56VN/NM93CS66VN
NM93CS06VM8/NM93CS46VM8/NM93CS56VM8/NM93CS66VM8
NM93CS46VMT8/NM93CS56VMT8/NM93CS66VMT8

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

**Operating Conditions**

Ambient Operating Temperature	0°C to +70°C
NM93CSxx	-40°C to +85°C
NM93CSxxE	-40°C to +125°C
NM93CSxxV	4.5V to 5.5V
Power Supply (V <sub>CC</sub> )	

**DC and AC Electrical Characteristics** V<sub>CC</sub> = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I <sub>CCA</sub>	Operating Current	NM93CS06-NM93CS66 NM93CS06E/V-NM93CS66E/V	CS = V <sub>IH</sub> , SK = 1.0 MHz SK = 1.0 MHz		1 1	mA
I <sub>CCS</sub>	Standby Current	NM93CS06-NM93CS66 NM93CS06E/V-NM93CS06E/V	CS = V <sub>IL</sub>		50 50	μA
I <sub>IL</sub> I <sub>OL</sub>	Input Leakage Output Leakage		V <sub>IN</sub> = 0V to V <sub>CC</sub> (Note 3)		± 1	μA
V <sub>IL</sub> V <sub>IH</sub>	Input Low Voltage Input High Voltage			-0.1 2	0.8 V <sub>CC</sub> + 1	V
V <sub>OL1</sub> V <sub>OH1</sub>	Output Low Voltage Output High Voltage		I <sub>OL</sub> = 2.1 mA I <sub>OH</sub> = -400 μA	2.4	0.4	V
V <sub>OL2</sub> V <sub>OH2</sub>	Output Low Voltage Output High Voltage		I <sub>OL</sub> = 10 μA I <sub>OH</sub> = -10 μA	V <sub>CC</sub> - 0.2	0.2	V
f <sub>SK</sub>	SK Clock Frequency	NM93CS06-NM93CS66 NM93CS06E/V-NM93CS66E/V	(Note 4)	0 0	1 1	MHz
t <sub>SKH</sub>	SK High Time	NM93CS06-NM93CS66 NM93CS06E/V-NM93CS66E/V		250 300		ns
t <sub>SKL</sub>	SK Low Time			250		ns
t <sub>SKS</sub>	SK Setup Time		SK Must Be at V <sub>IL</sub> for t <sub>SKS</sub> before CS goes high	50 50 100		ns
t <sub>CS</sub>	Minimum CS Low Time	NM93CS06-NM93CS66 NM93CS06E/V-NM93CS66E/V	(Note 2)	250 250		ns
t <sub>CSS</sub>	CS Setup Time			100		ns
t <sub>PRES</sub>	PRE Setup Time	NM93CS06-NM93CS66 NM93CS06E/V-NM93CS66E/V		50 50		ns
t <sub>DH</sub>	DO Hold Time			70		ns
t <sub>PES</sub>	PE Setup Time	NM93CS06-NM93CS66 NM93CS06E/V-NM93CS66E/V		50 50		ns
t <sub>DIS</sub>	DI Setup Time	NM93CS06-NM93CS66 NM93CS06E/V-NM93CS66E/V		100 100		ns
t <sub>CSH</sub>	CS Hold Time			0		ns

**DC and AC Electrical Characteristics**  $V_{CC} = 4.5V$  to  $5.5V$  unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
$t_{PEH}$	PE Hold Time	NM93CS06–NM93CS66 NM93CS06E/V–NM93CS66E/V		250 250		ns
$t_{PREH}$	PRE Hold Time			50		ns
$t_{DIH}$	DI Hold Time			20		ns
$t_{PD1}$	Output Delay to "1"	NM93CS06–NM93CS66 NM93CS06E/V–NM93CS66E/V			500 500	ns
$t_{PD0}$	Output Delay to "0"	NM93CS06–NM93CS66 NM93CS06E/V–NM93CS66E/V			500 500	ns
$t_{SV}$	CS to Status Valid	NM93CS06–NM93CS66 NM93CS06E/V–NM93CS66E/V			500 500	ns
$t_{DF}$	CS to DO in TRI-STATE®	NM93CS06–NM93CS66 NM93CS06E/V–NM93CS66E/V	CS = $V_{IL}$		100 100	ns
$t_{WP}$	Write Cycle Time				10	ms

**Capacitance**  $T_A = 25^\circ C$ ,  $f = 1$  MHz

Symbol	Test	Typ	Max	Units
$C_{OUT}$	Output Capacitance		5	pF
$C_{IN}$	Input Capacitance		5	pF

**Note 1:** Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2:** CS (Chip Select) must be brought low (to  $V_{IL}$ ) for an interval of  $t_{CS}$  in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (this is shown in the opcode diagrams in the following pages).

**Note 3:** Typical leakage values are in the 20 nA range.

**Note 4:** The shortest allowable SK clock period =  $1/f_{SK}$  (as shown under the  $f_{SK}$  parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both  $t_{SKH}$  and  $t_{SKL}$  limits must be observed. Therefore, it is not allowable to set  $1/f_{SK} = t_{SKH}(\text{minimum}) + t_{SKL}(\text{minimum})$  for shorter SK cycle time operation.

**AC Test Conditions**

$V_{CC}$ Range	$V_{IL}/V_{IH}$ Input Levels	$V_{IL}/V_{IH}$ Timing Level	$V_{OL}/V_{OH}$ Timing Level	$I_{OL}/I_{OH}$
$4.5V \leq V_{CC} \leq 5.5V$ (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	–2.1 mA/ 0.4 mA

Output Load: 1 TTL Gate ( $C_L = 100$  pF)

## Functional Description

The NM93CSxx EEPROM Family has 10 instructions as described below. All Data-In signals are clocked into the device on the low-to-high SK transition.

### Read and Sequential Register Read (READ):

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the **sequential register read** mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

### Write Enable (WEN):

When  $V_{CC}$  is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or  $V_{CC}$  is completely removed from the part.

### Write (WRITE):

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after the  $t_{CS}$  interval. D0 = logical 0 indicates that programming is still in progress. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

### Write All (WRALL):

The WRALL instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction, however, after loading the instruction the PE pin becomes a "don't care". As in the WRITE mode, the D0 pin indicates the READY/BUSY status of the chip if CS is brought high after the  $t_{CS}$  interval. This function is **DISABLED** if the Protect Register is in use to lock out a section of memory.

### Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

**Note:** For all Protect Register Operations: If the PRE pin is not held at  $V_{IH}$ , all instructions will be applied to the EEPROM array, rather than the Protect Register.

### Protect Register Read (PRREAD):

The PRREAD instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction sequence. Following the PRREAD instruction: the 6- or 8-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6- or 8-bit address string.

### Protect Register Enable (PREN):

The PREN instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction sequence.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

### Protect Register Clear (PRCLEAR):

The PRCLEAR instruction clears the address stored in the Protect Register and, therefore, enables all registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction sequence, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Please note that the PRCLEAR instruction and the PRWRITE instruction will both program the Protect Register with all 1s. However, the PRCLEAR instruction will allow the LAST register to be programmed, whereas the PRWRITE instruction = all 1s will PREVENT the last register from being programmed. In addition, the PRCLEAR instruction will allow the use of the WRALL command, where the PRWRITE = all 1s will lock out the Bulk programming opcode.

### Protect Register Write (PRWRITE):

The PRWRITE instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

### Protect Register Disable (PRDS):

The PRDS instruction is a **ONE TIME ONLY** instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

### Instruction Set for the NM93CS06 and NM93CS46

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5-A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Enable all programming modes.
WRITE	1	01	A5-A0	D15-D0	0	1	Writes address if unprotected.
WRALL	1	00	01XXXX	D15-D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming modes.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE.
PRWRITE	1	01	A5-A0		1	1	Programs address into Protect Register. Thereafter, memory addresses $\geq$ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	ONE TIME ONLY instruction after which the address in the Protect Register cannot be altered.

**Note:** Address bits A5 and A4 become "Don't Care" for the NM93CS06.

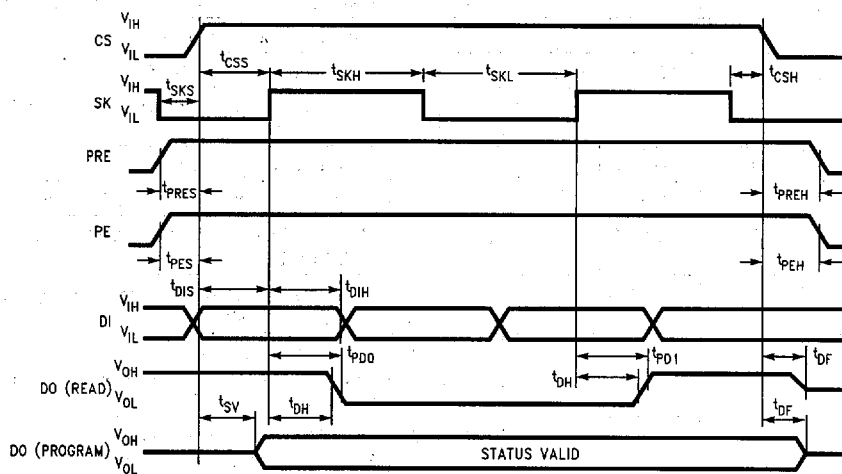
### Instruction Set for the NM93CS56 and NM93CS66

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7-A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Enable all programming modes.
WRITE	1	01	A7-A0	D15-D0	0	1	Writes address if unprotected.
WRALL	1	00	01XXXXXX	D15-D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming modes.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A7-A0		1	1	Programs address into Protect Register. Thereafter, memory addresses $\geq$ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	ONE TIME ONLY instruction after which the address in the Protect Register cannot be altered.

**Note:** Address bit A7 becomes "Don't Care" for the NM93CS56.

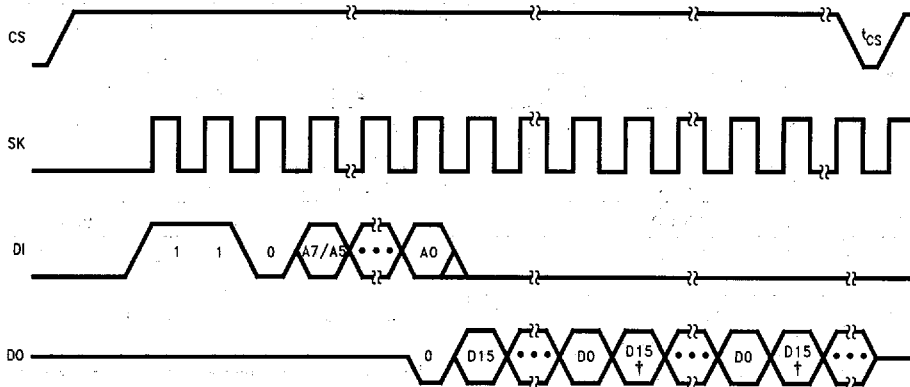
# Timing Diagrams

## Synchronous Data Timing



TL/D/10750-15

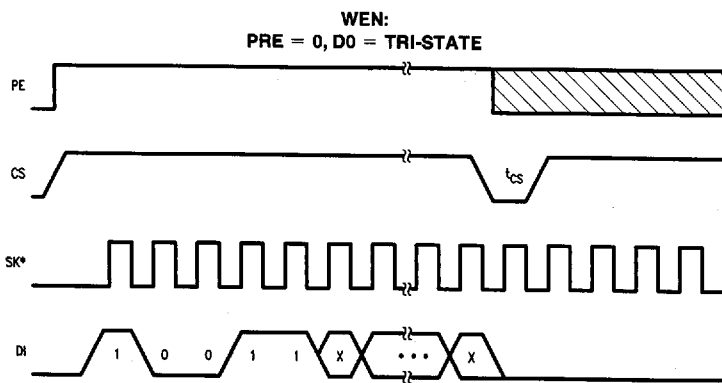
**READ:**  
PRE = 0, PE = X



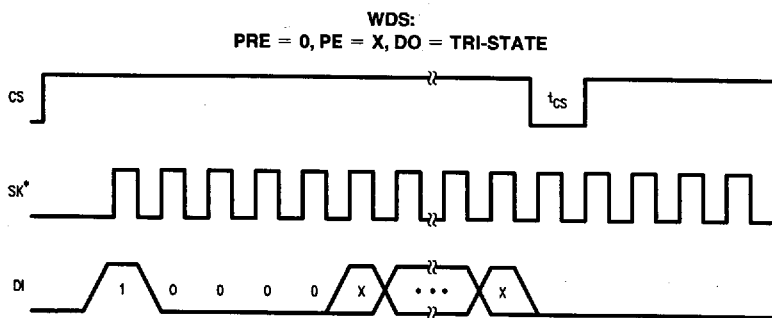
†The memory automatically cycles to the next register with continued clocking of SK.

TL/D/10750-4

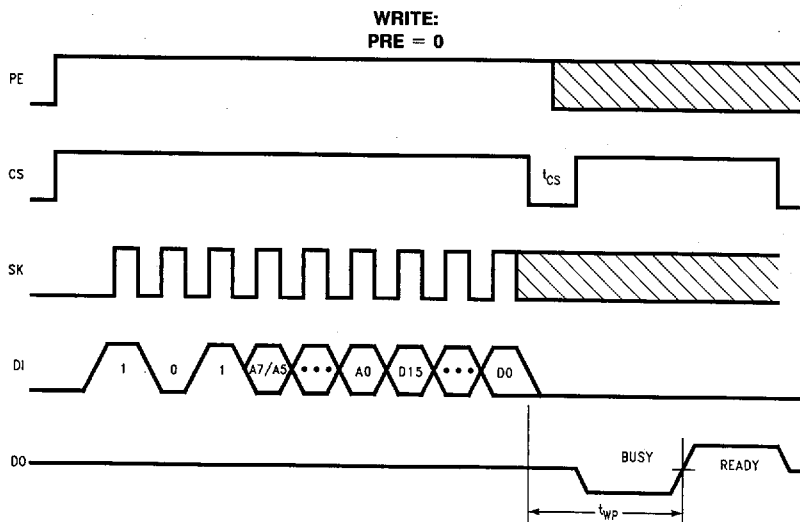
# Timing Diagrams (Continued)



TL/D/10750-5



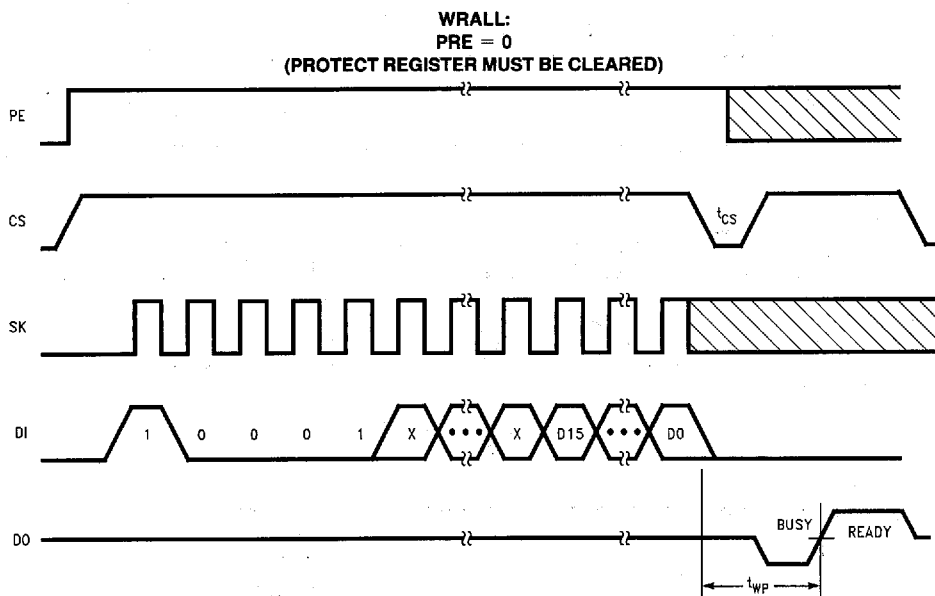
TL/D/10750-6



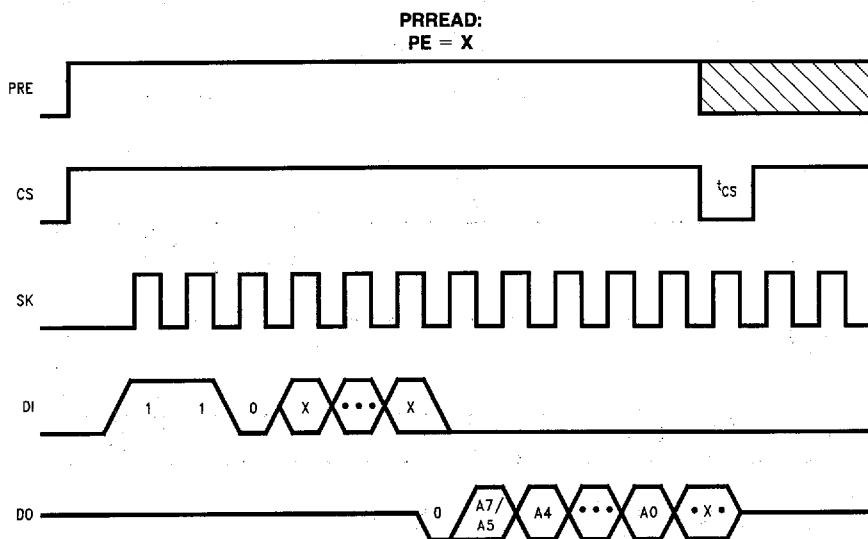
TL/D/10750-7



# Timing Diagrams (Continued)



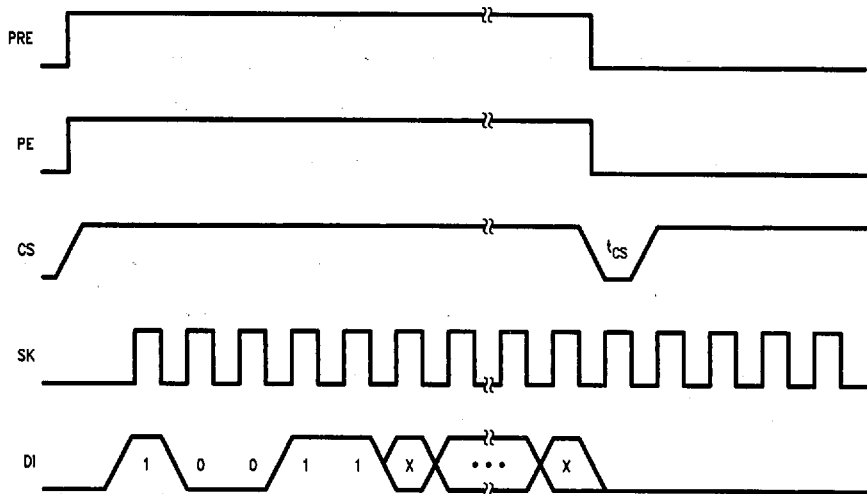
TL/D/10750-8



TL/D/10750-9

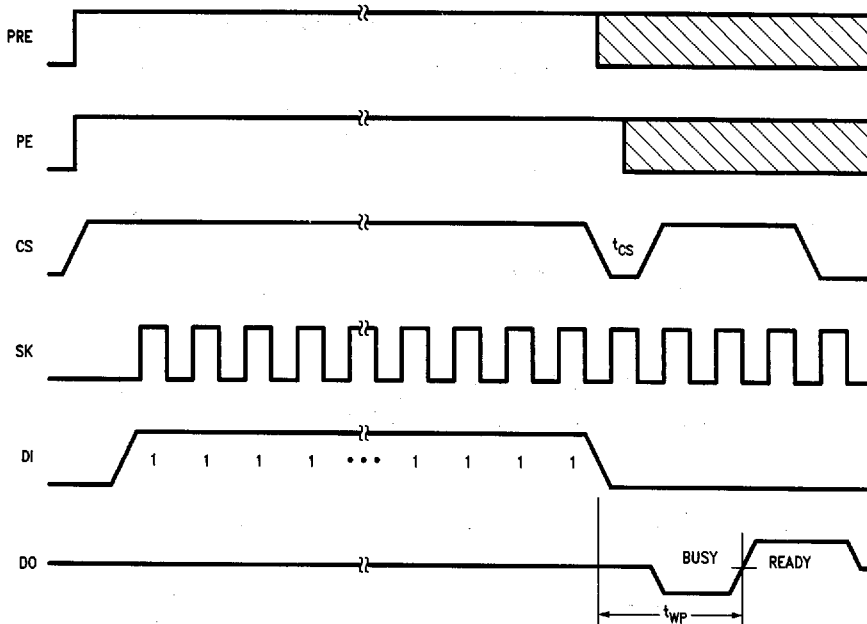
# Timing Diagrams (Continued)

**PREN:**  
D0 = TRI-STATE  
(A WEN CYCLE MUST PRECEDE A PREN CYCLE)



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**PRCLEAR:**  
(A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRCLEAR CYCLE)

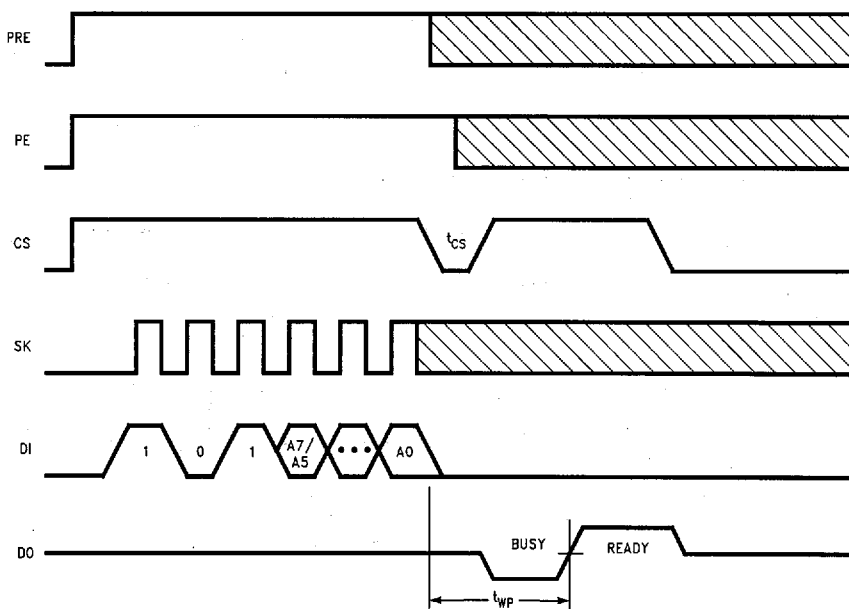


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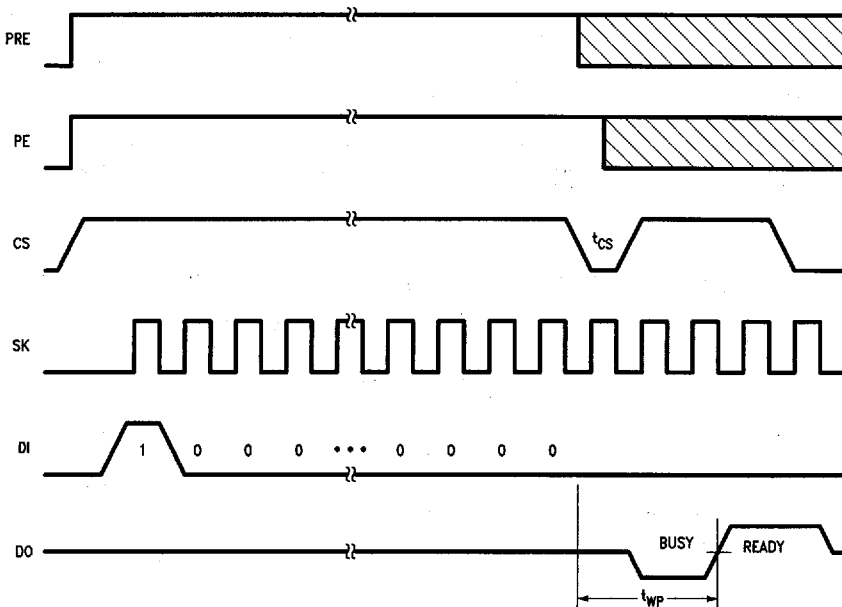
# Timing Diagrams (Continued)

**PRWRITE:**  
(PREN CYCLES MUST IMMEDIATELY PRECEDE A PRWRITE CYCLE.)



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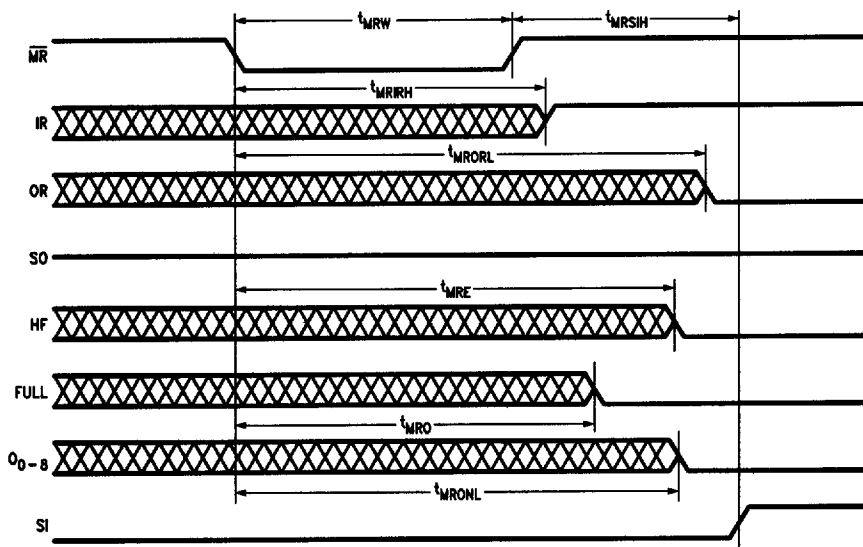
**PRDS:**  
(\*ONE TIME ONLY INSTRUCTION. A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRDS CYCLE.)



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**Functional Description** (Continued)**Mode 2: Master Reset****Sequence of Operation**

1. Input and Output Ready, HF and FULL can be in any state before the reset sequence with Master Reset ( $\overline{MR}$ ) HIGH.
2. Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width  $t_{MRW}$  before rising again.
3. Master Reset rises.
4. IR rises (if not HIGH already) to indicate ready to write state recovery time  $t_{MRRH}$  after the falling edge of  $\overline{MR}$ . Both HF and FULL will go LOW indicating an empty FIFO, occurring recovery times  $t_{MRE}$  and  $t_{MRO}$  respectively after the falling edge of  $\overline{MR}$ . OR falls recovery time  $t_{MRORL}$  after  $\overline{MR}$  falls. Data at outputs goes LOW recovery time  $t_{MRONL}$  after  $\overline{MR}$  goes LOW.
5. Shift-In can be taken HIGH after a minimum recovery time  $t_{MRSIH}$  after  $\overline{MR}$  goes HIGH.

**FIGURE 2. Mode of Operation Mode 2**

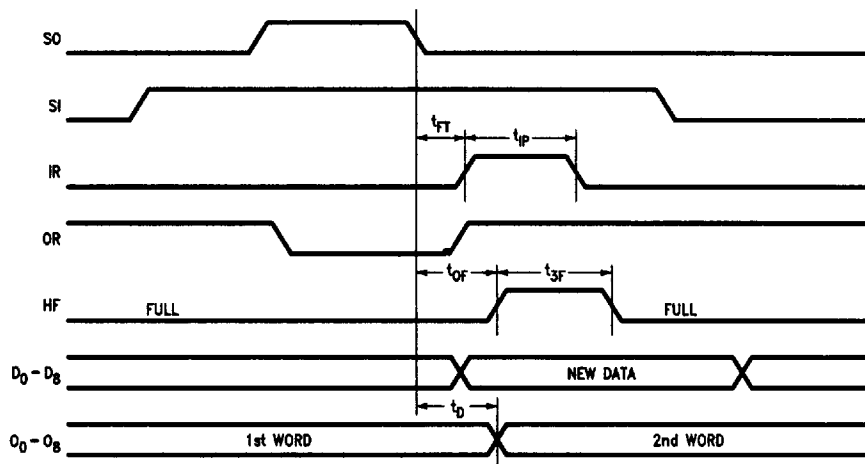
TL/F/10144-6

## Functional Description (Continued)

### Mode 3: With FIFO Full, Shift-In is Held HIGH In Anticipation of an Empty Location

#### Sequence of Operation

1. The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. Shift-Out is LOW. IR is LOW.
2. Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after propagation delay  $t_D$ . New data is written into the FIFO after SO goes LOW.
3. Input Ready goes HIGH one fall-through time,  $t_{FT}$ , after the falling edge of SO. Also, HF goes HIGH one  $t_{OF}$  after SO falls, indicating that the FIFO is no longer full.
4. IR returns LOW pulse width  $t_P$  after rising and shifting new data in. Also, HF returns LOW pulse width  $t_{3F}$  after rising, indicating the FIFO is once more full.
5. Shift-In is brought LOW to complete the shift-in process and maintain normal operation



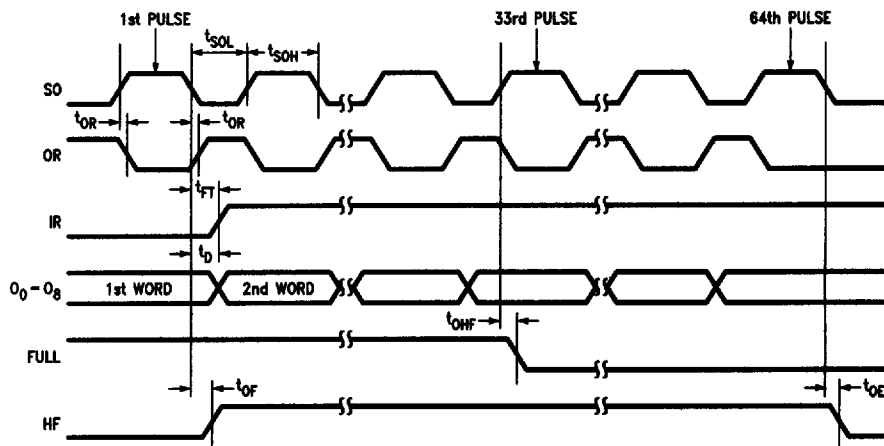
TL/F/10144-7

Note: MR and FULL are HIGH; OE is LOW.

FIGURE 3. Modes of Operation Mode 3

**Functional Description** (Continued)**Mode 4: Shift-Out Sequence, FIFO Full to Empty****Sequence of Operation**

1. FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.
2. SO goes HIGH, resulting in OR going LOW one propagation delay,  $t_{OR}$ , after SO rises. OR LOW indicates output stage is busy.
3. SO goes LOW, new data reaches output one propagation delay,  $t_D$ , after SO falls; OR goes HIGH one propagation delay,  $t_{OR}$ , after SO falls and HF rises one propagation delay,  $t_{OF}$ , after SO falls. IR rises one fall-through time,  $t_{FT}$ , after SO falls.
4. Repeat process through the 64th SO pulse. FULL flag goes LOW one propagation delay,  $t_{OHF}$ , after the rising edge of 33rd SO, indicating that the FIFO is less than half full. On the falling edge of the 64th SO, HF goes LOW one propagation delay,  $t_{OE}$ , after SO, indicating the FIFO is empty. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.



Note: SI and  $\overline{OE}$  are LOW;  $\overline{MR}$  is HIGH; D<sub>0</sub>-D<sub>8</sub> are immaterial.

**FIGURE 4. Modes of Operation Mode 4**

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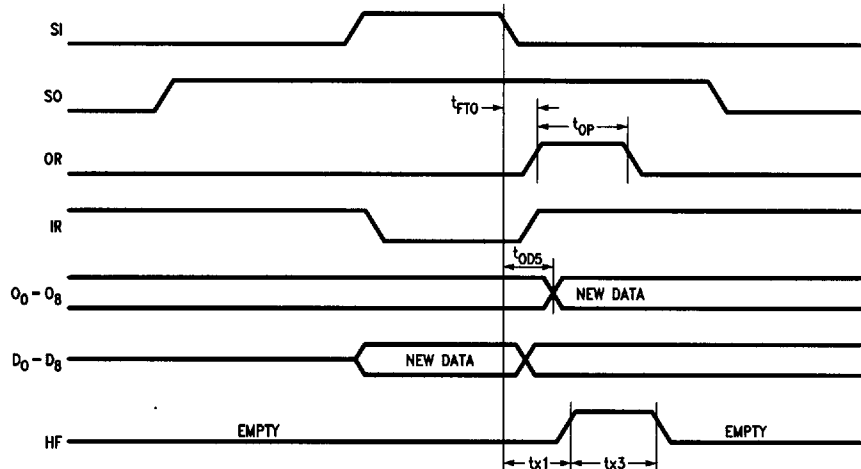
Functional Description (Continued)

Mode 5: With FIFO Empty, Shift-Out is Held HIGH In Anticipation of Data

Sequence of Operation

- 1. FIFO is initially empty; Shift-Out goes HIGH.
- 2. Shift-In pulse loads data into the FIFO and IR falls. HF rises propagation delay  $t_{x1}$  after the falling edge of SI.
- 3. OR rises a fall-through time of  $t_{FTO}$  after the falling edge of Shift-In, indicating that new data is ready to be output.

- 4. Data arrives at output one propagation delay,  $t_{OD5}$ , after the falling edge of Shift-In.
- 5. OR goes LOW pulse width  $t_{OP}$  after rising and HF goes LOW pulse width  $t_{x3}$  after rising, indicating that the FIFO is empty once more.
- 6. Shift-Out goes LOW, necessary to complete the Shift-Out process.



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Note: FULL is LOW;  $\overline{MR}$  is HIGH;  $\overline{OE}$  is LOW;  $t_{OPF} = t_{FTO} - t_{OD5}$ . Data output transition—valid data arrives at output stage  $t_{OPF}$  after OR is HIGH.

FIGURE 5. Modes of Operation Mode 5