FAIRCHILD SEMICONDUCTOR™

July 1998

NM95MS18
Plug & Play Front-end device for ISA-Bus Systems (Supports Windows®-NT, UNIX® and legacy systems)

General Description

The NM95MS18 is an industry standard ISA Plug-n-Play controller that also supports Non-Plug-n-Play platforms like DOS, WIN3.1x, Windows-NT and Unix.

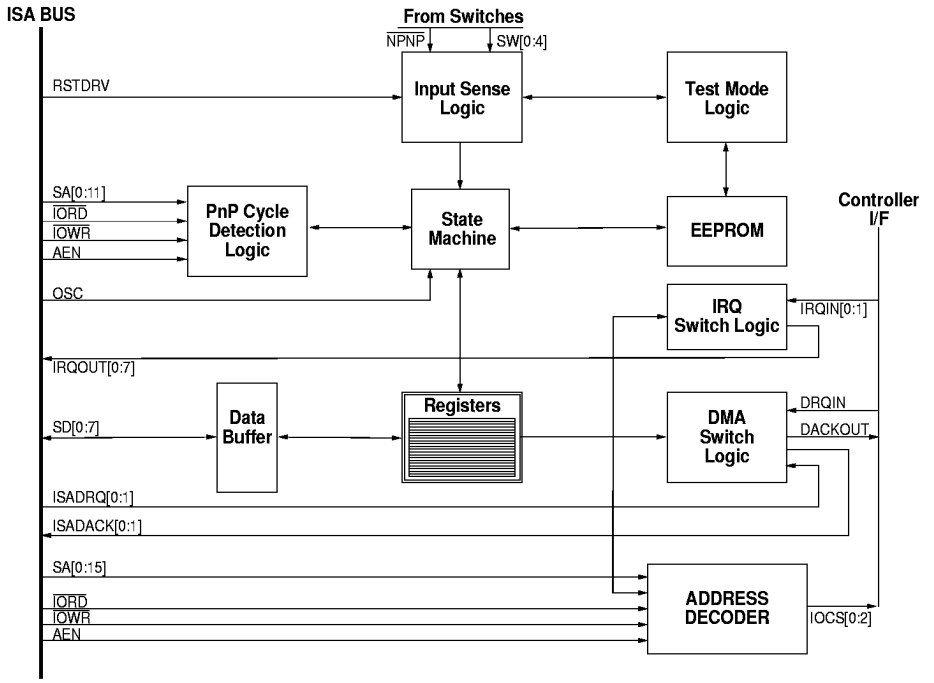
In additon to being completely compliant to ISA PnP Specification (Ver 1.0a), NM95MS18 integrates a total of 4Kbit of onchip EEPROM for both PnP Resource data as well as non-PnP configuration data to provide a true single chip solution.

NM95MS18 supports one logical device offering a flexible choice of DMA, Interrupt and I/O address decoding features within a single chip. NM95MS18 is implemented using Fairchild's Advanced CMOS process and operates on a single power supply.

Features

- Fully compliant with industry standard ISA PnP specification (Ver. 1.0a)
- Supports Non-PnP platforms like WINDOWS-NT, UNIX, DOS/WIN3.1x
  — No configuration utilities needed
- Supports Non-PnP "legacy" mode
  — Can be programmed to power-up in 31 settings
- On-chip "Write-Protected" EEPROM for:
  — PnP Resource data (2Kbits)
  — 31 Power-on "legacy" configurations (2Kbits)
- Two modes of operation:
  — DMA Mode
  — Extended Interrupt Mode (supports PC-97 requirements)
- Configurable Interrupt types:
  — TTL O/P
  — Open Drain O/P
- Supports Wire-AND I/O chipselects
- Fully compatible with NM95MS16
- Available in 52-Pin PLCC Package

Block Diagram



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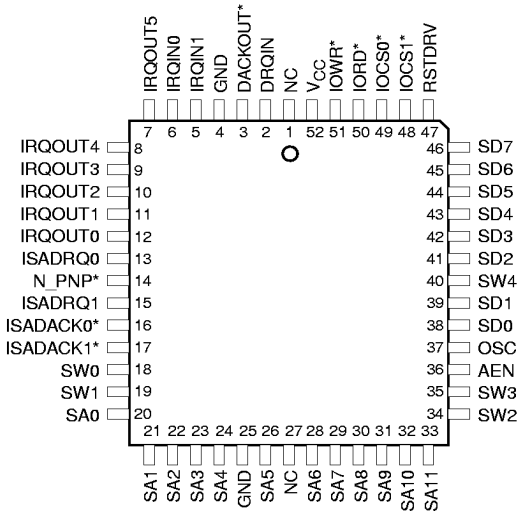
Block Signal Description

Signal	Type	Description
SA[0:11]	I	Address inputs from the ISA bus.
SA[12:15]†	I	Address inputs from the ISA bus.
IORD*	I	I/O Read strobe from the ISA bus.
IOWR*	I	I/O Write strobe from the ISA bus.
AEN	I	Address Enable Strobe from ISA bus.
OSC	I	14.31818 MHz clock source from ISA bus.
RSTDRV	I	Reset signal from ISA bus.
SD[0:7]	I/O	ISA Data bus.
IRQIN0	I	Source Interrupt signal from onboard controller.
IRQIN1†	I	Source Interrupt signal from onboard controller.
IRQOUT[0:5]	O	Interrupt output signals from NM95MS18. Can be connected to any of ISA IRQ channels.
IRQOUT[6:7] †	O	Interrupt output signals from NM95MS18. Can be connected to any of ISA IRQ channels.
DRQIN†	I	Source DMA request signal from onboard controller to NM95MS18.
ISADRQ[0:1] †	O	DMA request output signals from NM95MS18. Can be connected to any of ISA DMA channels
ISADACK[0:1]* †	I	DMA Acknowledge output signals from respective ISA DMA channels to which ISADRQ[0:1] are connected.
DACKOUT* †	I	DMA acknowledge signal from NM95MS18 to onboard controller.
IOCS[0:1]*	O	Programmable chipselects from NM95MS18 to onboard controller.
IOCS[2]* †	O	Programmable chipselects from NM95MS18 to onboard controller.
N_P 'N' P*	I	Input signal selecting either PNP mode or N_PNP mode of NM95MS18. This signal has a weak internal pull-up resistor defaulting to PnP mode and can be directly connected to ground . This signal is used in conjunction with SW[0:4] inputs. “1” - PNP mode. “0” - N_PNP mode.
SW[0:4]	I	Input signals to NM95MS18 selecting 1-out-of-31 Non-Plug-n-Play configurations. All these signals have a weak internal pull-up resistor and can be directly connected to ground. These signals are used in conjunction with N_PNP signal.

* Signal name with a “*” indicates active low signal.

† Multiplexed signals. Please refer Pinout Details.



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PLCC Pins

Pinout Details for NM95MS18 (PLCC Package)

Pin #	Pin Name	
Mode	DMA	Ext. Intr
1	NC	NC
2** (Note 3)	DRQIN	SA15
3**	DACKOUT*	IOCS2*
4	GND	GND
5**	IRQIN1	SA14
6	IRQIN0	IRQIN0
7	IRQOUT5	IRQOUT5
8	IRQOUT4	IRQOUT4
9	IRQOUT3	IRQOUT3
10	IRQOUT2	IRQOUT2
11	IRQOUT1	IRQOUT1
12	IRQOUT0	IRQOUT0
13**	ISADRQ0	IRQOUT6
14	N_PnP	N_PnP
15**	ISADRQ1	IRQOUT7
16**	ISADACK0*	SA12
17**	ISADACK1*	SA13
18	SW0	SW0
19	SW1	SW1
20	SA0	SA0
21	SA1	SA1
22	SA2	SA2
23	SA3	SA3
24	SA4	SA4
25	GND	GND
26	SA5	SA5

Pin #	Pin Name	
Mode	DMA	Ext. Intr
27	NC	NC
28	SA6	SA6
29	SA7	SA7
30	SA8	SA8
31	SA9	SA9
32	SA10	SA10
33	SA11	SA11
34	SW2	SW2
35	SW3	SW3
36	AEN	AEN
37	OSC	OSC
38	SD0	SD0
39	SD1	SD1
40	SW4	SW4
41	SD2	SD2
42	SD3	SD3
43	SD4	SD4
44	SD5	SD5
45	SD6	SD6
46	SD7	SD7
47	RSTDRV	RSTDRV
48	IOCS1*	IOCS1*
49	IOCS0*	IOCS0*
50	IORD*	IORD*
51	IOWR*	IOWR*
52	V_{CC}	V_{CC}

** Pins with multiplexed signals

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	–65°C to +150°C
All Input or Output Voltages with Respect to Ground	V_{CC} + 1V to –0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature NM95MS18	0°C to +70°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook sepcifications.

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 2)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		TBD	10.0	mA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.2	1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			1.0	µA
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1.0	V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA (Note 4) I_{OL} = 2.1 mA (Note 5)			0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = -3 mA (Note 4) I_{OH} = -400 µA (Note 5)	2.4 2.4			V V

Capacitance T_A = +25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test Conditions	Min	Max	Units
$C_{I/O}$ (Note 3)	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 3)	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT} (Note 3)	Output Capacitance	V_{OUT} = 0V	6	pF

Note 2: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: These values are for ISA signals like SD[0:7], IRQx, DRQx.

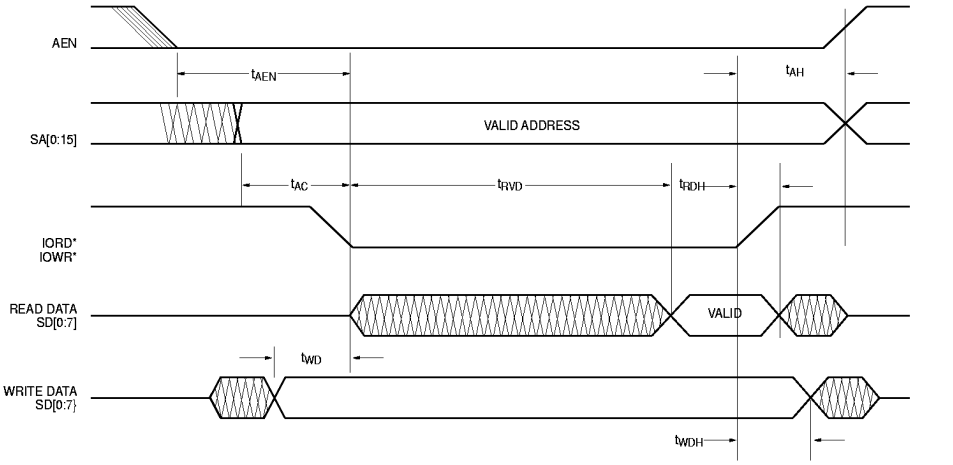
Note 5: These values are for card signal like IOCS[0:2]*, DO(EEPROM)

AC Electrical characteristics

Symbol	Parameter	Min	Max	Unit
t_{AEN}	AEN valid to command active	100		ns
t_{AC}	Address valid to command active	88		ns
t_{RVD}	Active read to valid data		150	ns
t_{AH}	Address, AEN hold from inactive command	30		ns
t_{RDH}	Read data hold from inactive read		5	ns
t_{WD}	Write data valid before write active	22		ns
t_{WDH}	Write data hold after write inactive	25		ns
t_{CSA}	Chip selects valid from address valid	5	20	ns
t_{CSC}	Chip selects valid from command active	5	20	ns
t_{IDD}	Propagation delay for IRQ/DRQ/DACK	5	20	ns

Timing Diagrams

Timings for ISA Read/Write Cycle



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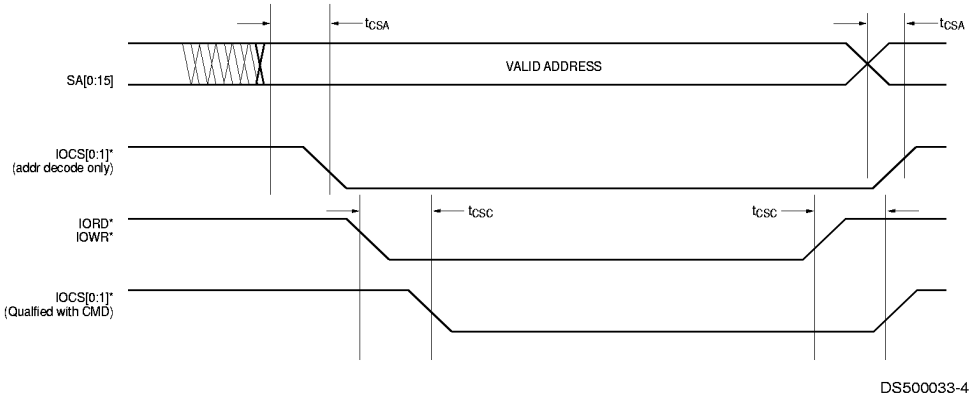
Decode Delay for Chipselect Generation



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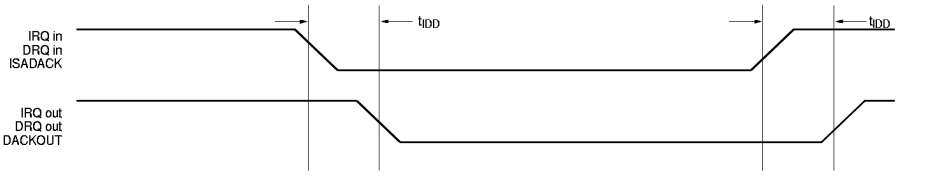
Propagation Delay for IRQ/DRQ/DACK



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INTRODUCTION

NM95MS18 supports both Plug-n-Play platforms (PC with WINDOWS-95 and/or PnP BIOS) as well as Non-Plug-n-Play platforms (PC with WINDOWS-NT, Win3.x/DOS and Non-PnP BIOS). The choice of interface (PnP or Non-PnP) is selected by using a single pin (N_PnP*). Under PnP interface, NM95MS18 is fully compliant with ISA Plug-n-Play specification (Ver 1.0a) and is functionally compatible to its predecessor NM95MS16. Under Non-P 'n' P interface, NM95MS18 powers-up active with a predetermined configuration eliminating any need for an external PnP configuration support. Five external inputs to NM95MS18 allows to choose the default power-up configuration from 31 different predetermined configurations. NM95MS18 integrates 2 kbits of on-board EEPROM to store all the 31 configuration information as well as an additional 2 kbits EEPROM area to store standard PnP resource information. Entire memory can be write protected. NM95MS18 also allows ISA interrupts to be shared.

Functional Description

As mentioned above, NM95MS18 can be configured for either Plug-n-Play environment or Non-Plug-n-Play environment. Under either interface, NM95MS18 provides a choice from 2 operating modes, viz, **DMA Mode** or **Extended Interrupt Mode** offering additional flexibility in selecting a suitable set of features for a particular application. Mode selection is made by setting appropriate bits in the "*I/O DECODE QUALIFICATION*" register in onboard EEPROM. Refer to "*NM95MS18 User's Guide*" for more detail. Each of these modes is explained below.

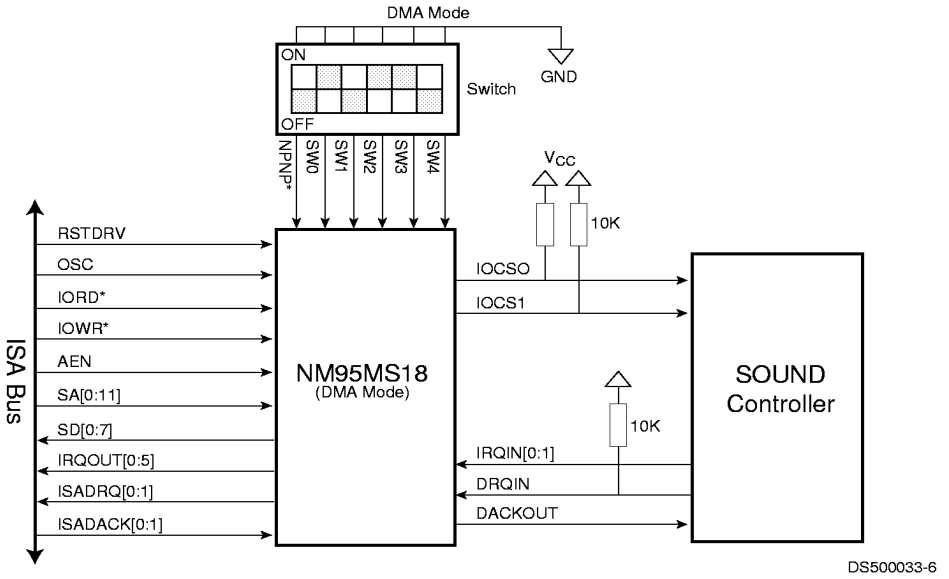
DMA Mode

In the DMA Mode, NM95MS18 provides the following features:

1. Two programmable I/O chipselects (IOCS0*and IOCS1*) each of which can be set to be decoded off of ISA address **SA[0:11]** and **IORD*/IOWR*** or just by **SA[0:11]**. In addition IOCS1* signal can be internally **Wire-ANDed** with IOCS0* signal, to provide "Output Enable" signal for ISA bus data buffers.
2. Two local Interrupt request signals switchable to any six IRQ channels on the ISA Bus. Choice of actual ISA IRQ channels selected is user dependent. Also the type of the six IRQ outputs can be independently set to be either **standard TTL type** or **Open-Drain type**. Selecting Open-Drain type allows interrupts to be shared on the ISA bus.
3. One local DMA request signal switchable to any two DMA channels on the ISA Bus. Choice of actual ISA DMA channels selected is user dependent.

Following figure shows a typical system block diagram of NM95MS18 used in DMA Mode.

DMA Mode



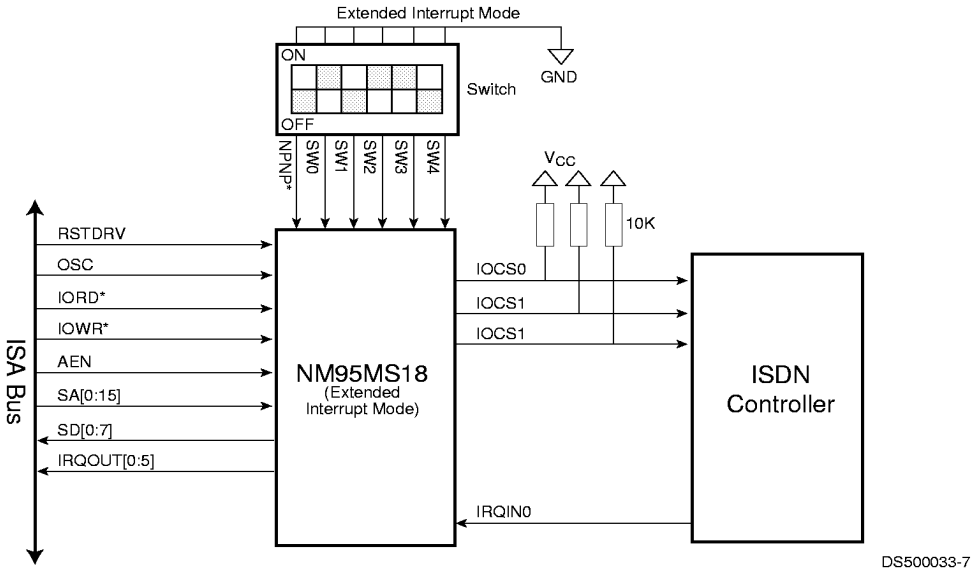
Extended Interrupt Mode (Supports PC-95/PC-97 Requirements)

In Extended Interrupt Mode, NM95MS18 provides these features:

1. Three programmable I/O chipselects (IOCS0*, IOCS1* and IOCS2*) each of which can be set to be decoded off of ISA address **SA[0:11]** and and **IORD*/IOWR*** or by just ISA address bus only. In addition IOCS1* and IOCS2* signals can be internally **Wire-ANDed** with IOCS0* signal, to provide "Output Enable" signal for ISA bus data buffers.
2. One on-board Interrupt request signals switchable to any eight IRQ channels on the ISA Bus. Choice of actual ISA IRQ channels selected is user dependent. Also the type of the eight IRQ outputs can be independently set to be either **standard TTL type** or **Open-Drain type**. Selecting Open-Drain type allows interrupts to be shared on the ISA bus.

Following figure shows a typical system block diagram of NM95MS18 used in Extended Interrupt Mode.

Extended Interrupt Mode (Supports PC-95/PC-97 Requirements)



Interface Options of NM95MS18 Plug-n-Play/Non-Plug-n-Play)

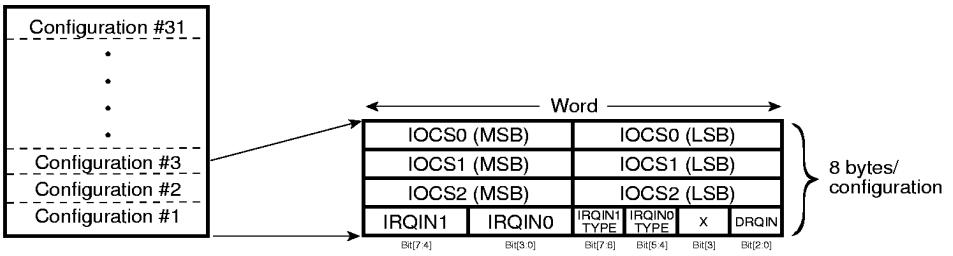
1) Plug-n-Play (PnP) Interface ("/N_PNP" = 1)

In a Plug-n-Play environment, a PnP configuration manager (typically PnP-BIOS, Windows'95 OS or PnP utility) that resides on the PC would read the *Plug-n-Play Resource data* fileand allocate the requested resource (I/O Address space, IRQ etc). PnP configuration is actually a defined process of updating defined PnP Registers on a PnP controller in a defined manner. The entire protocol and Register summary is provided in the ISA PnP Specification (Ver 1.0a). NM95MS18 is designed to be completely compliant with the existing ISA PnP standard and hence provides seamless PnP support for an ISA adapter. All that is required is to prepare the *Plug-n-Play Resource data* for an applicatDuring power-up, NM95MS18 defaults to Plug-n-Play interface if it senses logic "high" at the "N_PNP*" pin. This pin has an internal weak pullup logic and hence can be left unconnected for PnP interface.

2) Non-Plug-n-Play (legacy) Interface ("/N_PNP" = 0)

In a *legacy* interface NM95MS18 is designed to ignore the standard PnP configuration protocol and instead self-configure to a specific configuration. A specific configuration is selected by a set of switch inputs SW[0:4]. All possible combinations of these 5 inputs provide 31 configurations to choose from (the 32nd configuration is reserved for field programming. Refer section on "Software Write Configuration" for more detail). It is also possible to use fewer than five switch inputs (SW[0:3], SW[0:2], SW[0:1] or SW[0] to have fewer legacy configurations (15, 7, 3 or 1 respectively). All these five switch inputs have weak internal pull-up resistor allowing unused switch pins to be left unconnected when necessary.

During power-up, NM95MS18 defaults to Legacy interface if it senses logic "low" at the "N_P 'n' P*" pin. Along with "N_P 'n' P*" pin, the state of "SW[0:4]" inputs are also sensed to determine the particular legacy configuration that needs to be selected. Each legacy configuration occupies 8 bytes (4 Words) of internal memory as shown in the following figure.

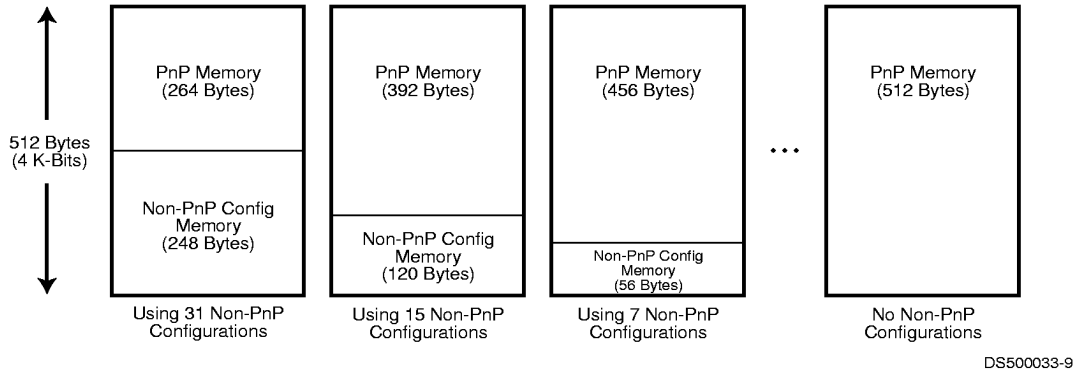


Interface Options of NM95MS18 (Plug-n-Play/Non-Plug-n-Play) (Continued)

Configuration #1 (first configuration) is stored at the bottom 8 bytes (higher address) of the memory and is selected when the SW[0:4] input reflects a "01111" combination. Following table describes all the configuration information with respect to SW[0:4] values and internal memory address.

Configuration Number	/N_PnP Signal	SW[0:4] Combination	Memory Location (Word Address)	Memory Location (Byte Address)
Configuration #1	0	0-1-1-1-1	0xFC - 0xFF	0x1F8 - 0x1FF
Configuration #2	0	1-0-1-1-1	0xF8 - 0xFB	0x1F0 - 0x1F7
Configuration #3	0	0-0-1-1-1	0xF4 - 0xF7	0x1E8 - 0x1EF
Configuration #4	0	1-1-0-1-1	0xF0 - 0xF3	0x1E0 - 0x1E7
Configuration #5	0	0-1-0-1-1	0xEC - 0xEF	0x1D8 - 0x1DF
Configuration #6	0	1-0-0-1-1	0xE8 - 0xEB	0x1D0 - 0x1D7
Configuration #7	0	0-0-0-1-1	0xE4 - 0xE7	0x1C8 - 0x1CF
Configuration #8	0	1-1-1-0-1	0xE0 - 0xE3	0x1C0 - 0x1C7
Configuration #9	0	0-1-1-0-1	0xDC - 0xDF	0x1B8 - 0x1BF
Configuration #10	0	1-0-1-0-1	0xD8 - 0xDB	0x1B0 - 0x1B7
Configuration #11	0	0-0-1-0-1	0xD4 - 0xD7	0x1A8 - 0x1AF
Configuration #12	0	1-1-0-0-1	0xD0 - 0xD3	0x1A0 - 0x1A7
Configuration #13	0	0-1-0-0-1	0xCC - 0xCF	0x198 - 0x19F
Configuration #14	0	1-0-0-0-1	0xC8 - 0xCB	0x190 - 0x197
Configuration #15	0	0-0-0-0-1	0xC4 - 0xC7	0x188 - 0x18F
Configuration #16	0	1-1-1-1-0	0xC0 - 0xC3	0x180 - 0x187
Configuration #17	0	0-1-1-1-0	0xBC - 0xBF	0x178 - 0x17F
Configuration #18	0	1-0-1-1-0	0xB8 - 0xBB	0x170 - 0x177
Configuration #19	0	0-0-1-1-0	0xB4 - 0xB7	0x168 - 0x16F
Configuration #20	0	1-1-0-1-0	0xB0 - 0xB3	0x160 - 0x167
Configuration #21	0	0-1-0-1-0	0xAC - 0xAF	0x158 - 0x15F
Configuration #22	0	1-0-0-1-0	0xA8 - 0xAB	0x150 - 0x157
Configuration #23	0	0-0-0-1-0	0xA4 - 0xA7	0x148 - 0x14F
Configuration #24	0	1-1-1-0-0	0xA0 - 0xA3	0x140 - 0x147
Configuration #25	0	0-1-1-0-0	0x9C - 0x9F	0x138 - 0x13F
Configuration #26	0	1-0-1-0-0	0x98 - 0x9B	0x130 - 0x137
Configuration #27	0	0-0-1-0-0	0x94 - 0x97	0x128 - 0x12F
Configuration #28	0	1-1-0-0-0	0x90 - 0x93	0x120 - 0x127
Configuration #29	0	0-1-0-0-0	0x8C - 0x8F	0x118 - 0x11F
Configuration #30	0	1-0-0-0-0	0x88 - 0x8B	0x110 - 0x117
Configuration #31	0	0-0-0-0-0	0x84 - 0x87	0x108 - 0x10F
Software Write	0	1-1-1-1-1	-	-

Internal EEPROM Memory of NM95MS18



NM95MS18 has a total of 4Kbits (512 Bytes) onboard EEPROM. Of the 512 Bytes, a mimimum of 264 Bytes are allocated for storing *Plug-n-Play Resource data* and the remaining 248 Bytes can be used for storing up to 31 different default power-on Non-PnP configurations (a.k.a. *legacy configurations*). As shown in the above figure, depending on the number of *legacy configurations* supported (can be 31 or 15 or 7 or 3 or 1 or 0), the space for storing *Plug-n-Play Resource data* can be extended to 512 bytes.

SOFTWARE WRITE CONFIGURATION

Under Non-PnP mode when SW[0:4] inputs reflect a 1-1-1-1-1 pattern, NM95MS18 selects a configuration called "Software Write". Primary use of this configuration is to allow field programming of the internal memory. Need for a field programming might arise if the predetermined 31 legacy configurations are exhausted and needs to be updated with a new set of 31 (or less) legacy configurations. Software-Write configuration overrides the general Write-Protection (refer Write-Protection section) offered by NM95MS18, temporarily.

Under this "Software Write" configuration the NM95MS18 expects an "Extended LFSR" key which is nothing but the regular 32 byte writes of LFSR sequence (as defined in the PnP Specification) followed by a 33rd byte write where the value is "0x9C". Once the 33rd write is detected, NM95MS18 will automatically transtition to the "CONFIG" state of PnP mode where programming of internal memory is enabled. In this configuration NM95MS18 selects ISA address "0x203" as the default Read_Data_Port, by default.

WRITE PROTECTION

NM95MS18 offers "Write-Protection" for the entire 4Kbits of internal memory. Protection is enabled by setting bit[15] of the "I/O DECODE QUALIFICATION" register to "0". Setting this bit to "1" disables write-protection. Under "Software Write configuration" this bit is overridden and write-protection is disabled.

PROGRAMMING OF ONCHIP EEPROM

The entire 4Kbit internal EEPROM can be programmed through the ISA bus or through MICROWIRE interface (TEST Mode). Each method is explained below.

PROGRAMMING THROUGH ISA BUS

This method is suited for in-circuit programmin where NM95MS18 is assembled on the ISA board before programming. NM95MS18 is shipped with a "1" pattern at all its bit locations from factory. This means it is shipped with "Write-Protection" disabled. Depending whether the "Write-Protection" is enabled or not there are two procedures to program the onchip memory. Each of these two procedures are explained below.

PROGRAMMING WHEN "WRITE-PROTECTION" IS DISABLED

Follow the procedure defined in ISA Plug-n-Play Specification (Ver. 1.0 a) to place NM95MS18 in "Config" mode of Plug-n-Play protocol. Once the device is is config state, programming of internal EEPROM is enabled. Programming is done by first setting the Address of the location, Data(16bit) to be programmed and then the "Go Ahead" bit to start the programming. A bit in the Status register provides the status of the operation. A programming utility is also available from Fairchild.

Following table summarizes all the registers involved during programming.

Internal EEPROM Memory of NM95MS18 (Continued)

PROGRAMMING INTERFACE

Programming EEPROM Register

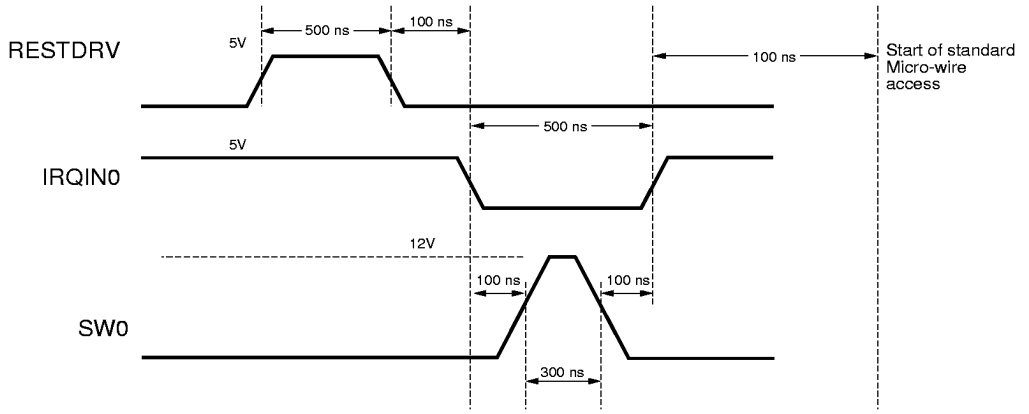
Name	Register	Definition
Status and Command Register	0xF0	Bit[1:0} OP Code bits 10 - Read operation 01 - Write operation 11 - Erase operation Bit [2] - GA (Go Ahead bits) If set to 1, the programming will continue Bit [7:3] - Reserved, should be 0
Address Register	0xF1	Address register [A0 - A7]
Data Register	0xF2	Data Byte [MSB]
Data Register	0xF3	Data Byte [LSB]
STATUS Register	0x05	Bit [0]: STATUS/BUSY bit during programming, '0' is BUSY, '1' is done

PROGRAMMING WHEN "WRITE-PROTECTION" IS ENABLED

In this case, programming is enabled when N_PNP* pin is "0" and the SW[0:4] inputs are "11111". Programming procedure is same as programming when Write-Protection is disabled with the exception of LFSR sequence. In this case 33-Byte Extended-LSFR should be used instead of 32-Byte LFSR.

PROGRAMMING THROUGH MICROWIRE INTERFACE (TEST MODE)

This method is suited when NM95MS18 is pre-programmed before board assembly. This method involves using special TEST mode of NM95MS18. Once the device is in TEST mode, the entire internal memory can be programmed like a standard Micro-wire EEPROM. The protocol to place the device in "test-mode" makes use of the following three signals, viz. RESETDRV, IRQIN0 and SW0. The timing diagram is shown below.



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Note: All timings shown here are minimum values.

Internal EEPROM Memory of NM95MS18 (Continued)

Details of timing information for Microwire protocol can be obtained from Fairchild's Microwire EEPROM Datasheets. Please refer NM93C66 datasheet. This datasheet can be downloaded from Fairchild's home page on World-Wide-Web. (http://www.fairchildsemi.com)

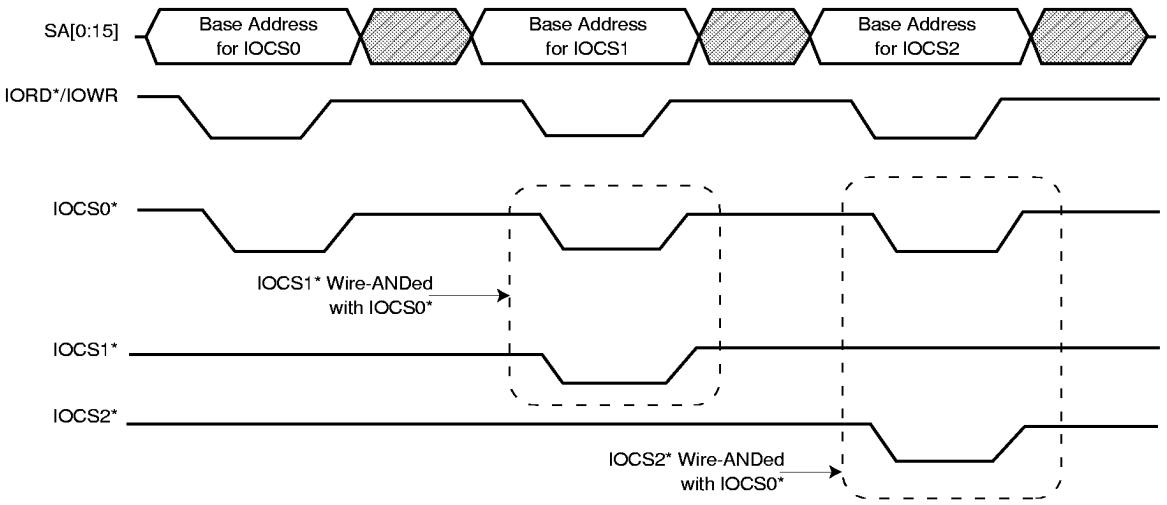
SHARING OF INTERRUPTS

Interrupt output (IRQOUTx) signals from NM95MS18 can be configured as either standard TTL type or Open-Drain type. Interrupt outputs configured as Open-Drain type can share an interrupt on the ISA bus. Sharing of interrupt increases ISA bus resource allocation probabilities and also allows presence of multiple cards of the same type. Each IRQOUTx signal can be individually set for either Interrupt type and this is done by setting appropriate bits in EEPROM register. Refer the USER'S GUIDE for more detail.

Wire-ANDing of I/O Chipselects

The IOCS1* and IOCS2* signals can be internally Wire-ANDed with IOCS0* signal on NM95MS18. When this feature is enabled, IOCS0* signal can also act as "Output Enable" signal for ISA bus data buffers eliminating extra glue logic on the board. Setting appropriate bits in EEPROM register enables this feature. Refer the USER'S GUIDE for more detail. Following diagram illustrates this feature.

WIRE-ANDing of I/O Chipselects



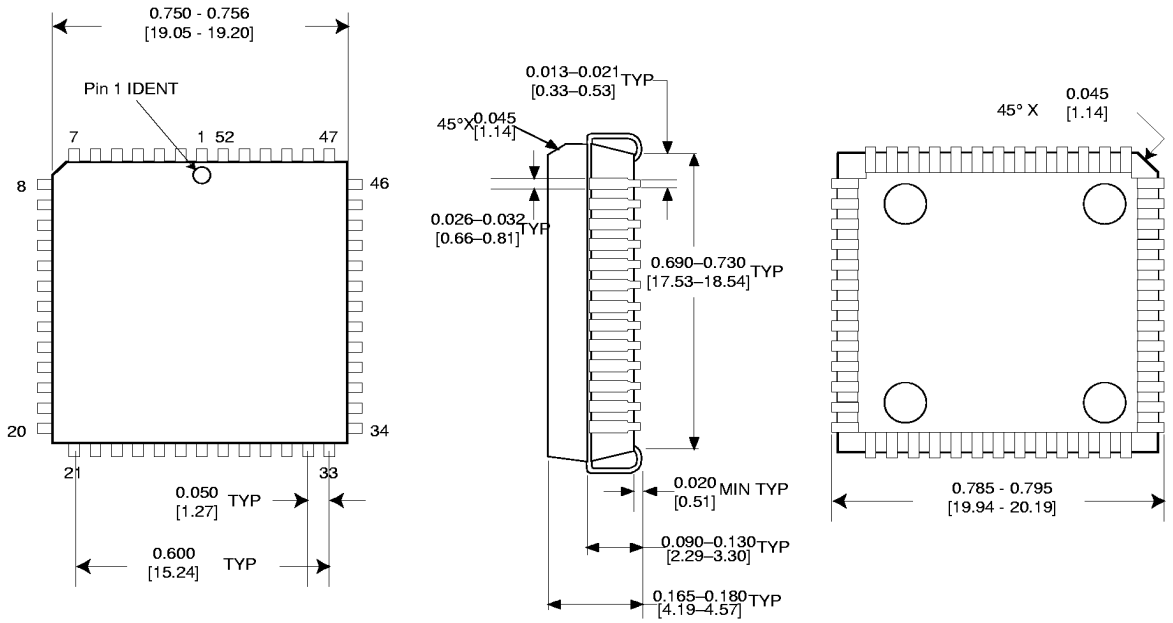
DS500033-11

Note 1: This illustratory waveform assumes that both IOCS1* and IOCS2* are set to be Wire-ANDed with IOCS0*. They can also be set individually.

Note 2: In this waveform, IOCSx* are set to be decoded off of address and IORD*/IOWR.

Note 3: Refer "I/O DECODE QUALIFICATION REGISTER" description for more information.

Physical Dimensions inches (millimeters) unless otherwise noted



52 Lead Molded Plastic Leaded Chip Carrier
Package Number V52A

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
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