National Semiconductor

NMC27CP128
131,072-Bit (16k x 8) UV Erasable CMOS PROM

General Description

The NMC27CP128 is a high-speed 128k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27CP128 is designed to operate with a single +5V power supply with ±10% tolerance.

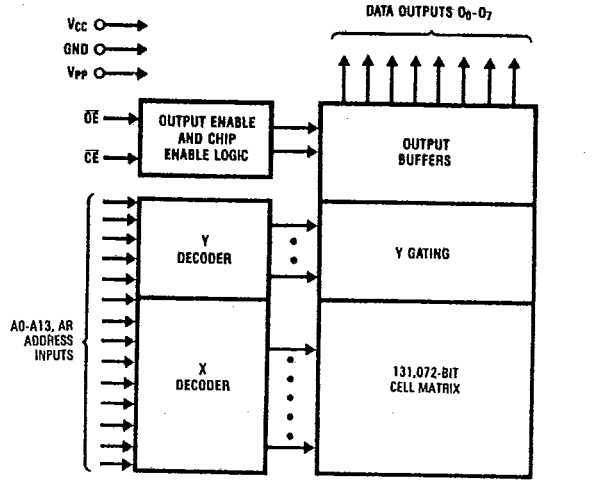
The NMC27CP128 is packaged in a 28-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Clocked sense amps for fast access time down to 200 ns
- Low CMOS power consumption
  - — Active power: 55 mW max
  - — Standby power: 0.55 mW max
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Fast and reliable programming
- Static operation—no clocks required
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Optimum EPROM for total CMOS systems

Block Diagram



TL/D/8805–1

Pin Names

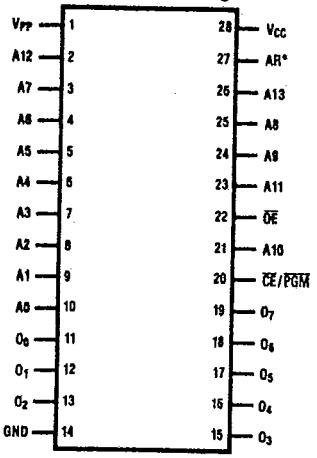
A0–A13	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect
AR	Block Select

Connection Diagram

T-46-13-29

27C512 27512	27C256 27256	27C64 2764	27C32 2732	27C16 2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

NMC27CP128Q
Dual-In-Line Package



TL/D/8805–2

27C16 2716	27C32 2732	27C64 2764	27C256 27256	27C512 27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

*AR held at V_{IH}

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27CP128 pins.

Order Number NMC27CP128Q
See NS Package Number J28AQ

Commercial Temp Range
(0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27CP128Q200	200
NMC27CP128Q250	250
NMC27CP128Q300	300

1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
All Input Voltages with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND−0.6V
V_{CC} Supply with Respect to Ground	+7.0V to −0.6V
V_{PP} Supply Voltage with Respect to Ground During Programming	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 7)

Temperature Range NMC27CP128Q200, 250, 300	0°C to +70°C
V_{CC} Power Supply	5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{PP}	V_{PP} Current	$V_{PP} = V_{CC}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE}/\overline{PGM} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}/\overline{PGM}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE}/\overline{PGM} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE}/\overline{PGM} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27CP128Q						Units
			200		250		300		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE}/\overline{PGM} = \overline{OE} = V_{IL}$		200		250		300	ns
t_{CE}	$\overline{CE}/\overline{PGM}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE}/\overline{PGM} = V_{IL}$		75		100		120	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE}/\overline{PGM} = V_{IL}$	0	60	0	60	0	105	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	60	0	60	0	105	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}/\overline{PGM}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE}/\overline{PGM} = \overline{OE} = V_{IL}$	0		0		0		ns

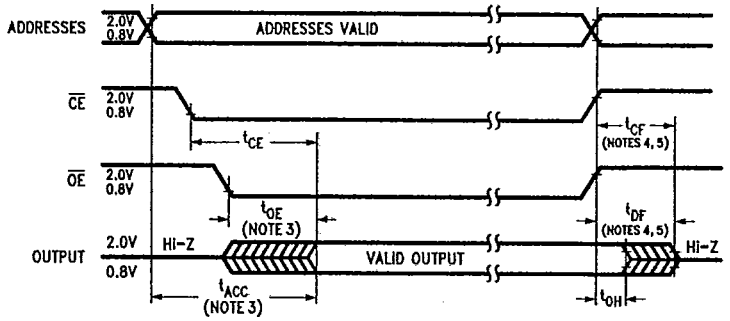
Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7 & 9)



TL/D/8805–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = −400 μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 11: AR held at V_{IH}.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.45	0.5	0.55	ms
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

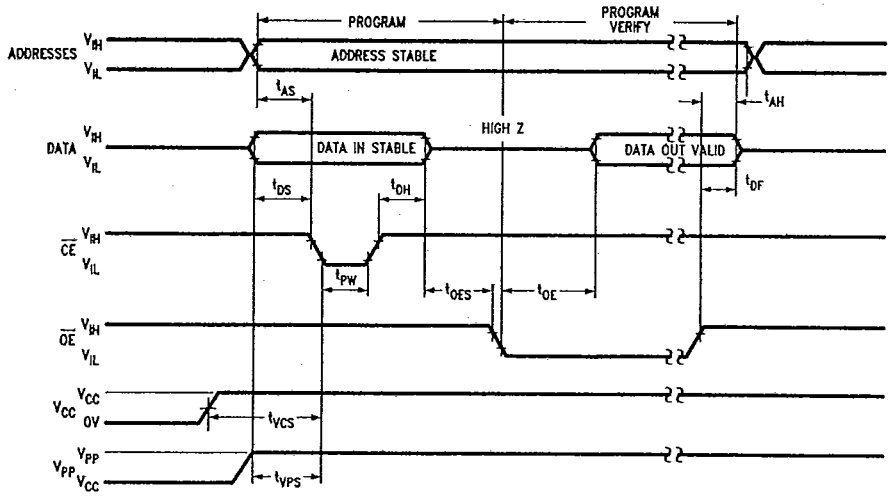
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

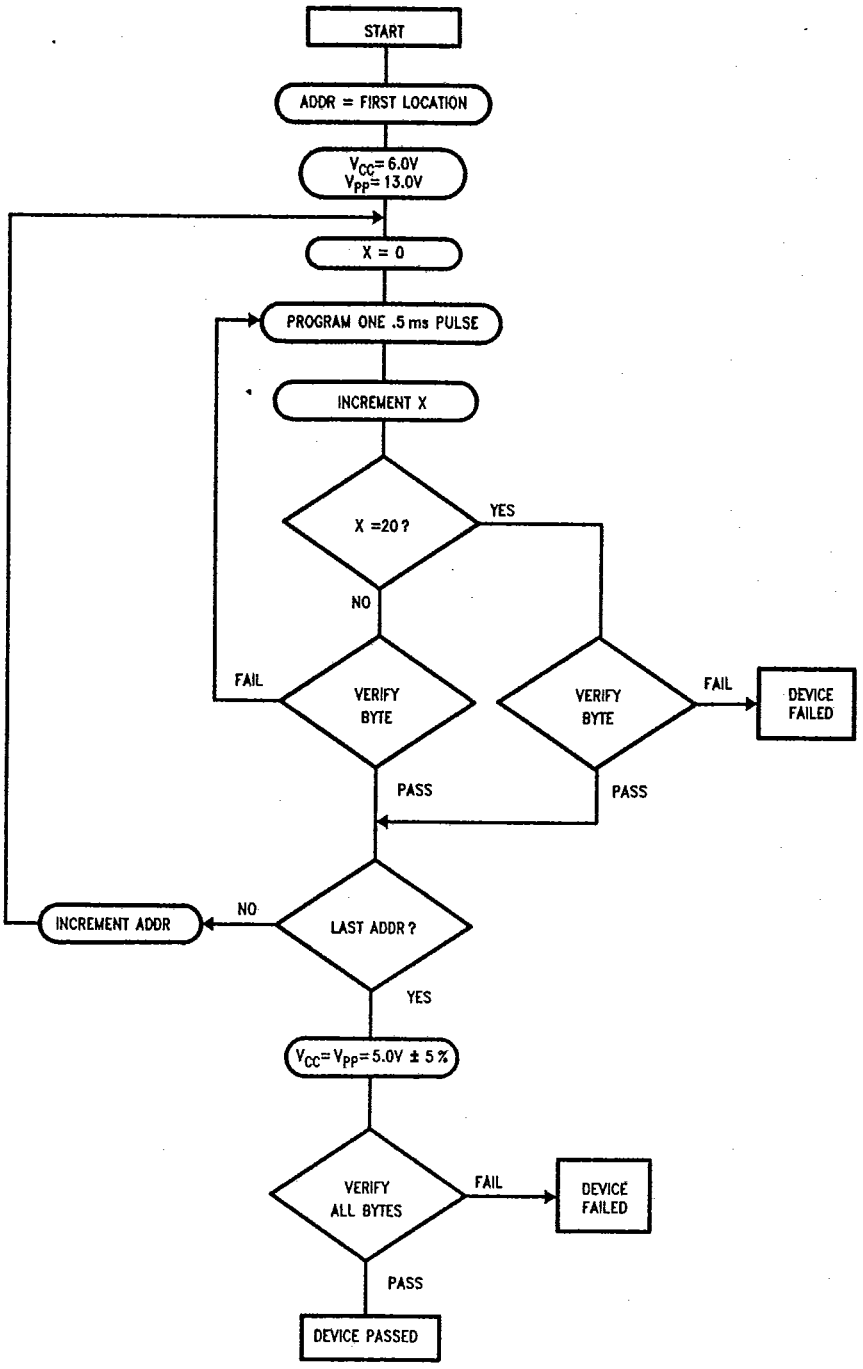
Note 4: Programming and program verify are tested with the Interactive Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Programming Waveforms (Note 3)



TL/D/8805-4

Interactive Programming Algorithm Flow Chart



TL/D/8805–5

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27CP128 are listed in Table I. It should be noted that all inputs for the six modes may be at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27CP128 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}/\overline{PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}/\overline{PGM}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}/\overline{PGM}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27CP128 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27CP128 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}/\overline{PGM}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27CP128s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}/\overline{PGM}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27CP128.

Initially, and after each erasure, all bits of the NMC27CP128 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27CP128 is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs may be TTL.

When the address and data are stable, an active low TTL program pulse is applied to the $\overline{CE}/\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. Any location may be programmed at any time—either individually, sequentially, or at random. The NMC27CP128 is designed to be programmed with interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). Since the NMC27CP128 employs the last 131,072 bits of a 262,144 bit memory array, programming must be started at address 16,384 to provide correct data read. The NMC27CP128 must not be programmed with a DC signal applied to the $\overline{CE}/\overline{PGM}$ input.

Programming multiple NMC27CP128s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27CP128s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}/\overline{PGM}$ input programs the paralleled NMC27CP128s.

The NMC27CP128 is a partial NMC27C256 and therefore is not program compatible with most 128k EPROMs.

The Manufacturer's Identification Code should not be used for programming control of the NMC27CP128.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	5V	Hi-Z
Program	Pulsed V_{IH} to V_{IL}	V_{IH}	13.0V	6V	D_{IN}
Program Verify	V_{IH}	V_{IL}	13.0V	6V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	13.0V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	5V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27CP128s in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$ all like inputs (including $\overline{OE}$) of the parallel NMC27CP128 may be common. A low level $\overline{CE}/\overline{PGM}$ input selects the devices to be programmed. A high level $\overline{CE}/\overline{PGM}$ input inhibits the other devices from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27CP128 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming, opaque labels should be placed over the NMC27CP128's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27CP128 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27CP128 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table II shows the minimum NMC27CP128 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Minimum NMC27CP128 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50