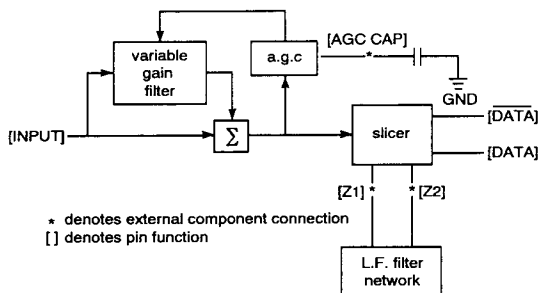




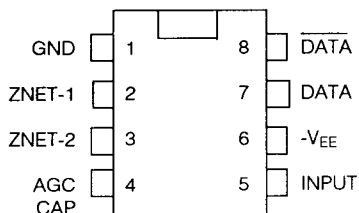
FEATURES

- automatic equalization up to 350 metres of 8281 cable at 143 MB/s data rates.
- 8 pin PDIP packaging
- single -5 volt power supply operation

FUNCTIONAL BLOCK DIAGRAM



PIN OUTS



DEVICE DESCRIPTION

The Gennum *GENLINX* GS9006A is a monolithic automatic cable equalizer developed for scrambled NRZI Serial Digital Video signals. It is fabricated on Gennum's proprietary LSI process and is suitable for 143 MB/s and 177 MB/s D2 signals.

The GS9006A accepts scrambled SMPTE/EBU Serial Digital Video signals and is driven as unbalanced using a 75Ω termination resistor. The DATA and DATA outputs typically deliver 750 mV p-p equalized signals into 220 ohm loads. These signals can be used to feed cable driver circuits for Serial Distribution Amplifier applications.

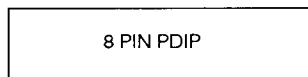
Packaging is 8 pin PDIP with the pin outs as shown below. Operating with a single -5 volts supply, the GS9006A typically draws 23 mA of current.

The circuitry of the GS9006A is protected by Patents Pending.

APPLICATIONS

- Front-end cable equalization for D2 serial digital routers.
- Input equalization for serial digital DAs.

AVAILABLE PACKAGING



ORDERING INFORMATION

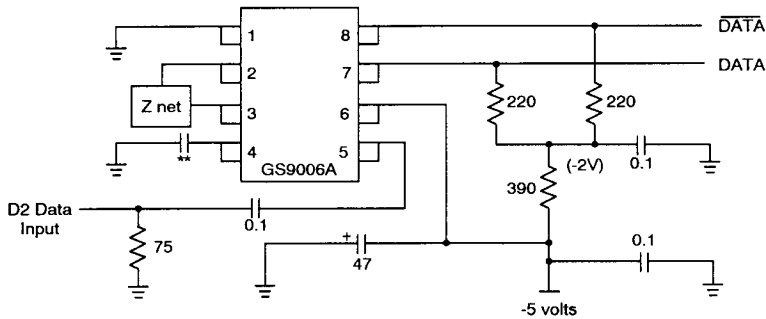
Part Number	Package	Temperature
GS9006ACDA	8 pin PDIP	0°C to 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, $V_s = -5V$, $T_A = 0$ to $70^\circ C$, $R_L = 220\Omega$

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
D.C.	Supply Voltage	V_{EE}	$T_A = 25^\circ C$	-4.5	-5.0	-5.5	volts
	Supply Current	I	$T_A = 25^\circ C$	-	23	-	mA
A.C.	Gain Lift relative to 10 MHz		$T_A = 25^\circ C$ $f = 70 \text{ MHz}$	22	-	-	dB
	Input Signal Level	V_{SIG-in}	$R_{IN} = 75\Omega$	720	-	880	mV p-p
	Output Signal Level	$V_{SIG-out}$	$R_{OUT} = 220\Omega$	-	750	-	mV p-p
	Input Resistance	R_{IN}		3K	-	-	Ω
	Input Capacitance	C_{IN}		-	1.0	-	pF

TEST CIRCUIT



unless otherwise shown, all resistors are in ohms, all capacitors in uF.

Figure 2

NOTES: The block marked [Znet] is a series R-C network used to control the amount of Low Frequency (DC component) rejection. In scrambled NZRI data, there should be no net DC component.

As a starting point, R can be 470 Ω and C can be 4.7 pF. The optimal values may be determined by observing the 'eye pattern' of the output data.

If no LF rejection is needed pins 2 and 3 may be directly connected together.

** The value of the AGC capacitor is also determined experimentally. It should fall between 0.1uF and 10 uF.

The circuit diagram shows a differential signal shaper. A differential input signal, labeled "D2 DATA IN", is connected to pins 1 and 2 of the GS9006A. The output of the GS9006A is connected to pins 3 and 4. The output of the GS9006A is connected to the bases of two BFR-96 transistors. The emitters of the transistors are connected to a common emitter resistor of 68 ohms, which is connected to ground. The collectors of the transistors are connected to a common collector resistor of 75 ohms, which is connected to ground. The output of the circuit is labeled "D2 DATA (75Ω) OUT". A note at the bottom states: "unless otherwise shown, all resistors are in ohms, all capacitors in uF."

Figure 3.

Due to the high bit rates of the signals involved, care should be taken to assure minimum track lengths and the liberal use of ground plane around the device. Figure 3 shows one application of the GS9006A used as a non-reclocking serial distribution amplifier.

The output stages of the GS9006A are designed for a minimum load resistance of 220 Ω . Reducing this load resistance or increasing the supply voltage in order to boost the output signal swing will cause damage to the output stages.

Figures 4, 5 and 6 show the input serial data 'eye pattern' after 100, 200 and 300 metres of belden 8281 cable. In each case, the corresponding equalized output 'eye pattern' is also shown.

Figures 7 through 9 show typical 143 MB/s input and output data waveforms for similar lengths of cable. Even though there is some signal jitter evident in the output signal (approximately ± 1 ns), this would not show up as a problem in a system if the equalized data is reclocked.

For non-reclocking applications, this jitter will limit the usefulness of the GS9006A to a single pass through of data.

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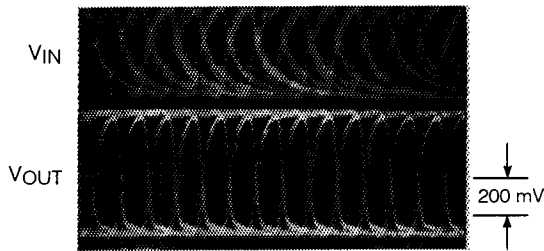


Fig. 4
(100 metres)

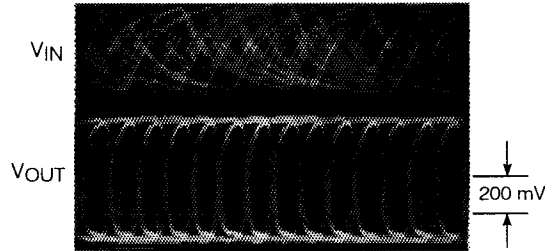


Fig. 5
(200 metres)

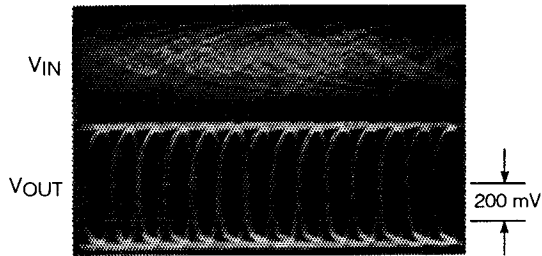


Fig. 6
(300 metres)

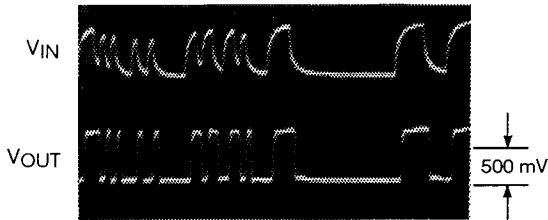


Fig. 7
(100 metres)

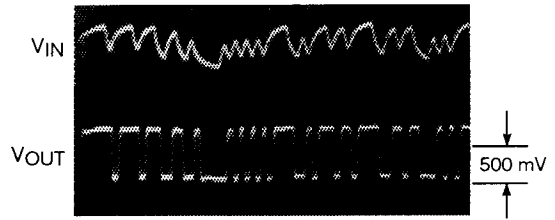


Fig. 8
(200 metres)

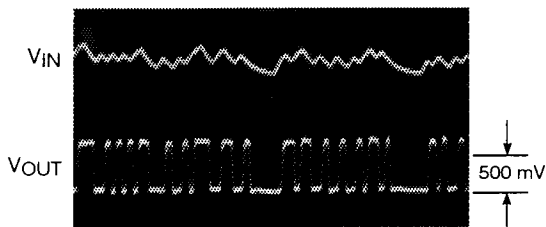
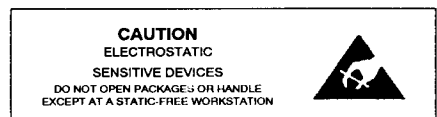


Fig. 9
(300 metres)



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