T-46-13-27

National Semiconductor

NMC93CS06x3/CS46x3/CS56x3/CS66x3 Extended Voltage 256-/1024-/2048-/4096-Bit Serial EEPROM with Protect Register

General Description

The NMC93CS family of extended operating voltage serial EEPROM are 256/1024/2048/4096 bits of read/write memory divided into 16/64/128/256 registers of 16 bits each. N registers (N≤16, N≤64, N≤128, N≤256) can be protected against data modification by programming a special on-chip register called the Protect Register with the address of the first register to be protected against data modification. Additionally, this address can be "locked" into the device, making all future attempts to change data impossible.

These memories feature a serial interface with the instruction, address, and write data input on the Data-In pin. All data-out, and device status are available on the Data-Out pin. A low to high transition of Serial Data Clock (SK) shifts all data in or out of the memory. This serial interface is MICROWIRE™ compatible providing simple interfacing to standard microcontrollers and microprocessors. There are a total of 10 instructions, 5 which operate on the EEPROM memory, and 5 which operate on the Protect Register. The memory instructions are READ, WRITE, WRITE ALL,* WRITE ENABLE, and WRITE DISABLE. To perform any of the memory instructions, the input PRE must be low. The instructions to the Protect Register are similar, except the input PRE must be high. The Protect register instructions are PRREAD, PRWRITE, PREN, PRCLEAR, and PRDS.

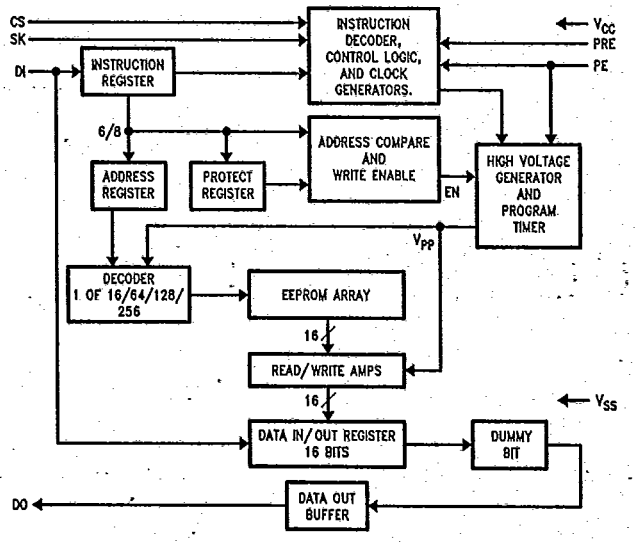
These memories feature a unique EEPROM memory cell which does not require erasing prior to writing, therefore reduces the total number of programming cycles, thus increasing the endurance of the device in actual application. These EEPROM memories are designed for applications requiring 40 years data retention and 100,000 data changes per bit. They are ideal for battery operated applications due to the wide operating voltage range. They are fully functional in all modes of operation across a guaranteed range of 3.0V–5.5V.

*The WRITE ALL instruction is only functional from 4.5V to 5.5V V_{CC}. Its primary purpose is as a test mode.

Features

- 3.0V to 5.5V guaranteed operating range
- Typical active current 400 μA; typical standby current 25 μA
- Write protection in a user defined section of memory
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self timed write cycle
- Device status during write mode
- 40 year data retention
- 100,000 data changes per bit

Block Diagram



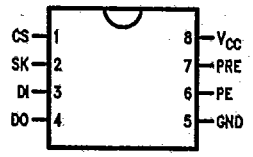
TL/D/10044–1

Connection Diagrams

T-46-13-27

PIN OUT:

Dual-In-Line Package (N)



TL/D/10044–2

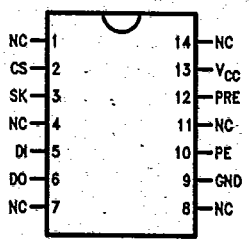
Top View

See NS Package Number N08E

Pin Names	
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

PIN OUT:

SO Package (M)



TL/D/10044–3

Top View

See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NMC93CS06N3/ NMC93CS46N3/NMC93CS56N3/NMC93CS66N3 NMC93CS06M3/ NMC93CS46M3/NMC93CS56M3/NMC93CS66M3

Extended Temp. Range (−40°C to +85°C)

Order Number
NMC93CS06EN3/ NMC93CS46EN3/NMC93CS56EN3/NMC93CS66EN3 NMC93CS06EM3/ NMC93CS46EM3/NMC93CS56EM3/NMC93CS66EM3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC93CSxx	0°C to +70°C
NMC93CSxxE	−40°C to +85°C
Positive Power Supply	3.0V to 5.5V

T-46-13-27

DC and AC Electrical Characteristics V_{CC} = 3.0V to 5.5V unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
V_{RPP}	Power Supply Ripple		Peak-to-Peak (Note 7)		0.1 V_{CC}	V
I_{CC1}	Operating Current CMOS Input Levels	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	CS = V_{IH}, SK = 1.0 MHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CSS66E	CS = V_{IH}, SK = 1.0 MHz 4.5V≤V_{CC}≤5.5V		3 3	mA
I_{CC3}	Standby Current	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	CS = 0V		50 100	μA
I_{IL}	Input Leakage	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CSS66E	V_{OUT} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage		4.5V≤V_{CC}≤5.5V	 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage		3V≤V_{CC}≤4.5V	−0.1 2	0.6 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		4.5V≤V_{CC}≤5.5V I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		3V≤V_{CC}≤4.5V I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E		0 0	1 0.5	MHz
t_{SKH}	SK High Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	(Note 2) (Note 3)	500 500		ns
t_{SKL}	SK Low Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	(Note 2) (Note 3)	250 500		ns
t_{CS}	Minimum CS Low Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	(Note 4) (Note 5)	250 500		ns
t_{CSS}	CS Setup Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	Relative to SK	50 100		ns
t_{PRES}	PRE Setup Time	NMC93CS06-NMC93CS66 NMC93CS06E-NMC93CS66E	Relative to SK	50 100		ns
t_{PES}	PE Setup Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	Relative to SK	50 100		ns
t_{DIS}	DI Setup Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	Relative to SK	100 200		ns

DC and AC Electrical Characteristics V_{CC} = 3.0V to 5.5V unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{PEH}	PE Hold Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	Relative to CS Relative to CS	250 500		ns
t_{PREH}	PRE Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	Relative to SK	100 200		ns
t_{PD1}	Output Delay to "1"	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	AC Test		500 1000	ns
t_{PD0}	Output Delay to "0"	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	AC Test		500 1000	ns
t_{SV}	CS to Status Valid	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	AC Test		500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC93CS06–NMC93CS66 NMC93CS06E–NMC93CS66E	CS = V_{IL} AC Test		100 200	ns
t_{WP}	Write Cycle Time				15	ms
	Endurance		Number of Data Changes per Bit	Typical 100,000		Cycles

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 microsecond, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1 microsecond. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature parts specifies a minimum SK clock period of 2 microseconds, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 microseconds. For example, if t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 microseconds in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Note 7: Rate of voltage change must be less than 0.5 V/ms.

Capacitance (Note 6)

T_A = 25°C, f = 1MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Functional Description

T-46-13-27

The NMC93CSxx family of extended voltage EEPROM have 10 instructions as described below. Note that there is a difference in the length of the instruction for the NMC93CS06 and NMC93CS46 vs. the NMC93CS56 and NMC93CS66. This is due to the fact that the two larger devices require 2 additional address bits which are not required for the smaller devices. Within the two groups of devices the number of address bits remain constant even though in some cases the most significant bit(s) are not used. In every instruction, the first bit is always a "1" and is viewed as a start bit. The next 8 or 10 bits (depending on device size) carry the op code and address. The address is either 6 or 8 bits depending on the device size.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the NONVOLATILE SHIFT-REGISTER mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Write All (WRALL):

The Write All (WRALL) instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. Additionally, it is only guaranteed at V_{CC} = 5.0V ±10%. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}).

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Protect Register Read (PRREAD):

The Protect Register Read (PRREAD) instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction. Following the PRREAD instruction the 6- or 8-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6- or 8-bit address string.

Protect Register Enable (PREN):

The Protect Register Enable (PREN) instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The Protect Register Clear (PRCLEAR) instruction clears the address stored in the Protect Register and, therefore, enables all registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Protect Register Write (PRWRITE):

The Protect Register Write (PRWRITE) instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become 'don't care'. Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

Protect Register Disable (PRDS):

The Protect Register Disable (PRDS) instruction is a **one** time only instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

Instruction Set for the NMC93CS06x3 and NMC93CS46x3

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared. Valid only at V_{CC} = 4.5V to 5.5V.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE.
PRWRITE	1	01	A5–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

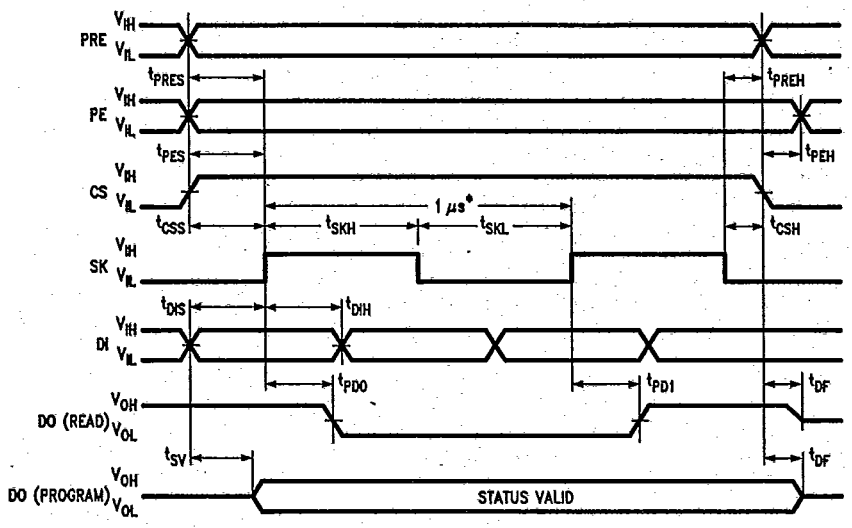
Instruction Set for the NMC93CS56x3 and NMC93CS66x3

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A7–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared. Valid only at V_{CC} = 4.5V to 5.5V.
WDS	1	00	00XXXXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A7–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

Timing Diagrams

T-46-13-27

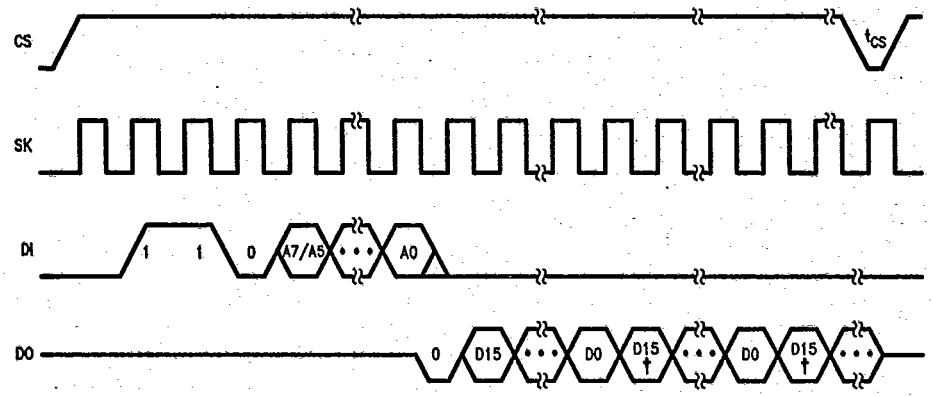
Synchronous Data Timing



TL/D/10044–4

*This is the minimum SK period (See Note 2).

READ:
PRE = 0, PE = X



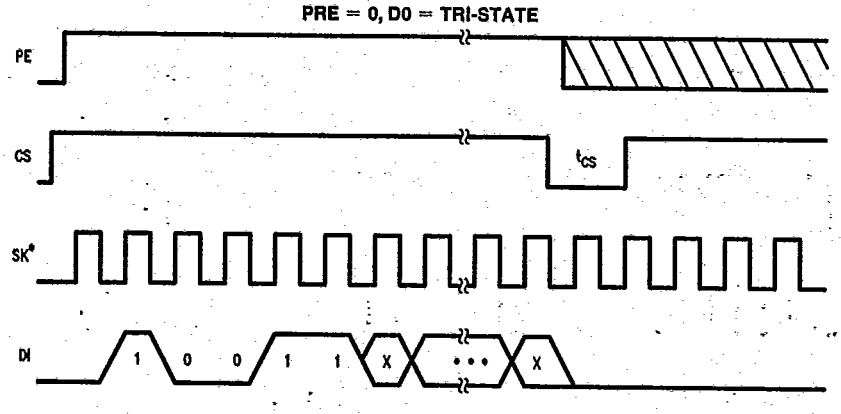
TL/D/10044–5

*Address bit A7 becomes "don't care" for NMC93CS56
*Address bits A5 and A4 become "don't cares" for NMC93CS06
†The memory automatically cycles to the next register.

Timing Diagrams (Continued)

T-46-13-27

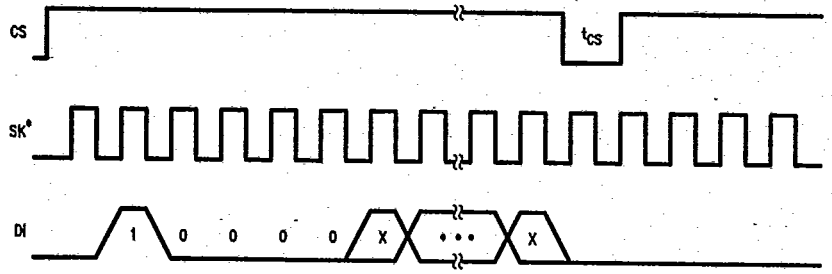
WEN:
PRE = 0, DO = TRI-STATE



TL/D/10044–6

*The NMC93CS56 and NMC93CS66 require a minimum of 11 clocks. The NMC93CS06 and NMC93CS46 require a minimum of 9 clock cycles.

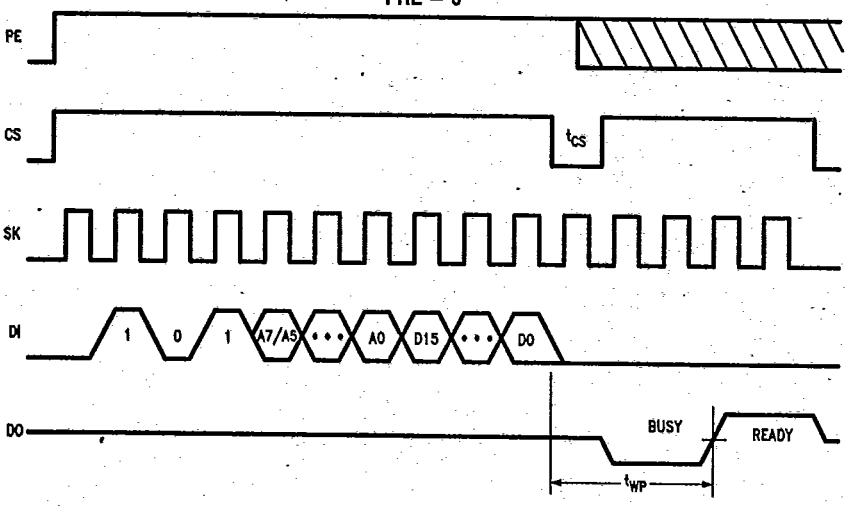
WDS:
PRE = 0, PE = X, DO = TRI-STATE



TL/D/10044–7

*The NMC93CS56 and NMC93CS66 require a minimum of 11 clocks. The NMC93CS06 and NMC93CS46 require a minimum of 9 clock cycles.

WRITE:
PRE = 0



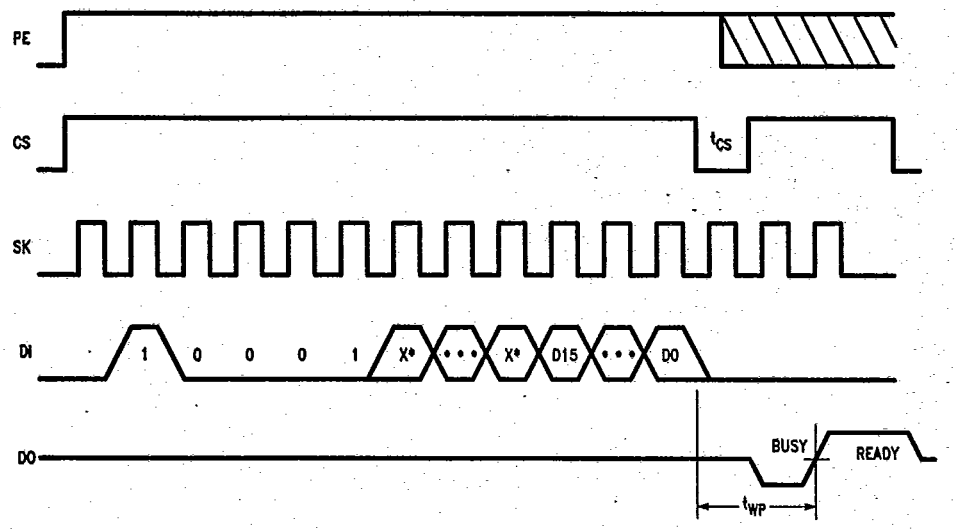
TL/D/10044–8

• Address bit A7 becomes a "don't care" for NMC93CS56
• Address bits A5 and A4 become "don't cares" for NMC93CS06

Timing Diagrams (Continued)

T-46-13-27

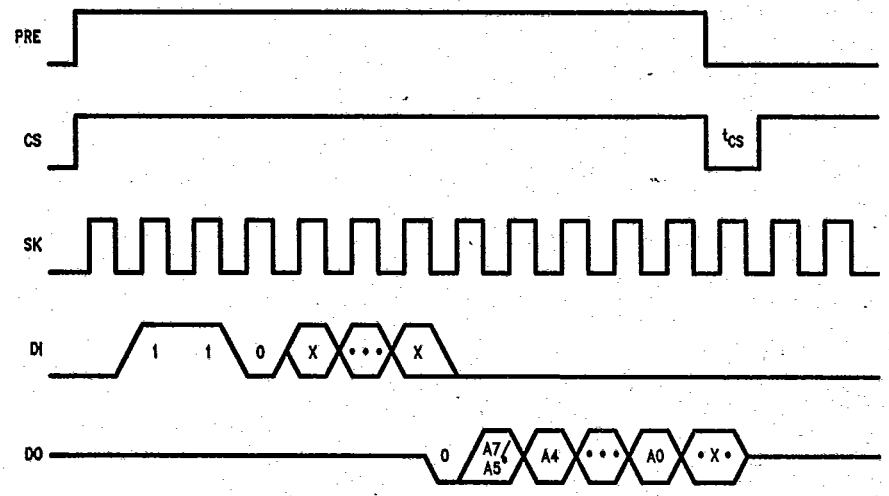
WRALL†:
PRE = 0



*Don't care
†Protect Register **MUST** be cleared.
†Valid only at V_{CC} = 4.5V to 5.5V.

TL/D/10044-9

PRREAD:
PE = X



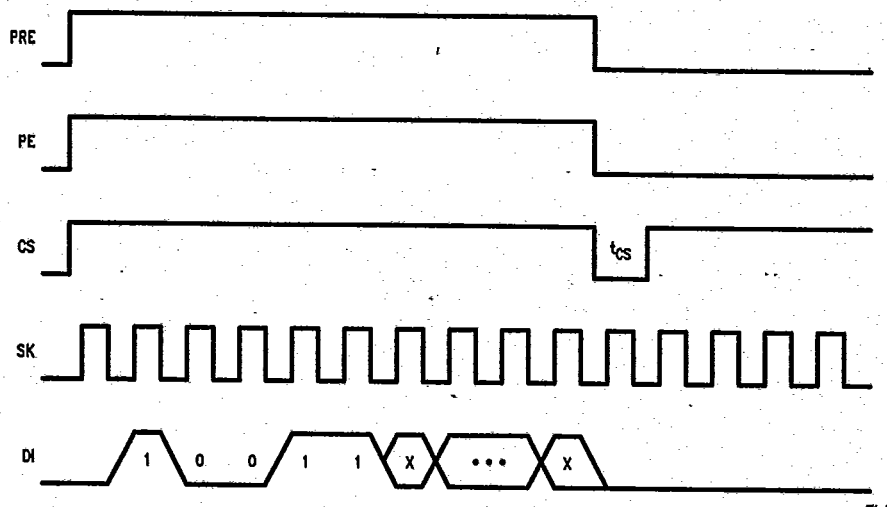
•Address bits A5 and A4 become "don't cares" for NMC93CS06
•Address bit A7 becomes "don't care" for NMC93CS56

TL/D/10044-10

Timing Diagrams (Continued)

T-46-13-27

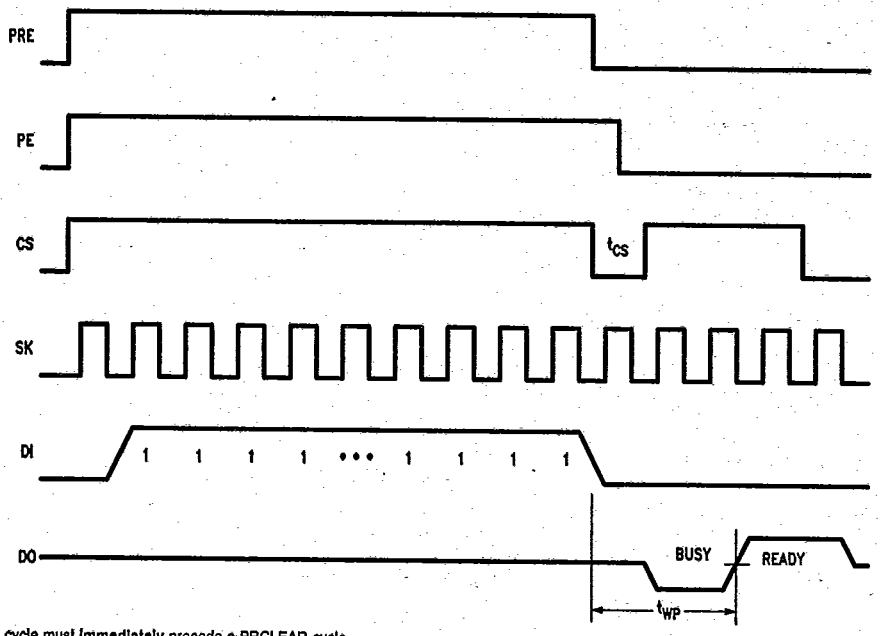
PREN*:
DO = TRI-STATE



TL/D/10044–11

*A WEN cycle must precede a PREN cycle.

PRCLEAR*:



*A PREN cycle must immediately precede a PRCLEAR cycle.

TL/D/10044–12

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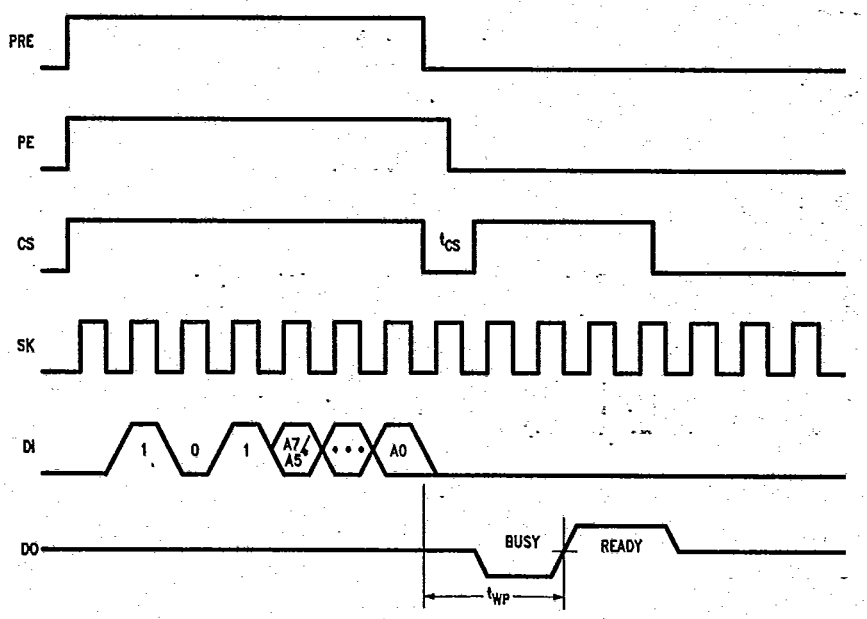
Timing Diagrams (Continued)

T-46-13-27

PRWRITE†:

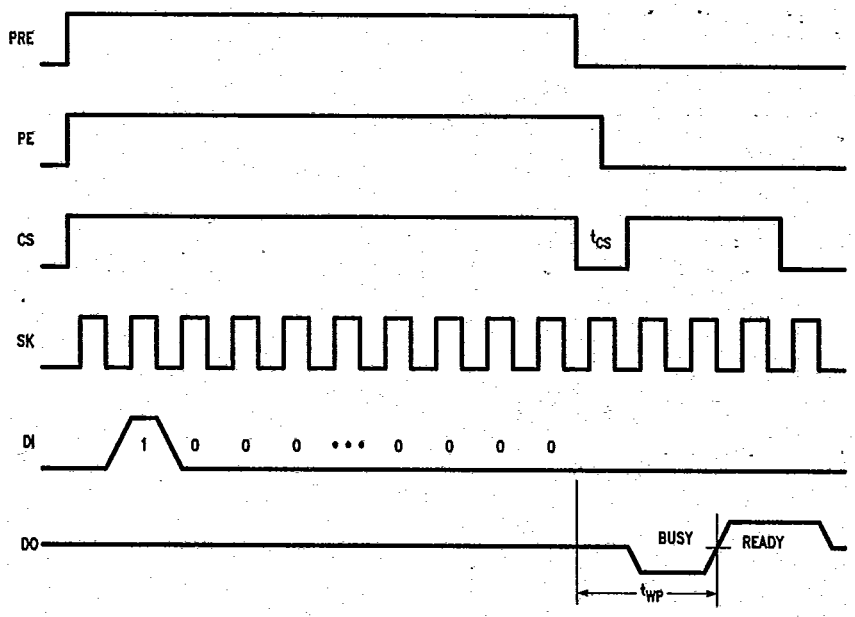


TL/D/10044–13

*Address bit A7 becomes a "don't care" for NMC93CS56
*Address bits A5 and A4 become "don't cares" for NMC93CS06

†Protect Register MUST be cleared before a PRWRITE cycle. A PREN cycle must immediately precede a PRWRITE cycle.

PRDS*:



TL/D/10044–14

*ONE TIME ONLY instruction. A PREN cycle must immediately precede a PRDS cycle.

National Semiconductor

PRELIMINARY

T-46-13-27

NMC93C06x3/C46x3/C56x3/C66x3 Extended Voltage 256-/1024/2048/4096-Bit Serial EEPROM

General Description

The NMC93C06x3/C46x3/C56x3/C66x3 are 256/1024/2048/4096 bits of CMOS electrically erasable memory divided into 16/64/128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high speed and low power. They operate from a single 3.0V to 5.5V supply since V_{PP} is generated on-board. The serial organization allow the NMC93C06x3/C46x3/C56x3/C66x3 to be packaged in an 8-pin DIP or 14-pin SO package to save board space.

The memories feature a serial interface with the instruction, address, and write data, input on the Data-In (DI) pin. All read data and device status come out on the Data-Out (DO) pin. A low-to-high transition of shift clock (SK) shifts all data in and out. This serial interface is MICROWIRE™ compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions: Read, Erase/Write Enable, Erase, Erase All*, Write, Write All*, and Erase/Write Disable. The NMC93C06x3/C46x3/C56x3/C66x3 do not require an erase cycle prior to the Write and Write All instructions. The Erase and Erase All instructions are available to maintain complete read and programming capability with the NMOS NMC9346. All programming cycles are completely self-timed for simplified operation. The busy status is available on the DO pin to indicate the completion of a programming cycle. EEPROMs are shipped in the erased state where all bits are logical 1's.

Compatibility with Other Devices

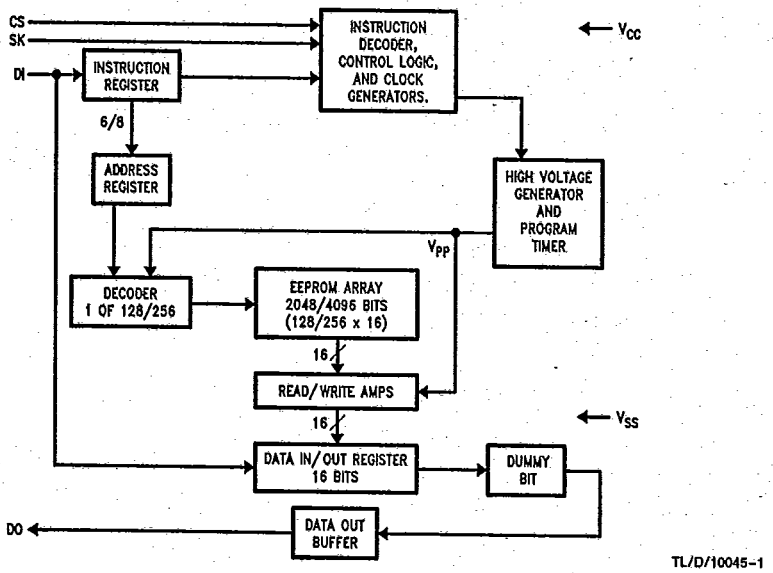
These memories are pin compatible to National Semiconductor's NMOS EEPROMs, NMC9306 and NMC9346 and CMOS EEPROMs NMC93C06x3/C46x3/C56x3/C66x3.

Features

- Typical active current 400 μA; Typical standby current 25 μA
- Reliable CMOS floating gate technology
- 3.0V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status signal during programming mode
- Sequential register read
- 40 years data retention
- 100,000 write cycles

*The Instructions Erase All and Write All are functional only from V_{CC} = 4.5V to 5.5V. Their primary purpose is as test modes.

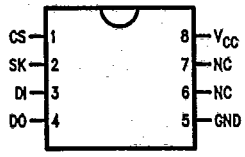
Block Diagram



TL/D/10045-1

Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



TL/D/10045-2

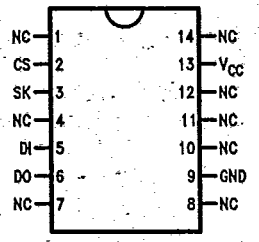
Top View

See NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

14-Pin SO Package (M)



TL/D/10045-3

Top View

See NS Package Number M14A

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NMC93C06N3
NMC93C46N3/NMC93C56N3/NMC93C66N3
NMC93C46M3/NMC93C56M3/NMC93C66M3
NMC93C06M83/NMC93C46M83

Extended Temp. Range (−40°C to +85°C)

Order Number
NMC93C06EN3
NMC93C46EN3/NMC93C56EN3/NMC93C66EN3
NMC93C46EM3/NMC93C56EM3/NMC93C66EM3
NMC93C06EM83/NMC93C46EM83

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC93C56–NMC93C66	0°C to +10°C
NMC93C56E–NMC93C66E	−40°C to +85°C
Positive Power Supply	3.0V to 5.5V

T-46-13-27

DC and AC Electrical Characteristics V_{CC} = 3.0V to 5.5V (unless otherwise specified)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	CS = V_{IH}, SK = 0.5 MHz		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	CS = V_{IH}, SK = 0.5 MHz		3 3	mA
I_{CC3}	Standby Current	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	CS = 0V		50 100	μA
I_{IL}	Input Leakage	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
I_{OL}	Output Leakage	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	V_{IN} = 0V to V_{CC}	−2.5 −10	2.5 10	μA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage		4.5V ≤ V_{CC} ≤ 5.5V	 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage		3V ≤ V_{CC} ≤ 4.5V	−0.1 2	0.6 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	 V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		3V ≤ V_{CC} ≤ 4.5V I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	 V V
f_{SK}	SK Clock Frequency	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E		0 0	1 0.5	MHz
t_{SKH}	SK High Time	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	(Note 2) (Note 3)	500 500		ns
t_{SKL}	SK Low Time	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	(Note 2) (Note 3)	250 500		ns
t_{CS}	Minimum CS Low Time	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	(Note 4) (Note 5)	250 500		ns
t_{CSS}	CS Setup Time	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	Relative to SK	50 100		ns
t_{PRES}	PRE Setup Time	NMC93CS06-NMC93CS66 NMC93CS06E-NMC93CS66E	Relative to SK	50 100		ns
t_{PES}	PE Setup Time	NMC93CS06-NMC93CS66 NMC93CS06E-NMC93CS66E	Relative to SK	50 100		ns

2

DC and AC Electrical Characteristics V_{CC} = 3.0V to 5.5V (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	Relative to SK	100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	Relative to SK	100 200		ns
t_{PD1}	Output Delay to "1"	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	AC Test		500 1000	ns
t_{PD0}	Output Delay to "0"	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	AC Test		500 1000	ns
t_{SV}	CS to Status Valid	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	AC Test		500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC93C06-NMC93C66 NMC93C06E-NMC93C66E	AC Test CS = V_{IL}		100 200	ns
t_{WP}	Write Cycle Time				15	ms
	Endurance		Number of Data Changes per Bit	Typical 100,000		Cycles

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 2 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 μs. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 1750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature parts specifies a minimum SK clock period of 2 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 2 μs. For example, if the t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Capacitance (Note 6)

T_A = 25°C f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Functional Description

T-46-13-27

The NMC93C06/C46/C56/C66 have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 10-bits carry the op code and the 8-bit address for register selection.

Read (READ):

The Read (READ) instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (EWEN):

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the specified register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The Write (WRITE) instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at V_{CC} = 5.0V ±10%.

Write All (WRAL):

The (WRAL) instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at V_{CC} = 5.0V ±10%.

Erase/Write Disable (EWDS):

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Instruction Set for the NMC93C06 and NMC93C46

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory, at specified address.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
ERASE	1	11	A5–A0		Erase register A5A4A3A2A1A0.
WRITE	1	01	A5–A0	D15–D0	Writes register.
ERAL	1	00	10XXXX		Erases all registers. Valid only at V_{CC} = 4.5V to 5.5V.
WRAL	1	00	01XXXX	D15–D0	Writes all registers. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXX		Disables all programming instructions.

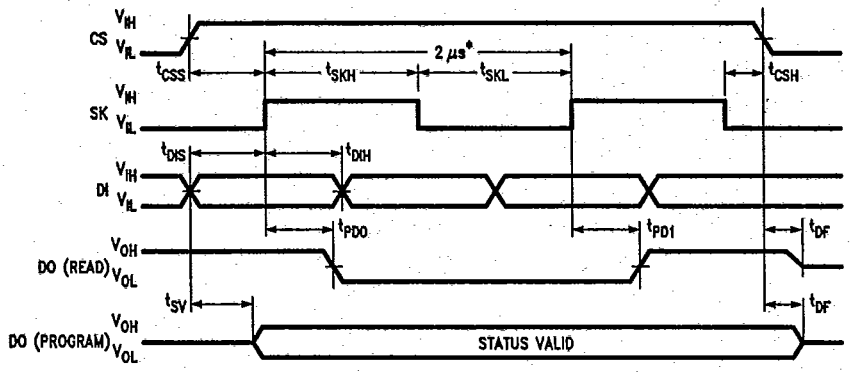
Instruction Set for the NMC93C56 and NMC93C66

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
ERASE	1	11	A7–A0		Erase register A7A6A5A4A3A2A1A0.
ERAL	1	00	10XXXXXX		Erases all registers. Valid only at V_{CC} = 4.5V to 5.5V.
WRITE	1	01	A7–A0	D15–D0	Writes register if address is unprotected.
WRAL	1	00	01XXXXXX	D15–D0	Writes all registers. Valid only when Protect Register is cleared. Valid only at V_{CC} = 4.5V to 5.5V.
EWDS	1	00	00XXXXXX		Disables all programming instructions.

T-46-13-27

Timing Diagrams

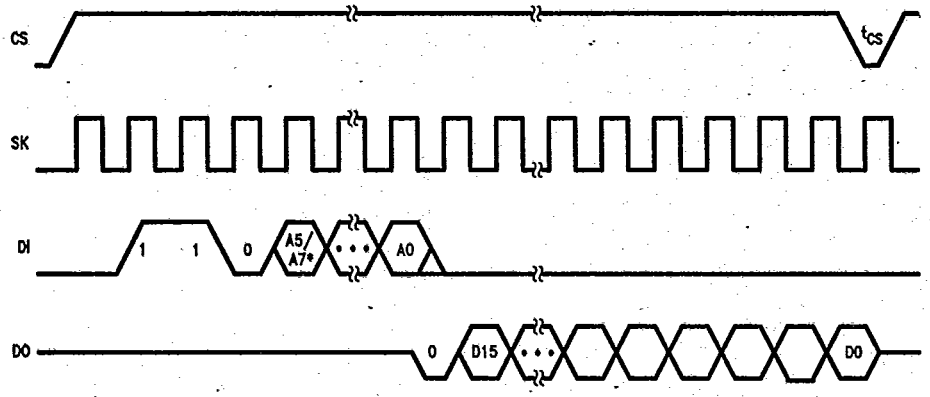
Synchronous Data Timing



TL/D/10045–4

*This is the minimum SK period (Note 2).

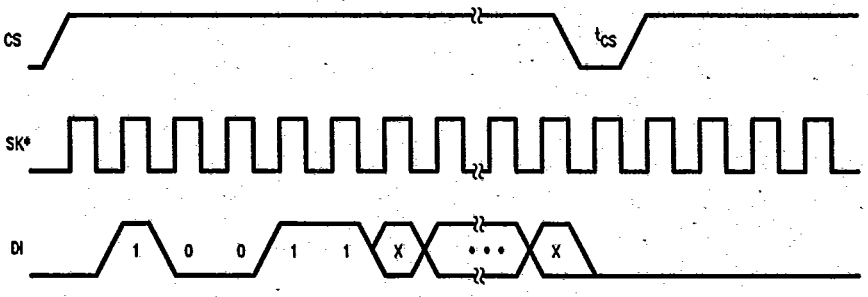
READ:



TL/D/10045–5

*Address bits A_5 and A_4 become "don't care" for NMC93C06.
*Address bit A_7 becomes a "don't care" for NMC93C56.

EWEN:



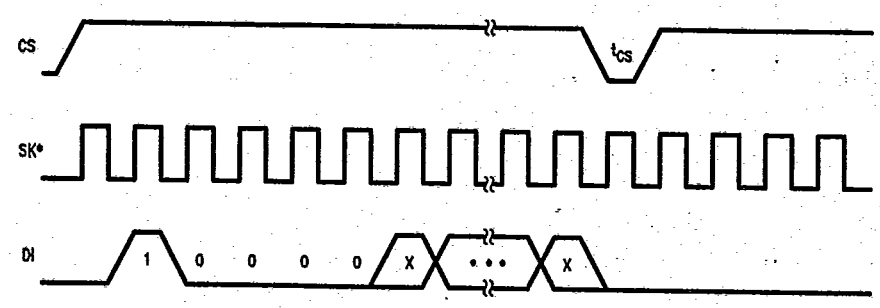
TL/D/10045–6

*The NMC93C56 and NMC93C66 require a minimum of 11 clocks. The NMC93C06 and NMC93C46 require a minimum of 9 clock cycles.

Timing Diagrams (Continued)

T-46-13-27

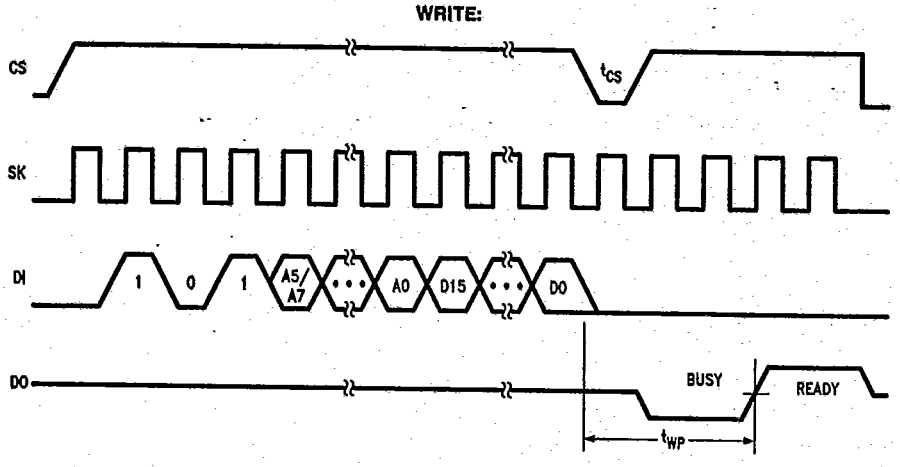
EWDS:



TL/D/10045–7

*The NMC93C56 and NMC93C66 require a minimum of 11 clocks. The NMC93C06 and NMC93C46 require a minimum of 9 clock cycles.

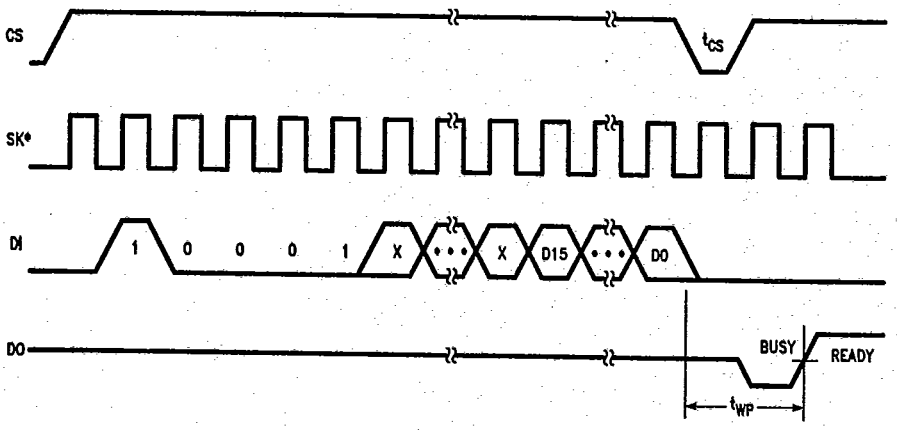
WRITE:



TL/D/10045–8

*Address bit A_5 and A_4 become "don't care" for NMC93C06.
*Address bit A_7 becomes a "don't care" for NMC93C56.

WRAL:†



TL/D/10045–9

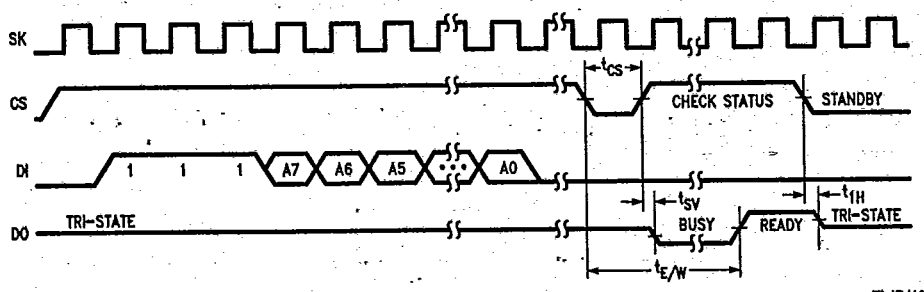
*The NMC93C56 and NMC93C66 require a minimum of 11 clocks. The NMC93C06 and NMC93C46 require a minimum of 9 clock cycles.
†Valid only at V_{CC} = 4.5V to 5.5V.

2

Timing Diagrams (Continued)

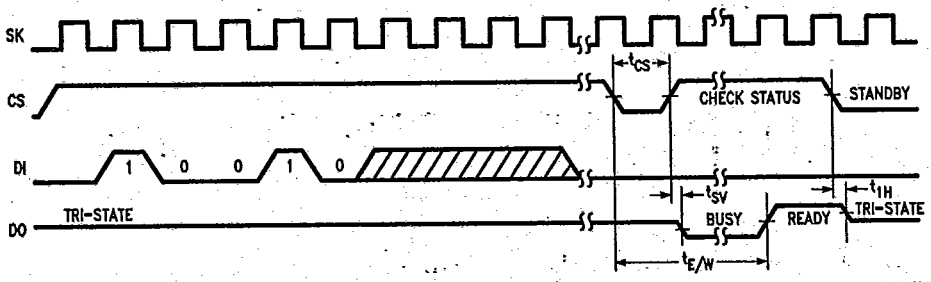
T-46-13-27

ERASE:



TL/D/10045-10

ERAL:†



TL/D/10045-11

†Valid only at V_{CC} = 4.5V to 5.5V.