National Semiconductor

PRELIMINARY

T-46-13-27

NMC95C12 1024-Bit CMOS EEPROM with DIP Switches

General Description

The NMC95C12 is a 1024-bit, CMOS EEPROM with 8 programmable outputs that can be used as DIP switches. The 1024 bits of memory are divided into 64 registers of 16 bits each and each register can be individually accessed. Registers 61–63 are dedicated to storing the switch settings.

In addition to the 1024 bits of EEPROM memory, the NMC95C12 contains eight individually programmable outputs which can be used as DIP switches. Each output may be programmed to provide either a High or Low level. These outputs may also be programmed to form four individual pairs of SPST switches.

The switch configuration information is obtained from a non volatile register whenever power is first applied to the device. This ensures the switches will always have a user determined state upon power-up.

The NMC95C12 is designed to meet applications requiring 40,000 write cycles per register and at least 10 year data retention.

Features

- 1024 bits of CMOS EEPROM memory
- 8 DIP switch positions or 4 SPST switch positions
- 4 mA (max) operating current, 50 μA (max) standby current
- Software write protection
- Serial I/O interface fully MICROWIRE compatible
- Single +5V ±10% operation
- 14-pin DIP or SO package availability
- 40,000 write operations
- 10 year data retention
- Reliable floating gate technology
- Sequential register read
- Self-timed write cycle
- Erase cycles not necessary
- Compatible with COPS™ microcontrollers

Block Diagram

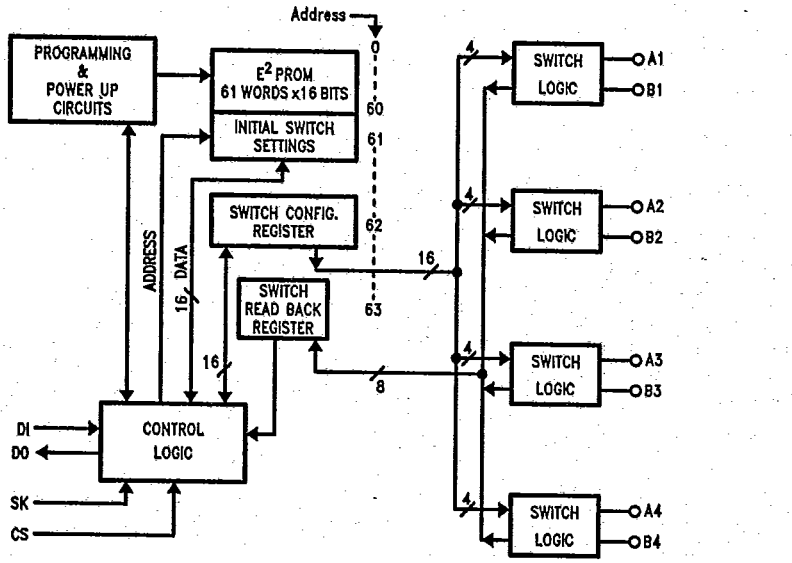

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FIGURE 1. Block Diagram

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	6.5V
Voltage at Any Pin	−0.3 to +6.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation @25°C	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NMC95C12	0°C to +70°C
NMC95C12E	−40°C to +85°C
NMC95C12M*	−55°C to +125°C
Power Supply Voltage	4.5V to 5.5V

*Contact factory for availability

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DC Electrical Characteristics V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	$C_S = V_{IH}$, SK = 1 MHz		4	mA
I_{CC2}	Operating Current TTL Input Levels	$C_S = V_{IH}$, SK = 1 MHz		6	mA
I_{CC3}	Standby Current CMOS Input Levels on Switches	C_S = 0V		50	μA
I_{CC4}	Standby Current TTL Input Levels on Switches	C_S = 0V		800	μA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}	−2.5	+2.5	μA
I_{oL}	Output Leakage	V_{OUT} = 0V to V_{CC}	−2.5	2.5	μA
V_{IL}	Input Low Voltage		−0.1	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA	2.4		V
R_{ON}	Switch On Resistance			200	Ω
R_{OFF}	Switch Off Resistance		10		MΩ
V_S	Maximum Voltage Allowed on any Switch Terminal			V_{CC} + 1	V

AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
f_{SK}	SK Clock Frequency	NMC95C12		0	1	MHz
		NMC95C12E		0	0.5	
		NMC95C12M		0	0.5	
t_{SKH}	SK High Time	NMC95C12	(Note 2)	250		ns
		NMC95C12E	(Note 3)	500		
		NMC95C12M	(Note 3)	500		
t_{SKL}	SK Low Time	NMC95C12	(Note 2)	250		ns
		NMC95C12E	(Note 3)	500		
		NMC95C12M	(Note 3)	500		
t_{CS}	Minimum CS Low Time	NMC95C12	(Note 4)	250		ns
		NMC95C12E	(Note 5)	500		
		NMC95C12M	(Note 5)	500		
t_{CSS}	CS Setup Time	NMC95C12	Relative to SK	50		ns
		NMC95C12E		100		
		NMC95C12M		100		

AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NMC95C12 NMC95C12E NMC95C12M	Relative to SK	100 200 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time	NMC95C12 NMC95C12E NMC95C12M	Relative to SK	100 200 200		ns
t_{PD1}	Output Delay to "1"	NMC95C12 NMC95C12E NMC95C12M	AC Test		500 1000 1000	ns
t_{PD0}	Output Delay to "0"	NMC95C12 NMC95C12E NMC95C12M	AC Test		500 1000 1000	ns
t_{SV}	CS to Status Valid	NMC95C12 NMC95C12E NMC95C12M	AC Test		500 1000 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NMC95C12 NMC95C12E NMC95C12M	CS = V_{IL} AC Test		100 200 200	ns
t_{ISWD}	Switch Delay from Switch Input	NMC95C12 NMC95C12E NMC95C12M	AC Test		250 500 500	ns
t_{SWPD0}	Switch Delay to 0 from Config. Change	NMC95C12 NMC95C12E NMC95C12M	AC Test		500 1000 1000	ns
t_{SWPD1}	Switch Delay to 1 from Config. Change	NMC95C12 NMC95C12E NMC95C12M	AC Test		500 1000 1000	ns
t_{SWS}	A1–A4, B1–B4 Setup Time	NMC95C12 NMC95C12E NMC95C12M		100 200 200		ns
t_{SWH}	A1–A4, B1–B4 Hold Time	NMC95C12 NMC95C12E NMC95C12M		100 200 200		ns
t_{WP}	Write Cycle Time				10	ms
	Endurance		Number of Data Changes per Bit	Typical 40,000		Cycles

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", the device should not be operated at these limits. The table of "Electrical Characteristics" provides actual operating limits.

Note 2: The SK frequency specification for Commercial parts specifies a minimum SK clock period of 1 μs, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 1 μs. For example if t_{SKL} = 250 ns then the minimum t_{SKH} = 750 ns in order to meet the SK frequency specification.

Note 3: The SK frequency specification for Extended Temperature and Military parts specifies a minimum SK clock period of 2 μs, therefore in an SK clock cycle t_{SKH} + t_{SKL} must be greater than or equal to 2 μs. For example, if t_{SKL} = 500 ns then the minimum t_{SKH} = 1.5 μs in order to meet the SK frequency specification.

Note 4: For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 5: For Extended Temperature and Military parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Note 6: This parameter is periodically sampled and not 100% tested.

Note 7: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from +65°C to +85°C.

Capacitance (Note 6)

T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Connection Diagrams

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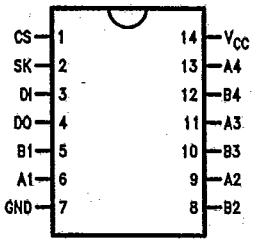
SO Package



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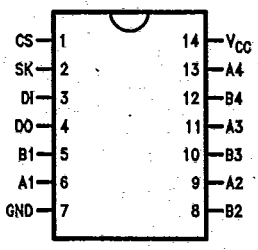
Top View
Order Number NMC95C12M, NMC95C12EM and NMC95C12MM
See NS Package M14A

Dual-In-Line Package



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Top View
Order Number NMC95C12N, NMC95C12EN and NMC95C12MN
See NS Package N14A

Pin Names

CS	Chip Select
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
A1–A4	Switch Terminals
B1–B4	Switch Terminals

Pin Descriptions

Pin Name	Description
CS	Chip Select, Input—This input must be high while communicating with the NMC95C12. When this input is LOW, the chip is powered down into the standby mode. It should be noted that the CS does not control the A1 through A4 and B1 through B4 outputs and hence has no effect on them. The CS input must be made LOW after completing an instruction to prepare the control logic to accept the next instruction. If the CS input becomes LOW prematurely, the operation in progress is aborted. If programming the E^2 memory is in progress and the CS goes LOW, the programming is not aborted but will proceed to its normal completion.
SK	Serial Clock, Input—This input is used for clocking the serial I/O. The CS input must be high for clocking to have any effect. Information presented on the DI input will be shifted into the device on the LOW to HIGH transition of the clock. Information from the device will be available on the DO output serially, in response to the LOW to HIGH transition of the clock.
DI	Serial Data In, Input—All information needed for the operation of the device is entered serially from this input. HIGH represents logic '1' and LOW represents logic '0'. The entry order is most significant bit first and least significant bit last.
DO	Serial Data Out, Output, 3-state—When data is read, data from the addressed location will be available on this output serially, in sync with the LOW to HIGH transitions on the SK input. Normally the DO pin is in high impedance state. During a read instruction, when the last bit of the address is shifted in, the DO will go LOW indicating that data will follow. The data will follow in response to the clock transitions. The data will come out most significant bit first and least significant bit last. During E^2 programming operations, this output is also used as the status indicator. During programming operations, LOW indicates Busy (programming in progress) and HIGH indicates Ready. The DO output will be in the high impedance state if the CS input is LOW unconditionally.
A1–A4 B1–B4	Switch Terminals—These pins provide the simulated DIP switch features and hence are called terminals. The behavior of these pins is determined by the settings in the Switch Configuration Register and are independent of the CS input.
V_{CC}	+5V Power Supply.
GND	Ground.

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Functional Description

Figure 1 is a block diagram of the NMC95C12. It consists of a 62-word X 16-bit E²PROM array, a 16-bit Switch Configuration Register (SCR), a 16-bit Switch Readback Register (SRR), four identical blocks of switch logic, programming and power-up circuits and the necessary control logic. It may be noted that only eight bit positions of the SRR are used in the NMC95C12.

ADDRESS SPACE

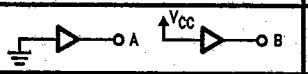
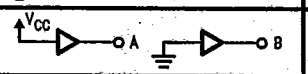
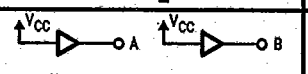
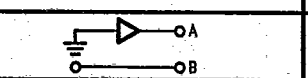
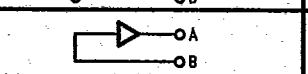
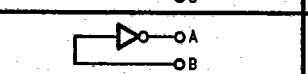
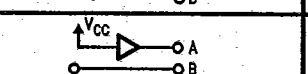
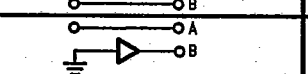
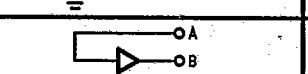
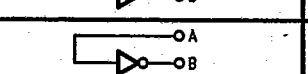
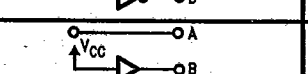
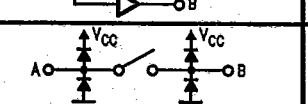
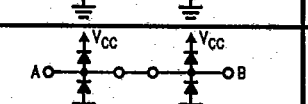
Registers 0–60 of the E²PROM are available to the user as general purpose non-volatile memory. Data may be read or programmed into this memory using the appropriate instructions. Address location 61 is an E² location which also can be read or programmed like any other E² location. However, address 61 is used in the NMC95C12 to provide the initial switch configuration information automatically on power-up.

The SCR is located at address 62. The SCR is not an E² location and hence is volatile. It does not have endurance limits or programming time requirements associated with it, allowing the switches to be reconfigured an unlimited number of times.

The SCR is automatically loaded from address 61 on power-up. The SCR controls the switch logic and hence the behavior of the terminals A1 through A4 and B1 through B4.

Located at address 63 is the Switch Readback Register (SRR). This is a read only register.

TABLE I. Switch Configurations

MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0 , B = 0
1	0	0	0	1		A = 0 , B = 1
2	0	0	1	0		A = 1 , B = 0
3	0	0	1	1		A = 1 , B = 1
4	0	1	0	0		A = 0 , B = Tristate
5	0	1	0	1		A = B
6	0	1	1	0		A = $\bar{B}$
7	0	1	1	1		A = 1 , B = Tristate
8	1	0	0	0		A = Tristate , B = 0
9	1	0	0	1		B = A
10	1	0	1	0		B = $\bar{A}$
11	1	0	1	1		A = Tristate , B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

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*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.

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Functional Description (Continued)

SWITCH CONFIGURATIONS

The 16-bit SCR format is shown in *Figure 2*. It consists of four 4-bit fields. Each field controls its corresponding switch control logic. The individual bits in each field are labelled W, X, Y, and Z. Table I shows the relationship between these bit values and the resulting behavior of the terminals. It should be remembered that the CS input has no effect on the behavior of the terminals.

SWITCH READBACK REGISTER

The SRR allows the current logic level present at the switch terminals to be read back via the Microwire bus. The SRR is loaded by the rising edge of SK immediately after the last instruction bit is clocked in (The same clock edge that loads A0). The SRR is loaded on this clock edge only when register 63 (Switch Readback Register) is being read. In the case of switch mode 13 (Analog switch mode), the SRR will not report the actual levels present at the terminals due to this mode being analog levels. In mode 13, bits 15–8 of the SRR will be all 0's to indicate a closed analog switch. This is done to avoid ambiguous logic levels which could exist when the device is used in the analog switch mode.

The bit assignments and conceptual function of the SRR is shown in *Figure 3*. As shown, only bits 15 thru 8 are used, and bits 7 thru 0 are always read as logical 0. The SRR is a Read-Only register and if it is written, the device will not perform a write or generate a Ready/Busy status. The SRR is not implemented in EEPROM, allowing an infinite number of cycles in the register.

INSTRUCTION SET

The NMC95C12 instruction set contains five instructions, and each instruction is nine bits long. One SK clock cycle is necessary, after CS equals logical "1", before an instruction can be loaded. The first bit of the instruction is the start bit (SB) and is always a logical "1", followed by the op code (2 bits) and the address field (6 bits). The WRITE and WRALL instructions are followed by sixteen bits of data (D15–D0) which is written into the memory. Table II is a list of the instructions and their format.

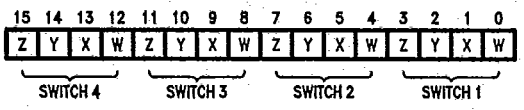

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FIGURE 2. Switch Configuration Register (SCR)

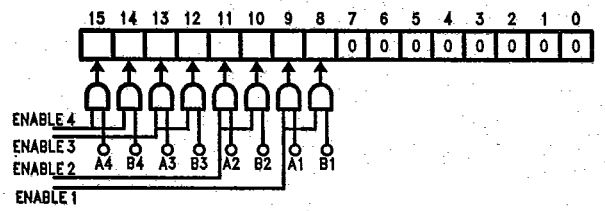

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FIGURE 3. Switch Readback Register (SRR)

TABLE II. NMC95C12 Instructions

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	Writes register.
WRALL	1	00	01XXXX	D15-D0	Writes all registers.
WDS	1	00	00XXXX		Disables all programming instructions.

Functional Description (Continued)

WDS (Write Disable): When this instruction is issued, all subsequent writing into the NMC95C12 is locked out. Any attempt to write into a locked device is ignored. The NMC95C12 powers up in the locked state. The WEN is the only instruction that unlocks the device. The write disable operation has no effect on read operations. Thus reading will occur normally even from a locked device.

WRALL (Write All): When this instruction is executed, the NMC95C12 bulk-programs the same 16-bit data pattern into all of its E^2 memory locations (address 0 through 61). The SCR is unaffected since it is not an E^2 location. The data pattern must follow immediately after the last bit of this instruction. The chip enters into the self-timed program mode after CS is brought low, before the next rising edge of SK.

WEN (Write Enable): This instruction is used to unlock the write circuits. The circuits will remain unlocked until the WDS instruction locks them. The NMC95C12 powers up in the locked state and hence WEN must be executed prior to any programming instructions.

WRITE (Write/Program): This instruction writes a 16-bit data word into the address location specified by the A_0–A_5 bits of the instruction. The 16 data bits must follow the last bit of the instruction. After loading the WRITE instruction and the 16-bit data, the chip enters into the self-timed program mode when CS is brought low before the next rising edge of the SK clock. If the addressed location is the SCR, then the chip does not enter into the self-timed E^2 programming mode (the SCR is not an E^2 location) but loads the switch configuration data into the SCR. The WRITE instruction can only be aborted by deselecting the chip (CS LOW) before entering all the instruction bits. The NMC95C12 does not require erasing prior to writing.

READ (Read): This instruction reads the data from the addressed location. As before, the instruction also contains the address. The data will come out serially on the DO output on the rising edge of the clock. A logical '0' precedes the 16-bit data (dummy bit).

The NMC95C12 has a convenient feature called sequential register read. Normally, the CS input is made LOW after the last data bit is shifted out. However, if the CS input is left HIGH and clocking continues, data from the next address location will be delivered on the DO pin. This sequential read can continue indefinitely whereby the address is automatically incremented after delivering 16 bits of data. It should be noted that in the sequential register read mode, address wrap-around will occur.

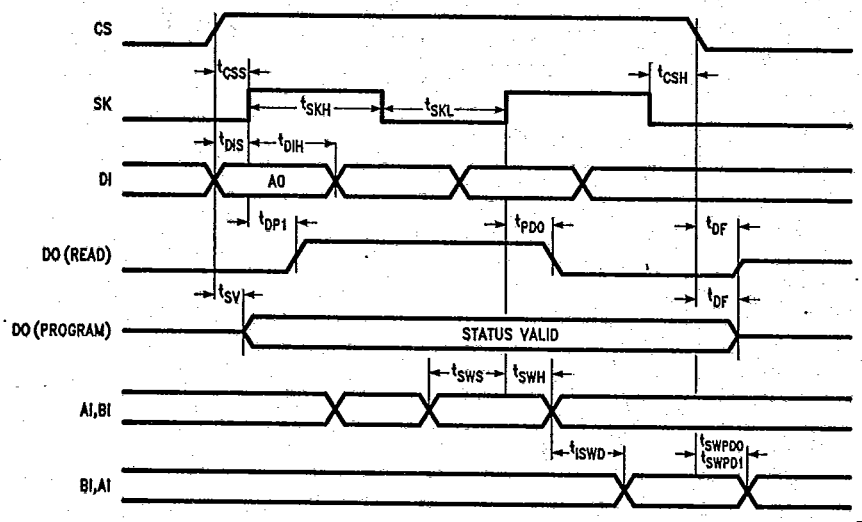
During a sequential register read there will be a dummy bit preceding the first word read, after which, the bit stream will be continuous without any dummy bits separating the data words.

Ready/Busy Indication

Programming an E^2 memory takes several milliseconds. Unlike some devices which require the user to keep track of the elapsed time to ensure completion of the programming cycle, the NMC95C12 contains an on-chip timer. The timer starts when the CS input goes LOW after the last data bit is entered. After entering a programming cycle (CS forced LOW), the timer status may be observed by forcing the CS input back HIGH. The timer status is available on the DO pin if the CS input is forced HIGH within one ms of starting the programming cycle. LOW on the DO pin indicates that the programming is still in progress while HIGH indicates the device is READY for the next instruction. It should be noted that if the CS input is made HIGH for status observation, it must be made LOW when READY is indicated before loading the next instruction.

Timing Diagrams

Synchronous Data Timing



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Timing Diagrams (Continued)

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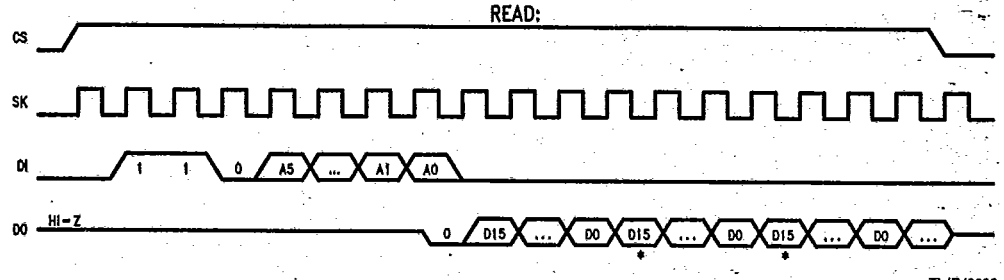
Instruction Sequence

READ:



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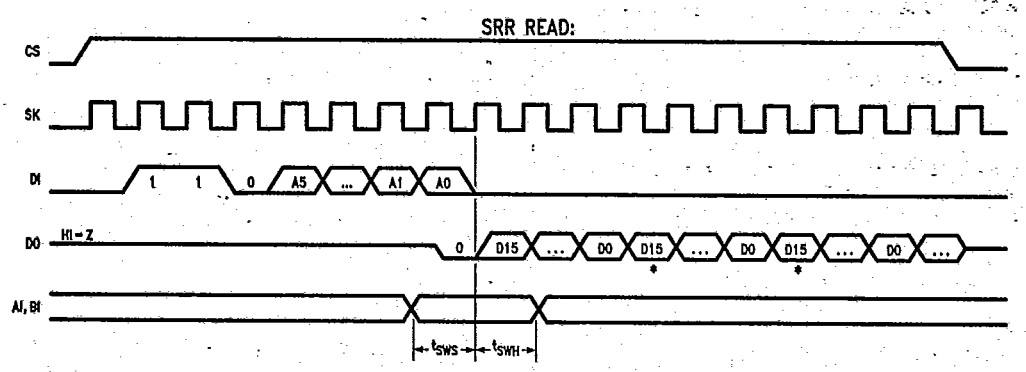
SRR READ:



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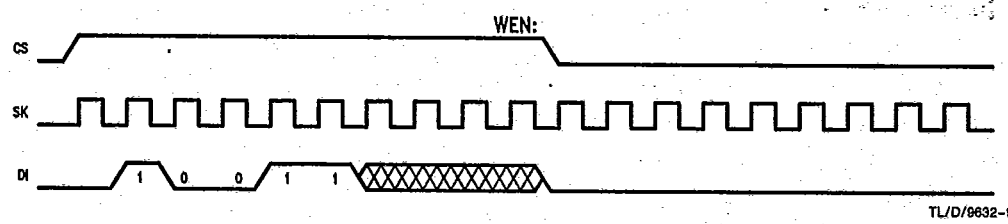
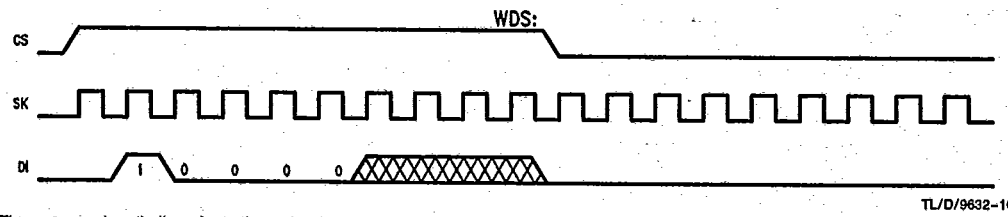
WEN:



TL/D/9632-9

WDS:



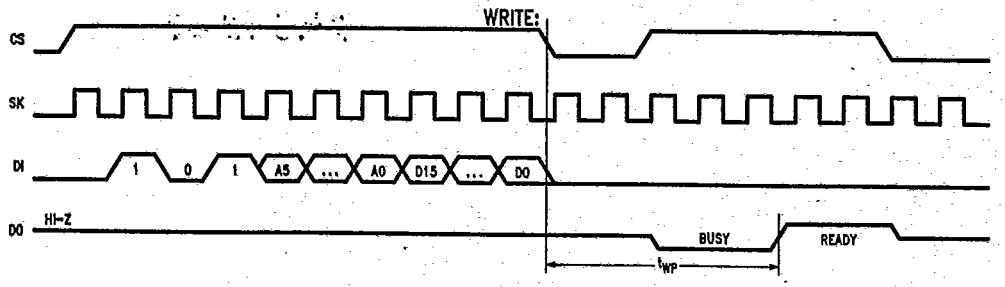
TL/D/9632-10

*The memory automatically cycles to the next register.

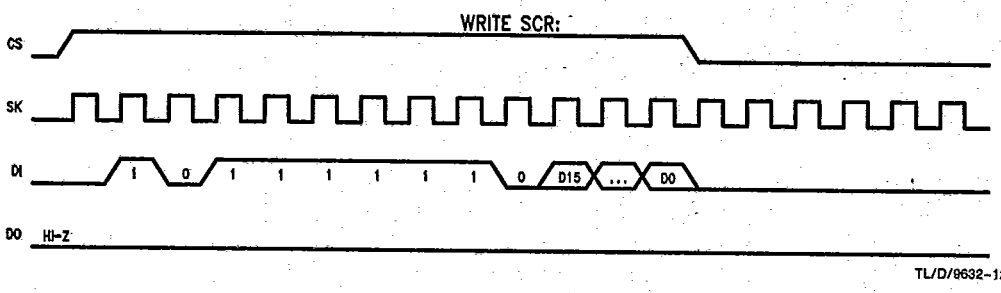
Timing Diagrams (Continued)

T-46-13-27

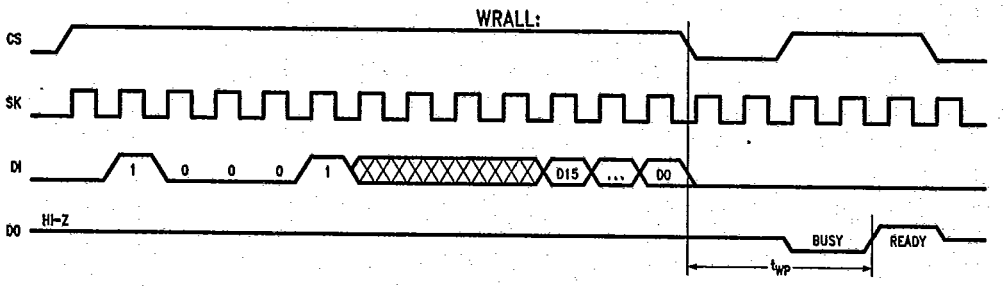
Instruction Sequence (Continued)



TL/D/9632-11



TL/D/9632-12



TL/D/9632-13

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