



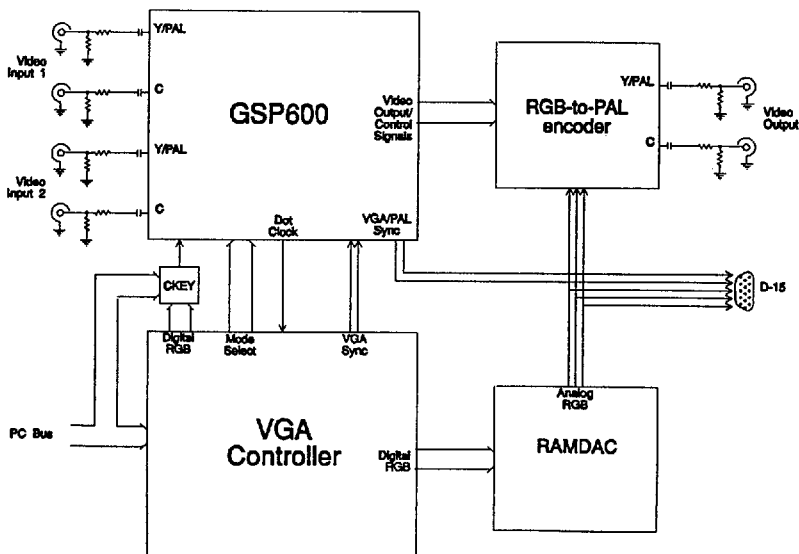
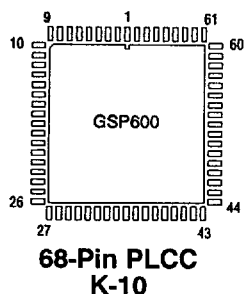
## VGA/PAL Video Genlock Processor with Overlay

### Overview

The **GSP600** allows the text and graphic images of VGA and Super VGA controllers to be displayed on standard PAL televisions or recorded on a VCR. Additionally, the **GSP600** accepts external video input from a camcorder or a VCR and will synchronize (genlock) the VGA or Super VGA controller to the external video. The **GSP600** also allows VGA and video images to be overlaid on the same television screen. The **GSP600** meets or exceeds all PAL broadcast standards for timing accuracy and allows the VGA controller to maintain true PAL compatibility at all times. The **GSP600** is compatible with virtually all VGA controllers. Tseng Labs, Oak Technology, Trident Microsystems, S3, and NCR have BIOS support available for the GSP family of products.

### Features

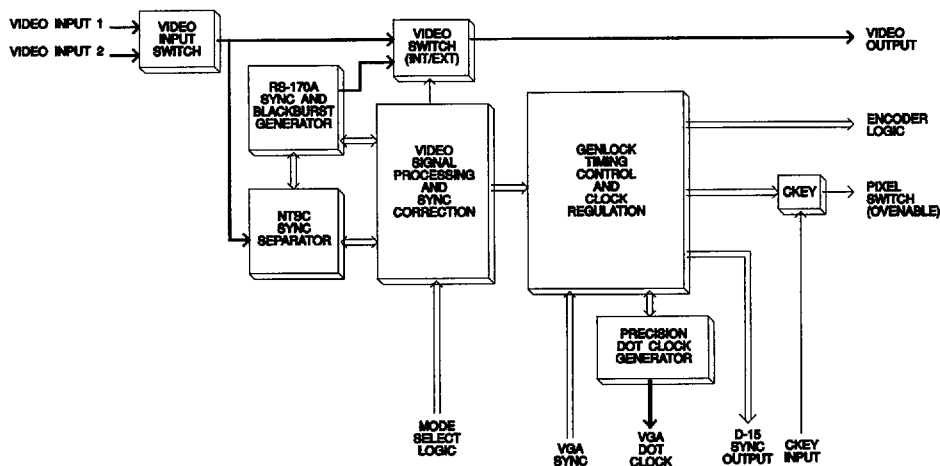
- Direct input of PAL or S-Video (S-VHS and Hi-8 video).
- On board PAL/S-Video sync and black burst generation for local video operation. Video chroma burst separate with 4.433618 MHz and 17.734475 MHz phase locked outputs.
- Meets or exceeds all timing specifications for studio and broadcast television.
- High efficiency PAL/S-Video conversion that maintains VGA performance.
- Dynamic overscan and underscan adjustment of PAL/S-Video modes under BIOS and/or software control.
- Software selection between all VGA and PAL/S-Video modes.
- PAL/S-Video conversion support for all VGA and Extended VGA modes with 600 or fewer lines.
- Built-in dot clock circuitry to eliminate crystal oscillators for VGA, plus extended VGA operation up to 135 MHz.
- Low power consumption, ideal for laptop computers.





# GSP600

Internal Block Diagram



## Theory of Operation

The **GSP600** can be thought of as an extremely sophisticated dot clock generator. In its simplest form, the **GSP600** will generate all of the dot clock frequencies necessary to drive VGA and Super VGA controllers. The different frequencies are selected with the **MODE SELECT LOGIC** from the VGA chip. Selection is similar to selecting frequencies on any of the ICS dot clock generators (i.e., ICS1394, ICS1494, ICS1561, ICS2494, etc.). Additionally, there are four reserved frequency addresses. These are labeled GL (genlock), OV (overlay), VO (video only), and GO (graphics only). Choosing any of these addresses will switch the **GSP600** from VGA mode to PAL mode. Under PAL mode, the **GSP600** accepts vertical and horizontal **VGA SYNC** from the VGA controller and uses the sync to generate and adjust the **VGA DOT CLOCK**. The **GSP600** will automatically vary the frequency of the dot clock in order to synchronize the VGA sync signals with a PAL reference signal. This reference signal can be derived from a video device (such as a camcorder) connected to **VIDEO INPUT 1** or **VIDEO INPUT 2**. The **GSP600** provides an RGB-to-PAL encoder with the **VIDEO OUTPUT** signal which is either **VIDEO INPUT 1**, **VIDEO INPUT 2**, or an internally generated black burst signal. All of the necessary **ENCODER LOGIC** signals to properly drive the encoder are provided by the **GSP600**.

During PAL modes the **GSP600** also creates the **D-15 SYNC OUTPUT** for the monitor connection to allow for TV projection output of the VGA images. The **PIXEL SWITCH** information derived from external **CKEY INPUT** tells the encoder whether to display the VGA image or external video for each pixel. Assuming the images are genlocked, this creates the overlay effect.

## Block definition

### Video Input Switch

The Video Input Switch selects whether the **GSP600** uses **VIDEO INPUT 1** or **VIDEO INPUT 2** as the external video source. It is controlled by an external pin of the **GSP600**.

### PAL Sync Separator

The **GSP600** contains a high quality sync separator to allow direct input of PAL, S-VHS, or HI-8 video signals from camcorders, VCRs, and other video products. The **GSP600** utilizes a differential video input circuitry for maximum noise immunity. It also employs digital noise filtering and enhanced digital signal tracking technology to ensure maximum compatibility with consumer, industrial, and broadcast video signals. Although low cost video sync separator products are commonly available, they are primarily designed for television and video monitor use. The simple diode clamping circuit used in these devices does not have the accuracy or noise immunity required for genlocking.



## **PAL Sync and Black Burst Generator**

### *PAL Sync Generator*

The studio quality built-in video sync generator allows the **GSP600** to operate without an external video input and still maintain broadcast video timing. This assures PAL compatibility at all times. When external video is present, the sync generator works in conjunction with the sync separator to isolate sync from noisy video signals.

### *Black Burst Generation*

Most RGB-to-PAL encoders synchronize a crystal oscillator to the chroma burst signal of the external video signal. This provides the color reference portion of the video signal. If an external video signal is not available, the crystal oscillator will free run, creating screen artifacts such as 45 degree moving lines in constant color portions of the screen. To eliminate this problem, the **GSP600** generates a black burst video signal. Black burst video is an analog signal containing both sync and a correctly phased chroma burst signal. This ensures proper color reference generation at all times. The **GSP600** provides black burst output to the encoder when external video is either missing or not selected (non-genlock mode).

### *INT/EXT Video Switch*

The Internal/External Video Switch determines whether the encoder uses external video or the black burst signal. If external video is chosen, the **GSP600** will simply pass the external video signal through to the encoder, unaffected. Black burst is used when external video is not present. The switch is controlled by the Video Signal Processing and Sync Correction circuitry.

## **Video Signal Processing and Correction**

### *Video Signal Processing*

The Video Signal Processing circuitry of the **GSP600** measures the incoming video signal for basic timing accuracy and signal noise. It contains intelligent circuitry to remove extraneous portions of the video signal that would normally be incorrectly categorized as sync. This is extremely important when using a VCR as a video input. If there is an interruption of the external video signal, this circuit will automatically switch inputs from the external video signal to the internal sync generator. When the external video signal resumes, the circuit will automatically switch back to the external video. The Video Signal Processing accepts the MODE SELECT LOGIC from the VGA chip. This logic chooses either VGA or PAL operation and selects whether genlock to external video is to be enabled.

### *Sync Correction*

The Sync Correction circuitry looks for missing sync pulses, block sync, single field video, and phase shift errors caused by the head switching zone of a VCR. It assures proper genlock during all of these problems common in consumer video products.

### *Genlock Timing Control and Clock Regulation*

The **GSP600** looks at the input sync from the VGA controller and determines how to alter the dot clock to create PAL timing. Both the frequency and the method can change with different VGA modes. The **GSP600** enables virtually any VGA controller capable of interlacing to create PAL timing. The **GSP600**'s unique architecture provides ultra-high efficiency and flexibility and allows the frequency of the dot clock to be controlled totally under BIOS or software control. Screen attributes such as horizontal width and position can be individually programmed for each mode while maintaining genlock integrity. This circuit will modify the timing of virtually any mode, with 600 or fewer lines, to meet PAL specifications. The **GSP600** genlock timing control and clock regulation design is awaiting patent approval.

## **Precision Dot Clock Generator**

The **GSP600** uses the same state-of-the-art dot clock technology that has made ICS the premier supplier of VGA dot clock generators. ICS offers the highest accuracy and lowest jitter products available.

### **CKEY**

The ckey (or color-key) circuitry creates the pixel switch for the encoder. This signal determines whether the VGA image or external video is displayed for each pixel. Ckey is modified by the **GSP600** to ensure that the pixel switch signal is delayed (to make up for delays in the RAMDAC) and that it has proper levels during sync and blanking. If the VGA and external signals are genlocked, this pixel switch will create an overlay effect.



# GSP600

| <u>PIN<br/>NUMBER</u> | <u>NAME</u>     | <u>DESCRIPTION</u>   |
|-----------------------|-----------------|--|
| 1                     | VLE             | VERTICAL LOCK ENABLE. HIGH for VGA controllers. LOW disables vertical lock feature, may be useful for Non-VGA Operation.   |
| 2                     | ODD/EVEN        | ODD/EVEN FIELD IDENTIFICATION. HIGH indicates odd numbered field, LOW indicates even numbered field.   |
| 3                     | BP              | BACK PORCH PULSE. Negative polarity TTL level signal used by some RGB-to-PAL encoders.   |
| 4                     | DATAIN          | Data input for inserting SMPTE time code in video signal.  |
| 5                     | CB              | COMPOSITE BLANKING OUTPUT. Indicates non-screen data portions of PAL signal.   |
| 6                     | CS              | COMPOSITE SYNC. PAL composite sync output for RGB-to-PAL encoders. Gated off during VGA modes.   |
| 7                     | CKEY            | COLOR KEY. Resultant input from the 8-bit compare of digital RGB (P0-P7) and a software selectable byte. This color key determines which pixels display VGA and which display external video in overlay mode. See Hardware Interface Manual for more details.                              |
| 8                     | TEST            | For ICS use only.  |
| 9                     | VSYNOUT         | VERTICAL SYNC OUTPUT. Vsync output for DB-15 connector.  |
| 10                    | DATAFRAME       | TTL level framing signal active during lines 10-20. For use in time code applications.   |
| 11                    | OVENABLE        | OVERLAY ENABLE. Fast pixel rate switch. HIGH displays PAL output, LOW display RGB output. Used for overlay encoders. See Application Notes for wiring details.   |
| 12                    | I/ES            | INT./EXT. SYNC. Determines sync selection in OVENABLE signal. Tie LOW normally.  |
| 13                    | LOC/REM         | LOCAL/REMOTE. A LOW output state signifies REMOTE status indicating that external video is present and a genlock mode has been selected. If external video goes away or a non-genlock mode is selected, LOCAL/REMOTE will go HIGH.   |
| 14                    | <u>BRSTACT</u>  | For ICS use only.  |
| 15                    | <u>FRTSTOUT</u> | For ICS use only.  |
| 16                    | HS              | HORIZONTAL SYNC. For some RGB-to-PAL encoders. Gated off during VGA modes.   |
| 17                    | <u>HRSTOUT</u>  | For ICS use only.  |
| 18                    | HSYNOUT         | HORIZONTAL SYNC OUTPUT. Hsync output for DB-15 connector.  |
| 19                    | VSS             | Digital ground. We strongly recommend the use of a multilayer board and a ground plane.  |
| 20                    | VDD             | 5 Volt digital power. We strongly recommend the use of a multilayer board and a power plane.   |
| 21                    | VDD             | 5 Volt digital power. We strongly recommend the use of a multilayer board and a power plane.   |
| 22                    | VSS             | Digital ground. We strongly recommend the use of a multilayer board and a ground plane.  |
| 23                    | FS5             | Frequency Select 5. Selects between multiple VGA Dot Clock frequencies, Genlock modes and PAL frequencies. See Dot Clock Generation and PAL Mode Selection sections for a more detailed description. Also see Application Notes for wiring diagrams and BIOS Interface Manual for details. |



| <u>PIN<br/>NUMBER</u> | <u>NAME</u> | <u>DESCRIPTION</u>   |
|-----------------------|-------------|--|
| 24                    | FS4         | Frequency Select 4. Selects between VGA Dot Clock frequencies and PAL modes.   |
| 25                    | FS3         | Frequency Select 3. Selects between VGA Dot Clock frequencies and PAL modes.   |
| 26                    | FS2         | Frequency Select 2. Selection between VGA Dot Clock frequencies and PAL modes.   |
| 27                    | FS1         | Frequency Select 1. Selects between VGA Dot Clock frequencies and PAL modes.   |
| 28                    | FS0         | Frequency Select 0. Selects between VGA Dot Clock frequencies and PAL modes.   |
| 29                    | EXTSYNC     | For ICS use only.  |
| 30                    | VCR1        | HIGH permits using VCRs as an input.   |
| 31                    | CLAMPLEV    | Clamping level adjustment for video input. See Application Notes for more details.   |
| 33                    | Y1          | PAL video input number 1. Note: This is also the Y (luminance) input for S-Video systems.  |
| 32                    | Y2          | PAL video input number 2. Note: This is also the Y (luminance) input for S-Video systems.  |
| 34                    | C2          | C (Chrominance) input number 2 for S-Video systems.  |
| 35                    | C1          | C (Chrominance) input number 1 for S-Video systems.  |
| 36                    | 4.43SC      | 4.433618 MHz SUBCARRIER OUTPUT. Phase-locked to the chroma burst signal to allow encoders to maintain proper SCH phasing.                                      |
| 37                    | FRSTIN      | For ICS use only.  |
| 38                    | AVDD        | 5 Volt analog power. We strongly recommend the use of a multilayer board and a power plane.  |
| 39                    | GFF         | Inverts field 1 and field 2 of VGA sync. Normally tied HIGH.   |
| 40                    | VCOLF       | VCO LOOP FILTER CIRCUIT. External RC circuit used in VCO circuitry. See Application Notes for component values.  |
| 41                    | SYNCTHRS    | Sync threshold adjustment for video input. See Application Notes schematic.  |
| 42                    | VGAO/E      | VGA ODD/EVEN FIELD IDENTIFICATION. HIGH indicates odd numbered field, LOW indicates even numbered field.   |
| 43                    | COUT        | C (Chrominance) OUTPUT. C output for S-Video systems.  |
| 44                    | RST         | Chip reset pulse. This to be tied high through a resistor. Do not tie to the computer reset line.  |
| 45                    | YOUT        | Y (Luminance) OUTPUT. PAL video output when the PAL/SVID input is in the HIGH state. Y output for S-Video systems when the PAL/SVID input is in the LOW state. |
| 46                    | HALIGNOUT   | For ICS use only, wire to pin 62.  |
| 47                    | SYSLF       | SYSTEM CLOCK LOOP FILTER CIRCUIT. External RC circuit used in the chroma burst phase locking circuit. See Application Notes for component values.              |
| 48                    | XTALI       | 17.734475 MHz crystal circuit. See Application Notes for parts specifications and wiring diagrams.   |
| 49                    | XTALO       | 17.734475 MHz crystal circuit. See Application Notes for parts specifications and wiring diagrams.   |



## GSP600

| <u>PIN<br/>NUMBER</u> | <u>NAME</u> | <u>DESCRIPTION</u>   |
|-----------------------|-------------|--|
| 50                    | AVSS        | Analog ground. We strongly recommend the use of a multilayer board and a ground plane.   |
| 51                    | VID1/2      | Input selector. High for Y1/C1, Low for Y2/C2.   |
| 52                    | VCOOUT      | For ICS use only, do not wire.   |
| 53                    | FILTSEL     | For ICS use only, wire to pin 57.  |
| 54                    | DOTCLOCK    | Clock signal input for VGA chip.   |
| 55                    | VFF         | Inverts field 1 and field 2 of PAL sync. Normally tied HIGH.   |
| 56                    | VCR2        | LOW modifies sync characteristics to permit operation with VCR input.  |
| 57                    | VGA/PAL     | Mode identification output signal. HIGH indicates a VGA mode, LOW indicates a PAL mode.  |
| 58                    | BG          | BURST GATE PULSE. Negative polarity TTL level signal used by RGB-to-PAL encoders.  |
| 59                    | LOC/REM IN  | For ICS use only, wire to pin 13.  |
| 60                    | VGAHSYNC    | VGA HORIZONTAL SYNC. HSYNC signal from VGA chip.<br>See BIOS Interface Manual for programming details.                           |
| 61                    | VGAVSYNC    | VGA VERTICAL SYNC. VSYNC signal from VGA chip.<br>See BIOS Interface Manual for programming details.                             |
| 62                    | HALIGNIN    | For ICS use only, wire to pin 46.  |
| 63                    | PAL/SVID    | PAL/S-VIDEO. Selects between PAL and S-Video output. HIGH=PAL;<br>Low=S-Video.   |
| 64                    | VS          | VERTICAL SYNC. PAL Vsync output for RGB-to-PAL encoders.<br>Gated off during VGA modes.  |
| 65                    | 4XSC        | 4 TIMES SUBCARRIER OUTPUT. 17.734475 MHz signal phase-locked to the chroma burst signal.   |
| 66                    | PCLK        | PCLK from VGA chip.  |
| 67                    | DATAOUT     | TTL level output. This reads data during lines 10-20 and outputs it as a digital signal. For use in time code applications.      |
| 68                    | SCH         | SCH PULSE. Positive polarity TTL level signal to distinguish between fields 1 and 3 or 2 and 4. Not necessary for most encoders. |



## BIOS Programming Example

BIOS support is currently available from Tseng Labs, Oak Technology, Trident Microsystems, S3, and NCR. Other VGA manufacturers have support programs underway. If you use one of these VGA controllers that have completed BIOS support, you can ignore this section. The following information may be helpful to VGA manufacturers and software developers. These tables represent register settings one particular VGA controller. Others are listed in the BIOS Interface Manual. This particular controller does not interlace text modes and uses an 8 x 8 font for modes 0, 1, 2, 3, and 7. The horizontal registers are adjusted to produce underscan for text modes and overscan for graphics modes.

### Horizontal CRTC Registers

| CRTC INDEX | CRTC REGISTER | Modes:<br>00, 01, 04, 05, 0D | Modes:<br>02, 03, 06, 07, 0E, 0F, 10 | Modes:<br>11, 12, 13 |
|------------|---------------|------------------------------|--------------------------------------|----------------------|
| 00         | HT            | 35                           | 6B                                   | 66                   |
| 01         | HDE           | 27                           | 4F                                   | 4F                   |
| 02         | SHB           | 2A                           | 53                                   | 52                   |
| 03         | EHB           | 96                           | 8B                                   | 87                   |
| 04         | SHR           | 30                           | 5B                                   | 58                   |
| 05         | EHR           | 92                           | 83                                   | 80                   |

### Vertical CRTC Registers

| CRTC INDEX | CRTC REGISTER | 200 Line Modes:<br>(Non-Interlaced)<br>00, 01, 02, 03, 07, 04,<br>05, 06, 0D, 0E, 13 | 350 Line Modes:<br>(Interlaced)<br>0F, 10 | 480 Line Modes:<br>(Interlaced)<br>12, 13 |
|------------|---------------|--|---|---|
| 06         | VT            | 05   | 05  | 05  |
| 07         | OVERFLOW      | 11   | 11  | 11  |
| 10         | VRS           | E0   | D3  | F4  |
| 11         | VRE           | 84   | 87  | 88  |
| 12         | VDE           | C7   | AE  | EF  |
| 15         | SVB           | DC   | CF  | F0  |
| 16         | EVB           | F2   | E5  | 06  |

Note: The MSB of the MSL register (INDEX 09) must be turned OFF in 200 line NTSC modes. When using an 8 x 8 font for text (modes 00, 01, 02, 03, 07) the 4 LSB of this register will change from F to 7.

### Miscellaneous Output Register

| NTSC mode          | Color Modes:<br>00, 01, 02, 03, 04, 05, 06,<br>0D, 0E, 10, 11, 12, 13 | Monochrome Modes:<br>07, 0F |
|--------------------|---|-----------------------------|
| Genlock (GL)       | 23  | 22                          |
| Overlay (OV)       | 27  | 26                          |
| Video Only (VO)    | 2B  | 2A                          |
| Graphics Only (GO) | 2F  | 2E                          |

### Extended Registers

Turn OFF all DOTCLOCK/2 bits.

The diagram illustrates the timing of the horizontal sync interval. The top part shows a standard sync pulse of 4.7uS followed by a blanking interval of 12uS. The bottom part shows a sync pulse followed by a blanking interval. Labels include 'Safe Action Area', 'Safe Title Area', 'Horizontal Display End', 'Horizontal Total', 'Sync', and 'Blanking'.

The figure displays three sets of timing diagrams for PAL, VGA, and VGA signals, separated by vertical lines. Each set includes three traces: PAL sync (black bars), VGA Hsync (black bars), and VGA Vsync (black bars). The diagrams are labeled with line numbers and frame numbers.

**Section 1 (Top):** PAL sync (lines 197-208, 219-222), VGA Hsync (lines 197-208, 219-222), VGA Vsync (lines 197-208, 219-222).

**Section 2 (Middle):** PAL sync (lines 624-625, 1-13), VGA Hsync (lines 223-238), VGA Vsync (lines 223-238).

**Section 3 (Bottom):** PAL sync (lines 260-263, 1-27), VGA Hsync (lines 239-245, 261-266), VGA Vsync (lines 239-245, 261-266).





## Electrical Specifications

Operating temperature range 0°C to 70°C

## Electrical Characteristics

| PARAMETER                    | SYMBOL                | MIN | TYP | MAX | UNITS |
|------------------------------|-----------------------|-----|-----|-----|-------|
| Analog Supply                | AVDD                  | 4.5 | 5.0 | 5.5 | Volts |
| Digital Supply               | DVDD                  | 4.5 | 5.0 | 5.5 | Volts |
| Operating Current - VGA Mode | I <sub>DD</sub> (VGA) |     | 35  |     | mA    |
| Operating Current - PAL Mode | I <sub>DD</sub> (PAL) |     | 50  |     | mA    |

## Input Signals

| SIGNAL TITLE | PIN # | TYPICAL VALUE      | OPERATING CONDITIONS                        |
|--------------|-------|--------------------|---|
| Y1           | 33    | 1 V <sub>p-p</sub> | 75 Ohm load                                 |
| C1           | 35    | 1 V <sub>p-p</sub> | 75 Ohm load                                 |
| Y2           | 32    | 1 V <sub>p-p</sub> | 75 Ohm load                                 |
| C2           | 34    | 1 V <sub>p-p</sub> | 75 Ohm load                                 |
| VID1/2       | 51    | TTL/CMOS           | High = Y1,C1; Low = Y2,C2                   |
| PAL/SVID     | 63    | TTL/CMOS           | High = PAL; Low = S-Video                   |
| VGAVSYNC     | 61    | TTL/CMOS           | Positive polarity                           |
| VGAHSYNC     | 60    | TTL/CMOS           | Positive polarity                           |
| FS0-5        | 28-23 | TTL/CMOS           | Address/mode select                         |
| CKEY         | 7     | TTL/CMOS           | High = RGB; Low = PAL                       |
| PCLK         | 66    | TTL/CMOS           | Pixel (DAC) Clock from VGA                  |
| I/ES         | 12    | TTL/CMOS           | High = Internal sync<br>Low = External sync |
| DATAIN       | 4     | TTL/CMOS           | Active during DATAFRAME                     |
| CLAMPLEV     | 31    | 1-1.5 V            |   |
| SYNCTHRS     | 41    | CLAMPLEV +0.1 V    |   |
| VLE          | 1     | TTL/CMOS           | Tie to V <sub>DD</sub> through resistor     |
| RST/         | 44    | TTL/CMOS           | Tie to V <sub>DD</sub> through resistor     |



## Output Signals

| SIGNAL TITLE | PIN# | TYPICAL VALUE     | OPERATING CONDITIONS                         |
|--------------|------|-------------------|--|
| VSYNOUT      | 9    | TTL               | Positive polarity during PAL modes           |
| HSYNOUT      | 18   | TTL               | Composite sync during PAL modes              |
| VS           | 64   | 1V <sub>P-P</sub> | Positive polarity                            |
| HS           | 16   | 1V <sub>P-P</sub> | Positive polarity                            |
| CS           | 6    | 1V <sub>P-P</sub> | Positive polarity                            |
| DOTCLOCK     | 54   | TTL               |  |
| YOUT         | 45   | 1V <sub>P-P</sub> | 75 Ohm load                                  |
| COUT         | 43   | 1V <sub>P-P</sub> | 75 Ohm load                                  |
| 4.43SC       | 36   | TTL               | 4.433618 MHz                                 |
| 4XSC         | 65   | TTL               | 17.734475 MHz                                |
| LOC/REM      | 13   | TTL               | High = local; Low = remote                   |
| OVENABLE     | 11   | TTL               | High = PAL; Low = RGB                        |
| VGA/PAL      | 57   | TTL               | High = VGA; Low = PAL                        |
| CB           | 25   | TTL               | Positive polarity                            |
| ODD/EVEN     | 2    | TTL               | High = odd field; Low = even field           |
| VGAO/E       | 42   | TTL               | High = VGA odd field<br>Low = VGA even field |
| BG/          | 58   | TTL               | Negative polarity                            |
| FP/          | 3    | TTL               | Negative polarity                            |
| SCH          | 68   | TTL               | Positive polarity                            |
| DATAFRAME    | 10   | TTL               | Lines 10-20                                  |
| DATAOUT      | 67   | TTL               | Active during DATAFRAME                      |



## GSP600

### Dot Clock Selection

The following charts represent two of the many dot clock frequency selection tables supported by **GSP600**. See the BIOS manual or contact ICS applications engineering for additional information.

| FREQUENCY (MHz) | FS5 | FS4,FS3,FS2 | FS1 | FS0 |
|-----------------|-----|-------------|-----|-----|
| 50.350          | 0   | 1           | 0   | 0   |
| 56.644          | 0   | 1           | 0   | 1   |
| 65.028          | 0   | 1           | 1   | 0   |
| 72.000          | 0   | 1           | 1   | 1   |
| 75.000          | 1   | 0           | 0   | 0   |
| 80.000          | 1   | 0           | 0   | 1   |
| 89.800          | 1   | 0           | 1   | 0   |
| 110.000         | 1   | 0           | 1   | 1   |
| GenLock         | 1   | 1           | 0   | 0   |
| OVerlay         | 1   | 1           | 0   | 1   |
| Video Only      | 1   | 1           | 1   | 0   |
| Graphics Only   | 1   | 1           | 1   | 1   |

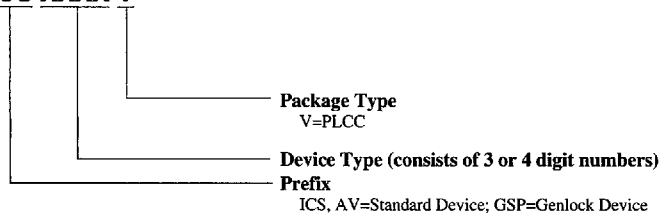
| FREQUENCY (MHz) | FS5,FS3 | FS4, FS2 | FS1 | FS0 |
|-----------------|---------|----------|-----|-----|
| 25.175          | 0       | 1        | 0   | 0   |
| 28.322          | 0       | 1        | 0   | 1   |
| 40.000          | 0       | 1        | 1   | 0   |
| 44.900          | 0       | 1        | 1   | 1   |
| GenLock         | 1       | 1        | 0   | 0   |
| OVerlay         | 1       | 1        | 0   | 1   |
| Video Only      | 1       | 1        | 1   | 0   |
| Graphics Only   | 1       | 1        | 1   | 1   |

### Ordering Information

#### GSP600V

Example:

ICS XXXX V



# GSP600 Frequently Asked Technical Questions.

## 1. What will the GSP600 do for me?

The GSP600 adjusts the timing of a VGA controller to conform to PAL (television) specifications. The GSP600 accepts direct video input from video cameras, videodisc players or other video sources and will synchronize (genlock) a VGA controller to either the external video input or an internal PAL sync generator. The GSP600 also contains a dot clock generator to eliminate the need for crystal oscillators or other dot clock generators.

## 2. How does the GSP600 differ from other genlock devices?

Other genlock devices, such as the Motorola MC1378, are very effective at genlocking two PAL signals together and are generally used in consumer electronics products such as video window-in-a-window devices. The GSP600 is specifically designed to genlock a computer graphics controller to PAL video and overcomes all of the incompatibilities between VGA and PAL. Additionally, the GSP600 contains an PAL sync generator and maintains chrominance phase lock in local modes. This allows the GSP600 to maintain PAL timing without an external video input. Furthermore, the sync separator circuit of the GSP600 is designed to satisfy the low jitter tolerances demanded by discriminating VGA customers.

## 3. Isn't genlock simply a phased-lock loop?

Phase locking two similar signals is fairly straightforward as long as phase jitter is not critical. As an example, ICS is one of the few companies able to successfully build phase-locked loop dot clock generators with low enough phase jitter for computer graphics display. Additionally, the differences between VGA and PAL signals further complicate the genlock procedure. The GSP600 has patents applied for for the most advanced computer video genlock methods in the industry. These methods assure you of the highest possible quality product.

## 4. Most Genlock and Overlay products have a lot of discrete components with trimmer capacitors and potentiometers. All these adjustments can become very expensive in a mass production environment. How much external circuitry does the GSP600 require?

Although the GSP600 can be run with no trimmer capacitors or potentiometers, one trimmer capacitor should be used to meet the PAL frequency tolerance of the chroma burst. This is a free running frequency and is very simple (and fast) to adjust. Additionally, the GSP600 uses high speed digital circuitry to eliminate virtually all discrete components. Only a few external components are needed for full operation.

## 5. Do I need an RGB-to-PAL encoder with the GSP600?

Yes, an external RGB-to-PAL encoder is needed. The encoder must be matched to the target audience. The GSP600 can be used under broadcast television scrutiny and most broadcast video equipment perform the encoding entirely with discrete components. As this may prove too costly and/or may use too much board space, the GSP600 contains all of the necessary signals to drive virtually any encoder. The GSP600's generous supply of timing signals will also drive external circuitry to turn off the encoder for laptop applications.

## 6. Why do I need the GSP600. Can't I program a VGA controller for PAL sync and just drive an RGB-to-PAL encoder?

PAL sync contains equalizing pulses, blanking signals and pulse widths that are impossible to create under normal VGA control. Although marginal display quality is achievable on a television without adhering to the PAL standard, compatibility with other PAL equipment is compromised. As an example, depending on which edge of horizontal sync the monitor triggers on will determine how far an incorrect width horizontal sync pulse will skew the screen. Additionally, it becomes virtually impossible to assure proper chroma burst (SCH) phasing. The GSP600 sync generator meets or exceeds all PAL broadcast standards for timing accuracy assuring you of maximum compatibility and ultimate quality.

## **7. National sells a sync separator for less than \$2 while the Brooktree part costs over \$50. What is the difference and how does the sync separator in the GSP600 compare?**

The sync separation circuitry in the National part is a simple diode clamp. Although this may be adequate for driving a picture tube, the lack of noise and jitter immunity make it unsuitable for genlock applications. Additionally, the analog vertical sync detection circuit of these type of devices will not accurately track a VCR signal. The Brooktree device represents a mixed-mode approach to sync separation. By utilizing a fast analog circuitry coupled with high speed digital logic, noise and jitter immunity can be optimized. The GSP600 also uses a mixed mode approach specifically optimized for genlock operation yet the incorporation of a sync generator allows signal analysis not possible with other devices.

## **8. Is the GSP600 compatible with any VGA controller?**

VGA controllers need to have two features to work with the GSP600. First, they need to be able to interlace - if your controller can display 1024 x 768 resolution, then it can probably interlace (the additional 256K memory is not necessary). Second, the controller must have at least three clock select lines for external dot clock generator support. Virtually all current VGA controllers have this feature. Check with your VGA controller manufacturer or ICS if you are unsure.

## **9. How do I turn the PAL on and off and control it?**

The GSP600 uses the three clock select lines to support 4 VGA clocks and 4 PAL modes. The VGA clocks are available in 7 different patterns (i.e. 25.175, 28.322, 40.000, 65.000 is one pattern). The 4 PAL modes are Genlock, Overlay, Graphics Only, and Video Only. The selection between any PAL mode or between PAL and VGA is done entirely under BIOS or software control.

## **10. Why did you incorporate a dot clock generator in the GSP600?**

The GSP600 works by modifying the dot clock input for the VGA controller. It essentially is a dot clock generator designed for PAL genlock. The dot clock generator is not so much of an extra feature as it is a subset of the genlock design. Consequently, this unity design assures you of a reliable glitch-free solution.

## **11. When the GSP600 displays an Overlay, how do I determine which part of the screen displays graphics and which is VGA?**

The GSP600 uses a technique called Color-Key to determine where to display the external video. This Color-Key color is based on the VGA color number. Therefore, no colors are actually lost. As an example, the background color is always Color 0. When Color-Keying on Color 0, the screen will appear to have a background of the external video. The actual color that the VGA assigns to Color 0 does not matter. Any of the 256 color numbers can be assigned to be a Color-Key. Although the GSP600 modifies the Color-Key input, the Color-Key selection is done by an external 8 bit digital compare.

## **12. Why is the Color-Key selection external to the GSP600?**

Color-Key selection is done with an 8 bit compare of the digital RGB signals with a preassigned byte. The digital RGB data comes from the VGA controller and the preassigned byte normally comes from the IBM bus via a port selection. The output of this comparison is fed into the CKEY (Color-Key) input of the GSP600. Although this Color-Key method will satisfy 95% of all customers, the external design allows other schemes with multiple or different comparison options. Additionally, since all of these signals are already available inside the VGA controller, many manufacturers have announced plans to incorporate the Color-Key function inside the VGA controller.

## **13. What about NTSC and/or SECAM compatibility?**

ICS has an NTSC version of the GSP600 (the GSP500). In its current implementation, it is pin compatible with the GSP600 but require different values for the discrete components and will also need a different crystal oscillator. Although a SECAM version is technically possible, due to the uncertain market potential product development is not currently underway.

## **14. Can I look forward to a combination PAL and NTSC product?**

Unfortunately, the amount of circuitry common to both a PAL and an NTSC version is minimal. Separate versions are currently the lowest cost solution. Although the crystal frequency, some discrete components and the Bios would have to change, the same board layout could support both standards by simply changing the parts list.

## **15. Does the GSP600 accept multiple video inputs? What about an S-Video input?**

The GSP600 has two independent video inputs. Either input can be used or they can both be disabled. Either input can be wired to accept either S-Video or PAL. Selection between the two inputs is performed under hardware control.

## **16. Why doesn't the GSP600 incorporate audio?**

The PAL and S-Video baseband signals do not have a provision for audio. This means that the video and audio signals are completely separate signals at all times. ICS offers audio products for the multimedia market that can be incorporated into the design but allows the designer maximum flexibility by keeping them separate products.

## **17. Can I use the GSP600 with an RF modulator?**

Yes, but the quality of the image may suffer. When PAL is modulated up to RF frequencies, audio is modulated onto a 4.5 MHz carrier and the video is limited to a maximum frequency of 4.2 MHz. Although 4.2 MHz may be sufficient for moving images it can be limiting for high resolution computer graphics. This problem is magnified because the majority of RF modulators are very low quality devices. Additionally, even if a high quality RF modulation is obtained, the signal may still be degraded by the RF demodulator inside the television set. ICS does recognize that these limitations may be outweighed by the user-friendliness and compatibility of the RF standard. High quality RF modulators are available and the GSP600 does have the necessary signals for support but these issues should be carefully weighed before implementation.

## **18. Can the GSP600 display PAL video on my VGA screen?**

No, in order to display PAL video at 31.25 KHz, it is necessary to convert PAL into component form, digitize it in real time, and store at least one frame of video. Although technology exists to accomplish this, the price-to-performance ratio of these products is too high for mass market acceptance at this time.

## **19. Is there any question that I forgot to ask?**

*Yes, when I use a graphics program, I find the borders very distracting yet I need the borders in text modes to insure that I can read the DOS prompt. Can the GSP600 help me with this problem? The GSP600 has the ability to adjust the width of the screen totally under Bios control. This means that you can have limited overscan in mode 13, minor underscan in mode 3 and generous overscan in mode 12. Software drivers can even be written to dynamically change the screen width with the cursor keys.*

## **20. Does this mean I can change the height of the screen also?**

PAL has a fixed number of lines. In order to change the vertical size, the screen data must be compressed or expanded into fewer or greater lines. This can be accomplished in a text mode by changing the font size or in a graphics mode with linear interpolation. The GSP600 always maintains an exact one-to-one correlation between the PAL and VGA line position and therefore does not support vertical sizing.

## **21. Where do I get a development kit for the GSP600?**

Call ICS at (800) 220-3366 for more information. We will put you in touch with a local rep. who will be more than happy to supply you with a full GSP600 development kit. The ICS full service support organization is always ready to help you with the latest in Multimedia solutions.