DEC 8 1992

National Semiconductor

NMD1024X1
1MX1 Bit CMOS Dynamic RAM with Fast Page Mode

Data Sheet

May 1992

FEATURES

- Performance range:

NSC Part Number	t_{RAC}	t_{CAC}	t_{RC}
NMD1024X1-60	60ns	15ns	110ns
NMD1024X1-70	70ns	20ns	130ns
NMD1024X1-80	80ns	20ns	150ns

- Fast Page Mode operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- TTL compatible input and output
- Single +5V±10% power supply
- Low power dissipation
  - I_{CC5}: 200µA
  - I_{CC7}: 200µA (Battery Backup Mode)
- 512 cycles/64ms refresh
- 256Kx4 fast test mode
- JEDEC standard pinout
- Available in Plastic SOJ package
- Consult Marketing for availability of the DIP, ZIP and TSOP packages

GENERAL DESCRIPTION

The National Semiconductor NMD1024X1 is a high speed CMOS 1,048,576 x 1 Dynamic Random Access Memory. It's design is optimized for high performance applications such as minicomputers, graphics and high performance microprocessor computers.

The NMD1024X1 features Fast Page Mode operation which allows high speed random access of memory cells within the same row. CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only Refresh. All inputs and output are fully TTL compatible.

The NMD1024X1 is fabricated using an advanced CMOS process.

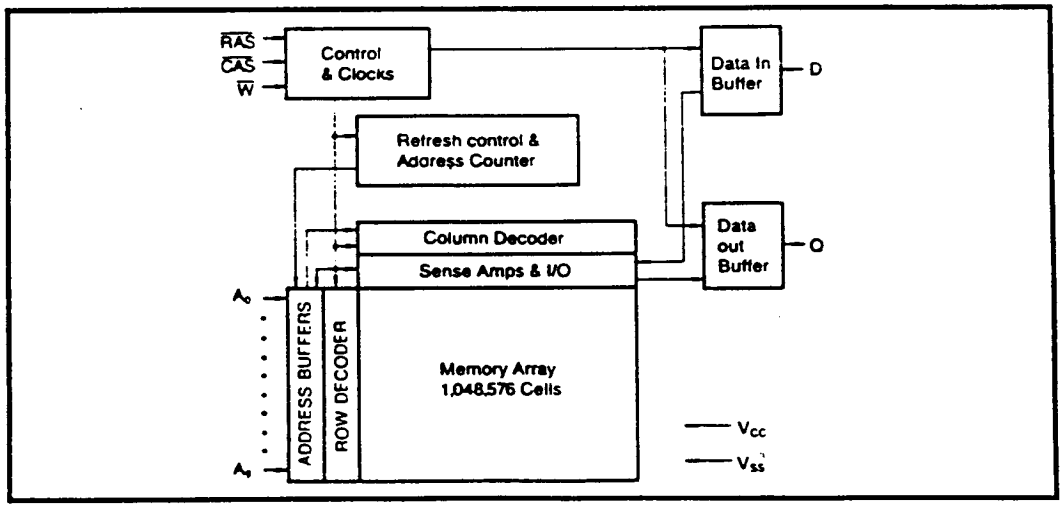


Figure 1. 1MX1 DRAM Block Diagram

page 1

PIN CONFIGURATIONS (Top Views)

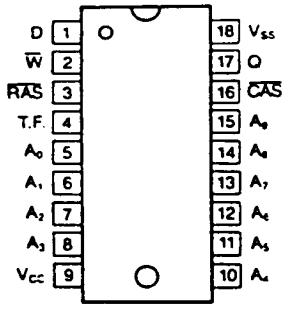


Figure 1. DIP Package

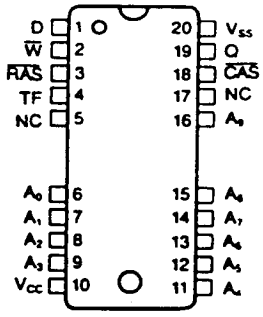


Figure 2. SOJ Package

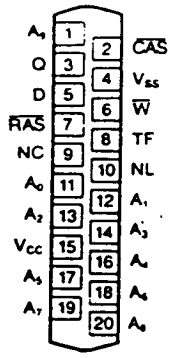


Figure 3. ZIP Package

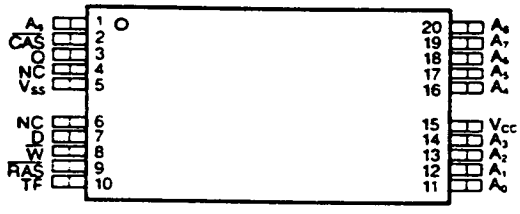


Figure 4. TSOP II (Forward)

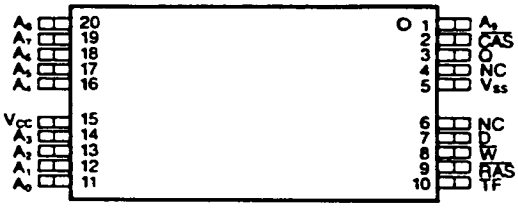


Figure 5. TSOP II (Reverse)

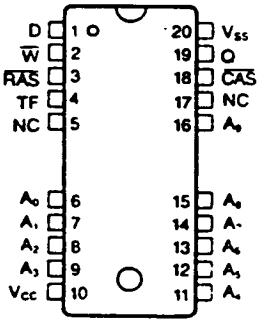


Figure 6. TSOP I (Forward)

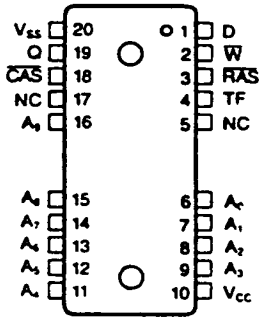


Figure 7. TSOP I (Reverse)

PIN DESCRIPTION	
Pin Name	**Pin Function**
A_0-A_9	Address Inputs
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
TF	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection
NL	No Lead

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	600	mW
Short Circuit Output Current	I_{OS}	50	mA

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, TA=0 to 70 °C)

Parameter	Symbol	Min	Type	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

DC AND OPERATING CHARACTERTISTICS (°C≤Ta≤70 °C, VCC=5.0V ± 10%)

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Operating Current[2] ($\overline{RAS}$, $\overline{CAS}$, Address Cycling @ t_{RC}=min.)	NMD1024X1-60	I_{CC1}	-	70	mA
	NMD1024X1-70		-	65	mA
	NMD1024X1-80		-	60	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	-	2	mA
RAS-Only Refresh Current[2] ($\overline{CAS}$=V_{IH}, $\overline{RAS}$, Address Cycling @ t_{RC}=min.)	NMD1024X1-60	I_{CC3}	-	70	mA
	NMD1024X1-70		-	65	mA
	NMD1024X1-80		-	60	mA
Fast Page Mode Current[2] ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	NMD1024X1-60	I_{CC4}	-	55	mA
	NMD1024X1-70		-	50	mA
	NMD1024X1-80		-	45	mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		I_{CC5}	-	200	µA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current[2] ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC}=min.)	NMD1024X1-60	I_{CC6}	-	70	mA
	NMD1024X1-70		-	65	mA
	NMD1024X1-80		-	60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode ($\overline{CAS}$=$\overline{CAS}$-Before-$\overline{RAS}$ Cycling or 0.2V, W = V_{CC}-0.2V or 0.2V, A_0 - A_9 = V_{CC}-0.2V or 0.2V, D_{IN} =V_{CC}-0.2, 0.2V or OPEN: t_{RC} = 125µS, t_{RAS} = t_{RAS} min. -1µS)	NMD1024X1-60 NMD1024X1-70 NMD1024X1-80	I_{CC7}	-	200	µA
Input Leakage Current (Any input 0≤V_{IN}≤6.5V, all other pins not under test=0 volts)		I_{IL}	-10	10	µA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}<5.5V)		I_{OL}	-10	10	µA
Output High Voltage Level (I_{OH}=-5mA)		V_{OH}	2.4	-	V
Output Low Voltage Level (I_{OL}=4.2mA)		V_{OL}	-	0.4	V

NOTES: 1. Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified value are obtained with the output open. I_{CC} is specified as average current. I_{CC1}, I_{CC3} Address can be changed maximum two times while $\overline{RAS}$=V_{IL}. I_{CC4} Address can be changed maximum once while $\overline{CAS}$=V_{IH}.

CAPACITANCE (T_A=25 °C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (D)	C_{IN1}	-	5	pF
Input Capacitance (A_0-A_9)	C_{IN2}	-	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$,$\overline{W}$,)	C_{IN3}	-	7	pF
Output Capacitance (Q)	C_{OUT}	-	7	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, V_{CC}=5.0V ± 10%, See notes 3,4)

Standard Operation	Symbol	NMD1024X1-60		NMD1024X1-70		NMD1024X1-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		150		ns	
Read-modify write cycle time	t_{RWC}	130		150		170		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70		80	ns	5,6,13
Access time from $\overline{CAS}$	t_{CAC}		15		20		20	ns	5,6,7
Access time from column address	t_{AA}		30		35		40	ns	5,12
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	5
Output buffer turn-off delay	t_{OFF}	0	15	0	20	0	20	ns	9
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	4
$\overline{RAS}$ precharge time	t_{RP}	40		50		60		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	10,000	20	10,000	20	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	20	60	ns	6
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	15	40	ns	13
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		15		15		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30		35		40		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	11
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	11
Write command hold time	t_{WCH}	10		10		10		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	45		50		55		ns	8
Write command pulse width	t_{WP}	10		10		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		15		15		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	12

AC CHARACTERISTICS (Continued)

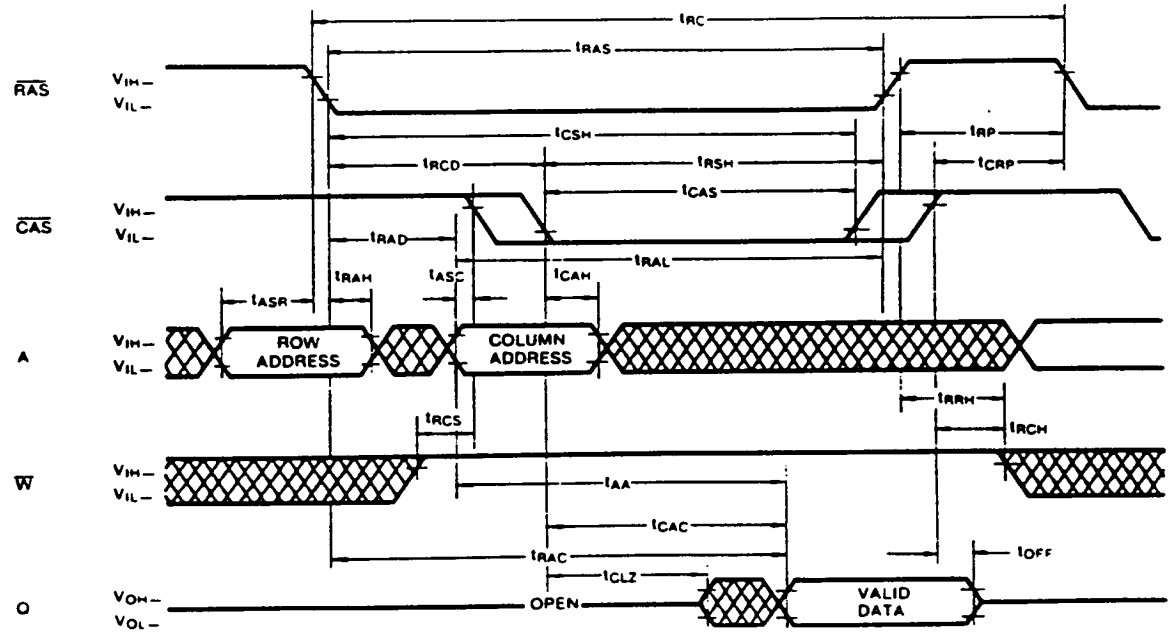
Standard Operation	Symbol	NMD1024X1-60		NMD1024X1-70		NMD1024X1-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	15		15		15		ns	12
Data-in hold referenced to $\overline{RAS}$	t_{DHR}	50		55		60		ns	8
Refresh period (512 cycles)	t_{REF}		64		64		64	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	10
$\overline{CAS}$ to $\overline{W}$ delay	t_{CWD}	15		20		20		ns	10
$\overline{RAS}$ to $\overline{W}$ delay	t_{RWD}	60		70		80		ns	10
Column address to $\overline{W}$ delay time	t_{AWD}	30		35		40		ns	10
$\overline{CAS}$ setup time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{C}$-B-$\overline{R}$ refresh)	t_{CHR}	15		15		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5		5		5		ns	
$\overline{CAS}$ precharge ($\overline{C}$-B-$\overline{R}$ counter Test)	t_{CPT}	20		25		30		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		35		40	ns	5
Fast Page mode cycle time	t_{PC}	40		45		50		ns	
Fast page mode read-modify-write	t_{PRWC}	60		60		65		ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	60	100K	70	100K	80	100K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40		45		50		ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10		10		10		ns	

NOTES:

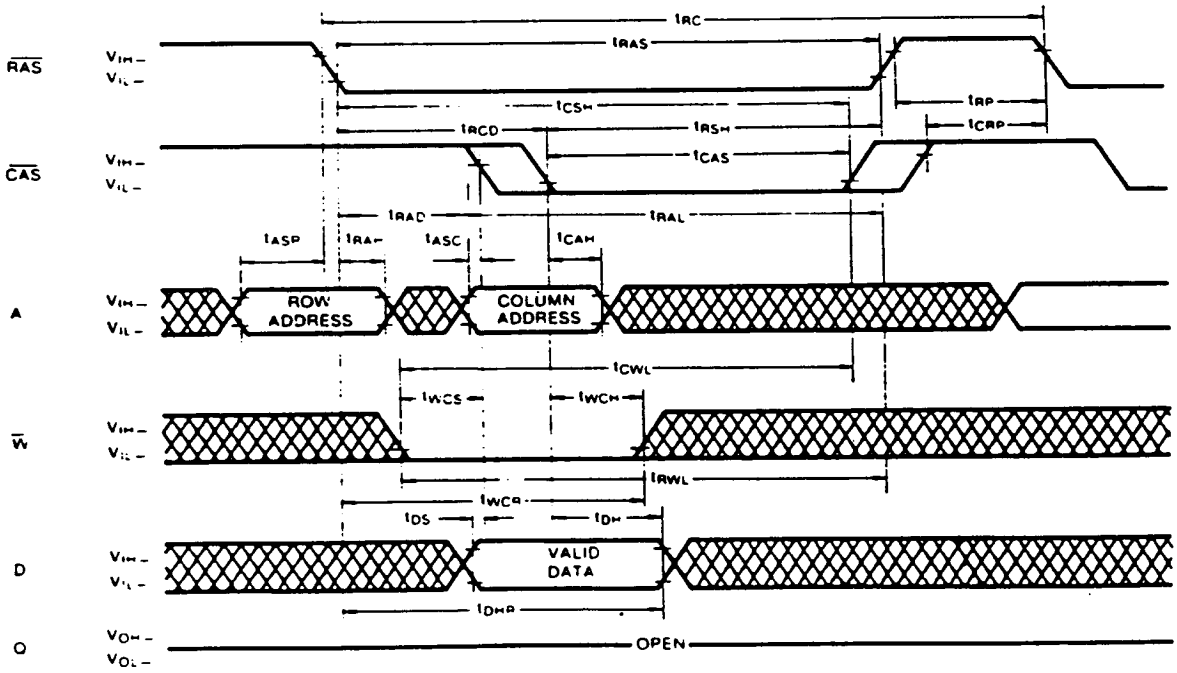
3. An initial pause of 200µs is required after powerup followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
4. $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min)}$ and $V_{IL(max)}$, and are assumed to be 5ns for all inputs.
5. Measured with a load equivalent to 2 TTL loads and 100pF.
6. Operation within the $t_{RCD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.
7. Assumes that $t_{RCD} \geq t_{RCD(max)}$.
8. t_{WCR}, t_{DHR} are referenced to $t_{RAD(max)}$.
9. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ and $t_{AWD} \geq t_{AWD(min)}$, then the cycle is a read-write cycle and the data output will contain the data read from the selected cell. In either of the above conditions are satisfied, the condition of the data out is indeterminate.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{W}$ leading edge in read-write cycles.
13. Operation within the $t_{RAD(max)}$ limit insures that $t_{RAC(max)}$ can be met. $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max)}$ limit, then access time is controlled by t_{AA}.
14. Normal operation requires the "T.F" pin to be connecte to V_{SS} or TTL logic low level or left unconnected on the printed wiring board.
15. When the "T.F" pin is connected to a defined positive voltage, the internal test function may be activated. Contact National Semiconductor for specific operational details of the "test function."
16. In a test mode read cycle, the value of t_{RAC}, t_{CAC}, t_{AA} is delayed for 3ns.

TIMING DIAGRAMS

READ CYCLE

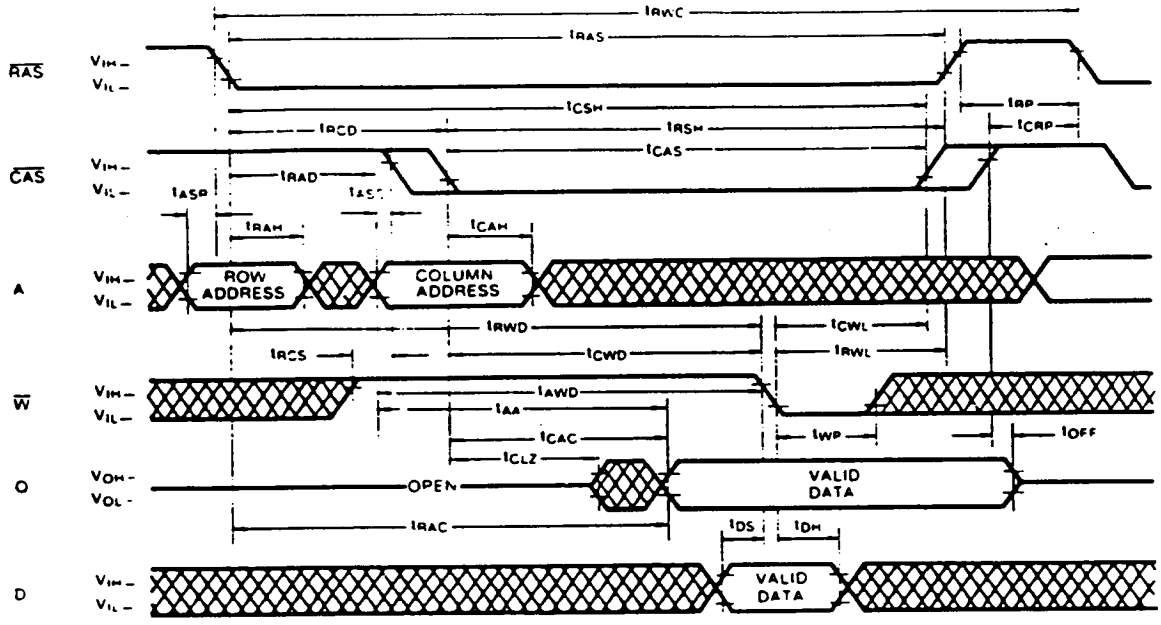


WRITE CYCLE (EARLY WRITE)



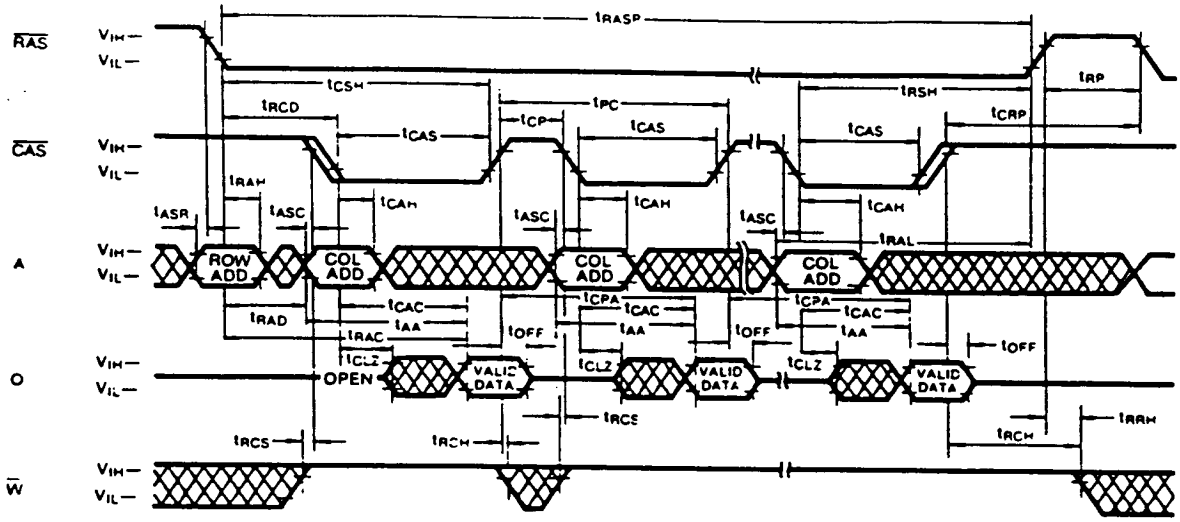
TIMING DIAGRAMS (Continued)

READ-WRITE/READ-MODIFY-WRITE CYCLE

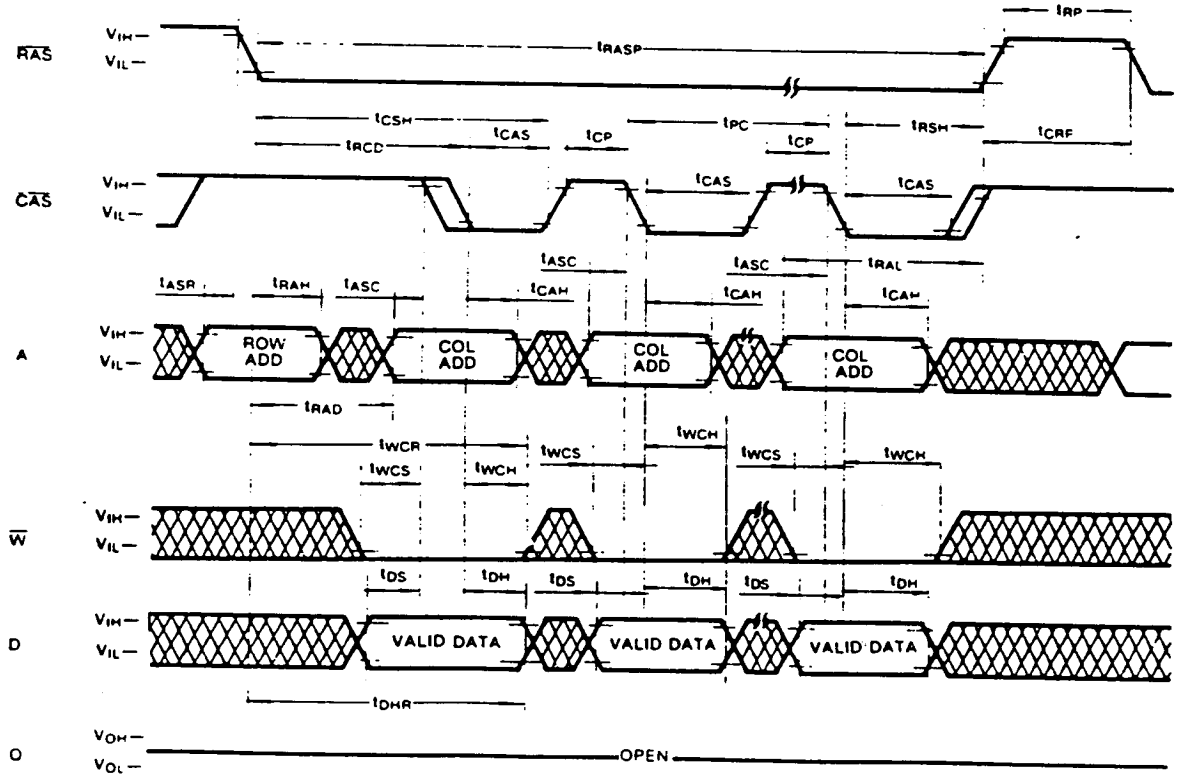


TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ CYCLE

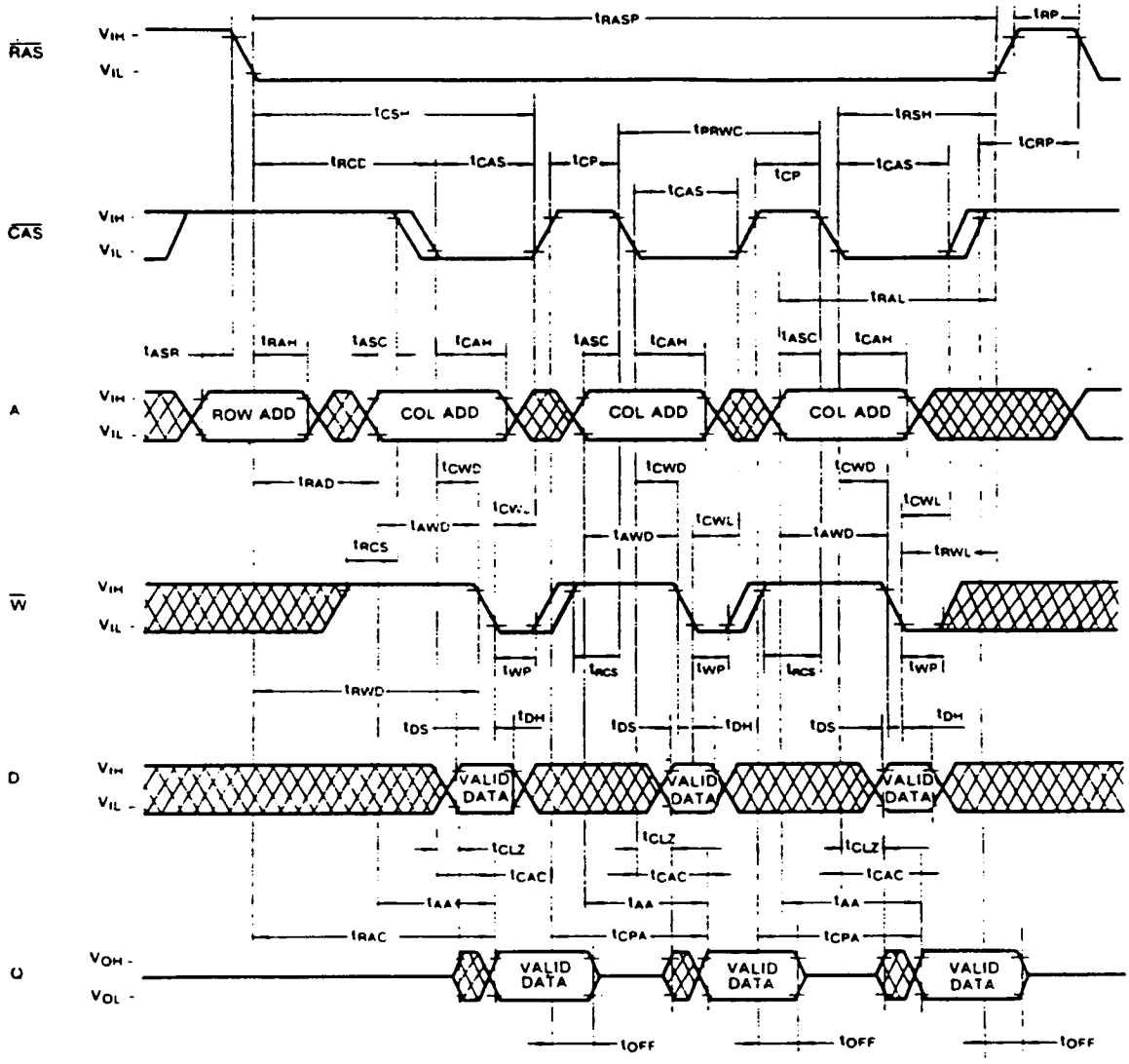


FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



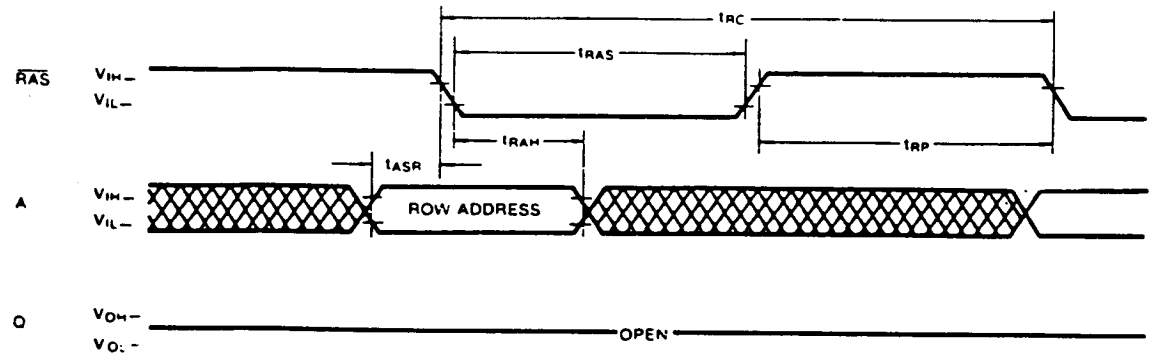
TIMING DIAGRAMS (Continued)

FAST PAGE MODE READ-MODIFY-WRITE

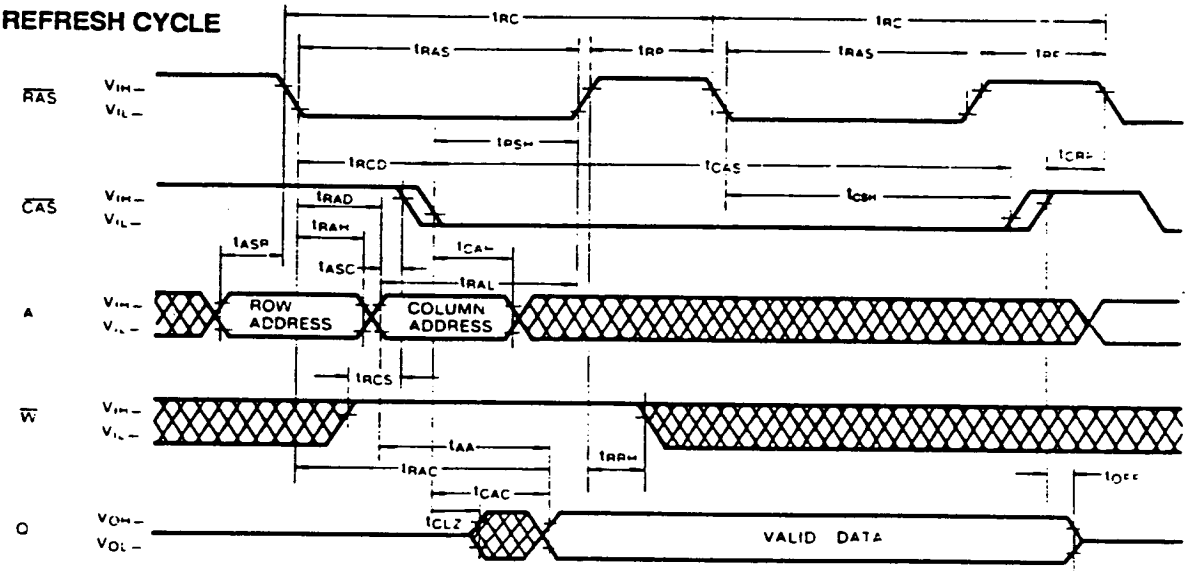


TIMING DIAGRAMS (Continued)

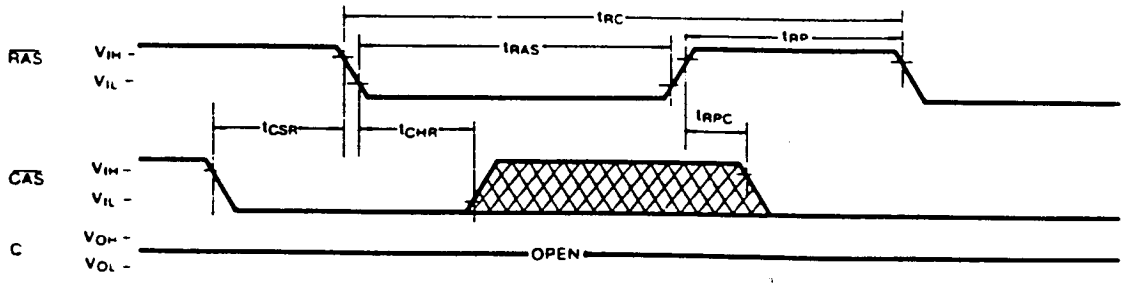
$\overline{RAS}$-ONLY REFRESH CYCLE[17]



HIDDEN REFRESH CYCLE



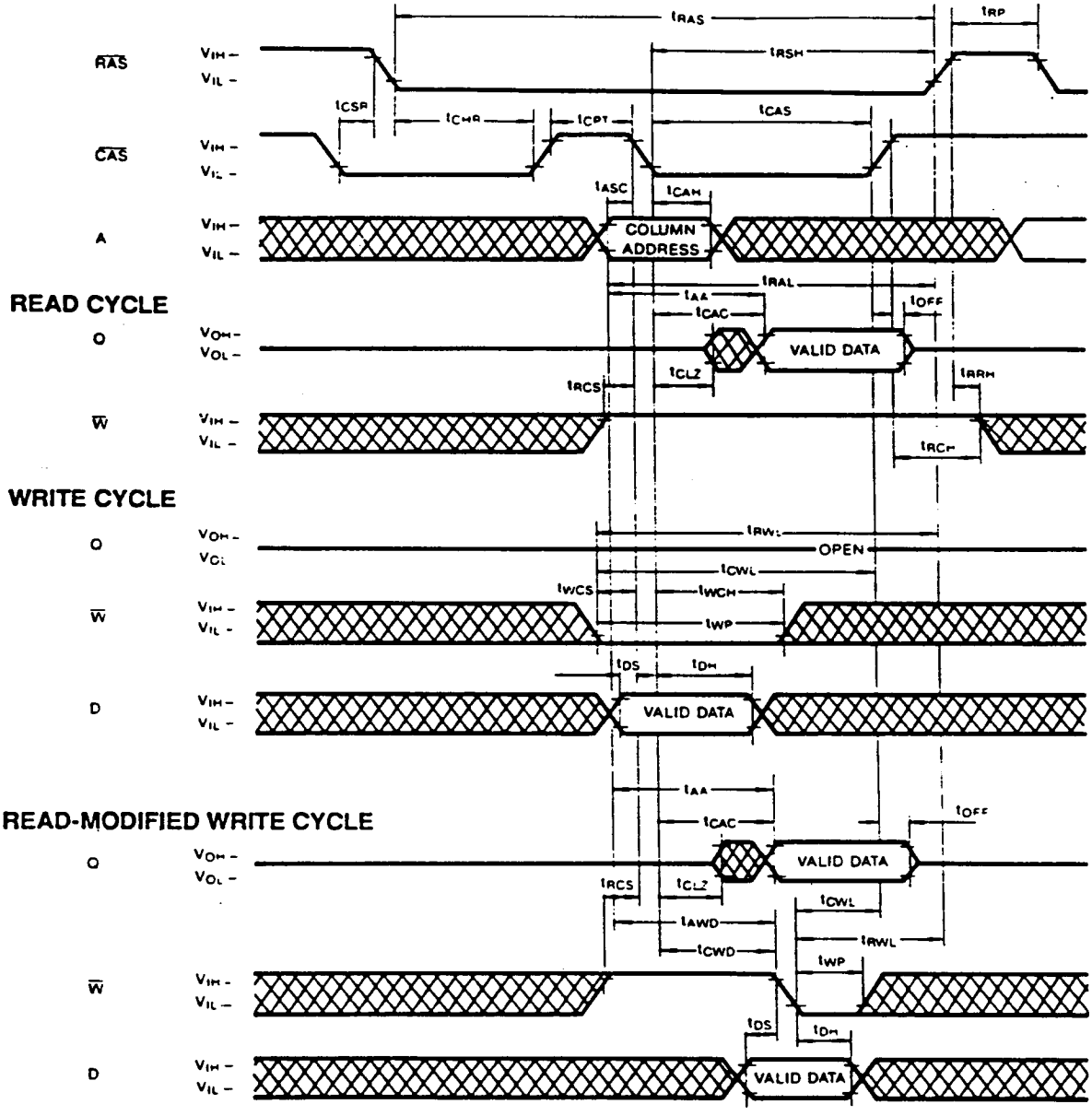
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



Note:
17. $\overline{CAS}$ = V_{IH}, $\overline{W}$, D, A_9 = Don't Care

TIMING DIAGRAMS (Continued)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE OPERATION

Device Operation

The NMD1024X1 contains 1,048,576 memory locations. Twenty address bits are required to address a particular memory location. Since the NMD1024X1 has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid row and column address inputs.

Operating of the NMD1024X1 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any NMD1024X1 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition a new cycle must not begin until satisfying the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the NMD1024X1 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{RAS}$. But the access time also depends on the falling edge of $\overline{CAS}$ and on the valid column address transition.

If $\overline{CAS}$ goes low before t_{RCD}(max), and if the column address is valid before $t_{RAD(max)}$ then the access time to valid data is specified by $t_{RAC(min)}$. However, if $\overline{CAS}$ goes low after $t_{RCD(max)}$ or if the column address becomes valid after $t_{RAD(max)}$, access is specified by t_{CAC} or t_{AA}. In order to achieve the minimum access time, $t_{RAC(min)}$, it is necessary to meet both $t_{RCD(max)}$ and $t_{RAD(max)}$.

Write

The NMD1024X1 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, Date-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing $\overline{W}$ low before $\overline{CAS}$. The data at the data input pin (D) is written the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} and t_{AWD}, are not necessarily met. The state of date-out is indeterminate since the output can be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The NMD1024X1 has a three-state output buffer which is controlled by $\overline{CAS}$. Whenever $\overline{CAS}$ is a high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameters t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the NMD1024X1 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Fast Page Mode Read, Fast Page Mode Read-Modify-Write.

Hi-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Fast Page Mode Write, CAS-before-RAS Refresh, CAS-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the NMD1024X1 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 64 ms. There are several ways to accomplish this.

DEVICE OPERATION (Continued)

$\overline{RAS}$-Only Refresh: This is the most common method of performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each 512 row addresses, (A_0-A_8). The state of address A9 is ignored during refresh.

$\overline{CAS}$-before-$\overline{RAS}$: The NMD1024X1 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The NMD1024X1 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh counter.

Other Refresh Methods: It is also possible to refresh the NMD1024X1 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the perferred method.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing seqence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. The cycle begins as a $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. Then, if $\overline{CAS}$ is brought high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled. In this mode, the row address bits A0 through A8 are supplied by the on-chip refresh counter. The A9 is set low internally.

Fast Page Mode

The NM1024X1 has Fast Page mode capability which provides high speed read, write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begns with a normal cycle. Then, while $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Power-up

If $\overline{RAS}$=V_{SS} during power-up, the NMD1024X1 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current

An initial pause of 200µs is required after power-up followed by 8 initialization cycles before proper device operaion is assured. Eight initialization cycles are also required after any 8 msec period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the NMD1024X1 inputs act like unterminated transmission lines resulting in significant overshoot and undershoot at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the NMD1024X1 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20 to 40 ohms.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMS. The impedance is minimized if all the power supply traces to all the DRAMS run both horizontally and vertiCally and are connected at each intersection or better yet if power and ground planes are used.

Decoupling

The importance of proper decoupling can not be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). It is recommended that the total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500mV.

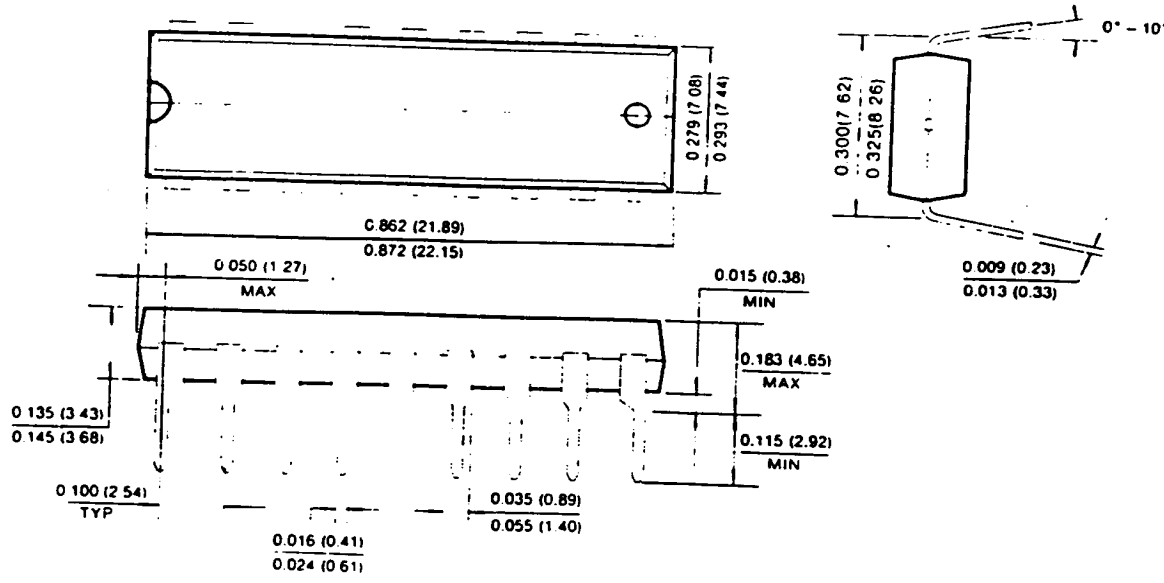
A high frequency 0.1µF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each NMD1024X1 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the NMD1024X1 and they supply much of the current used by the NMD1024X1 during cycling.

In addition, a large tantalum capacitor with a value of 47µF to 100µF should be used for bulk decoupling to recharge the 0.1µF capacitors between cycles, thereby reducing power line drop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor around the memory array.

PACKAGE DIMENSIONS (Continued)

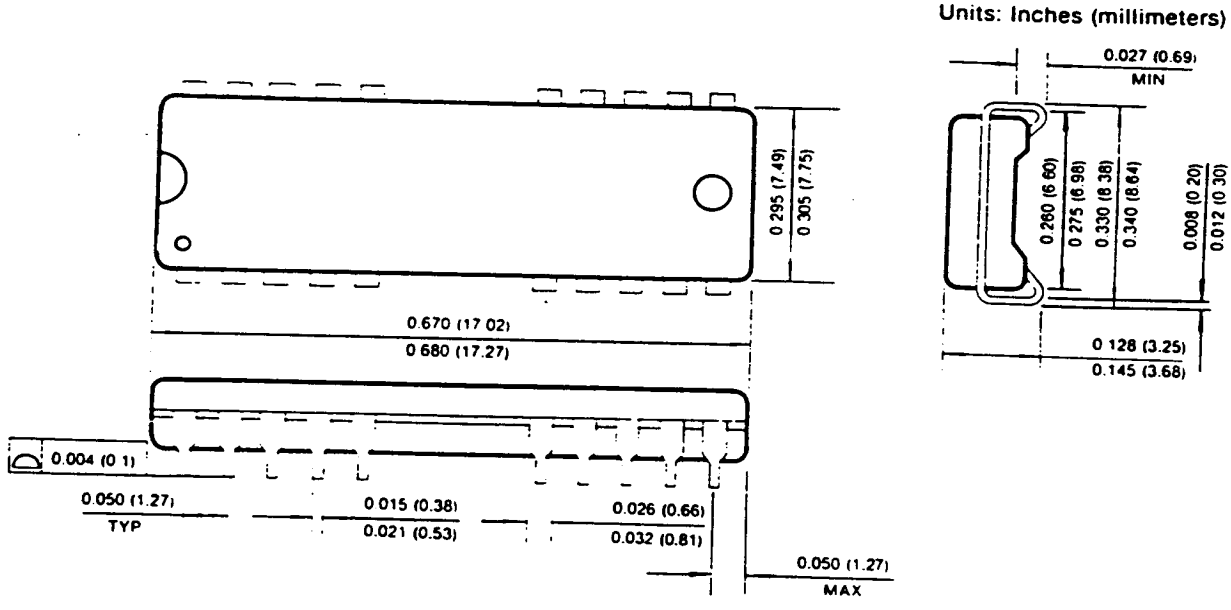
18-LEAD PLASTIC DUAL IN-LINE PACKAGE

Units: Inches (Millimeters)



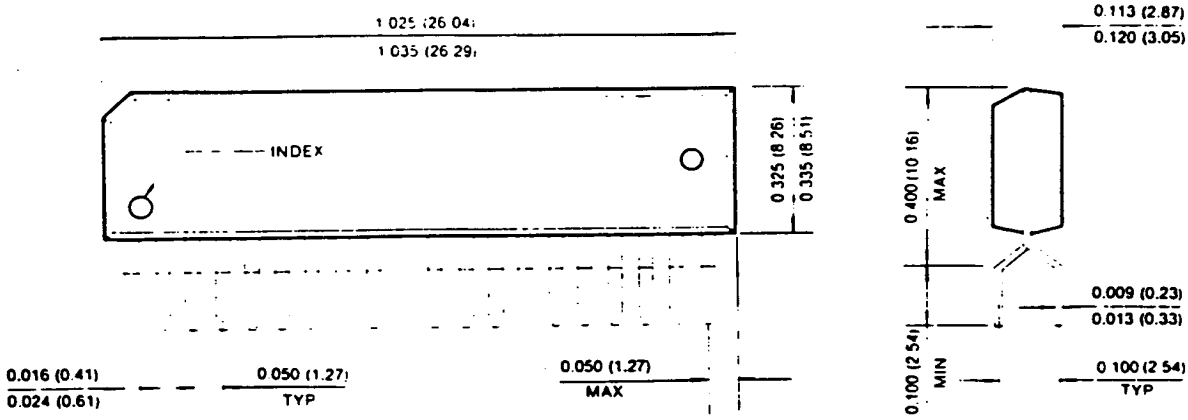
20-LEAD PLASTIC SMALL OUT-LINE J-LEAD

Units: Inches (millimeters)



PACKAGE DIMENSIONS (Continued)

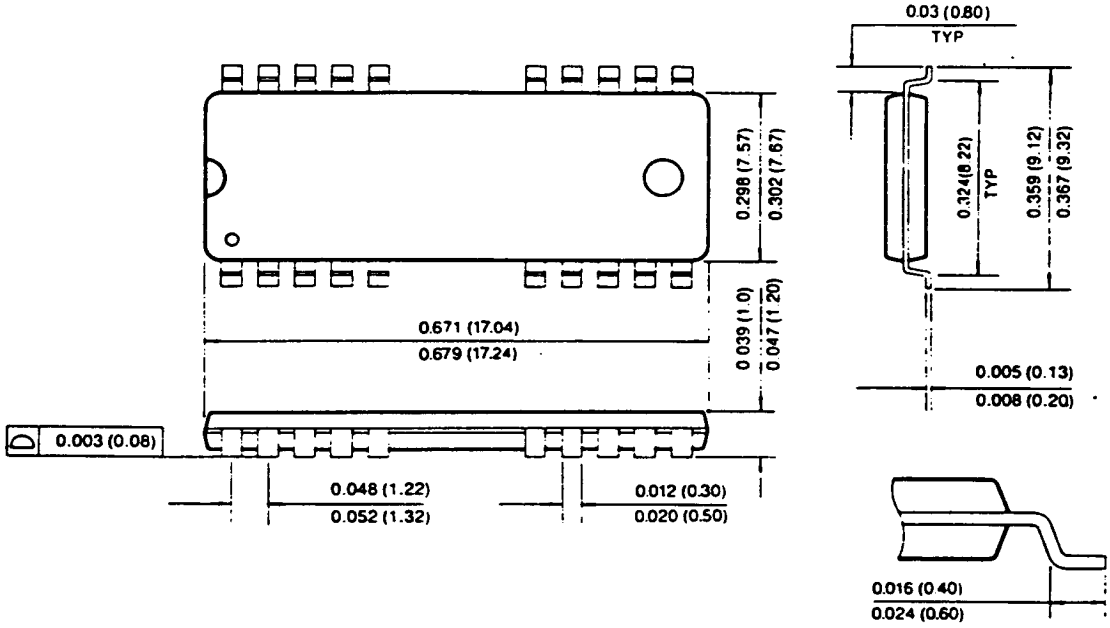
20-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE



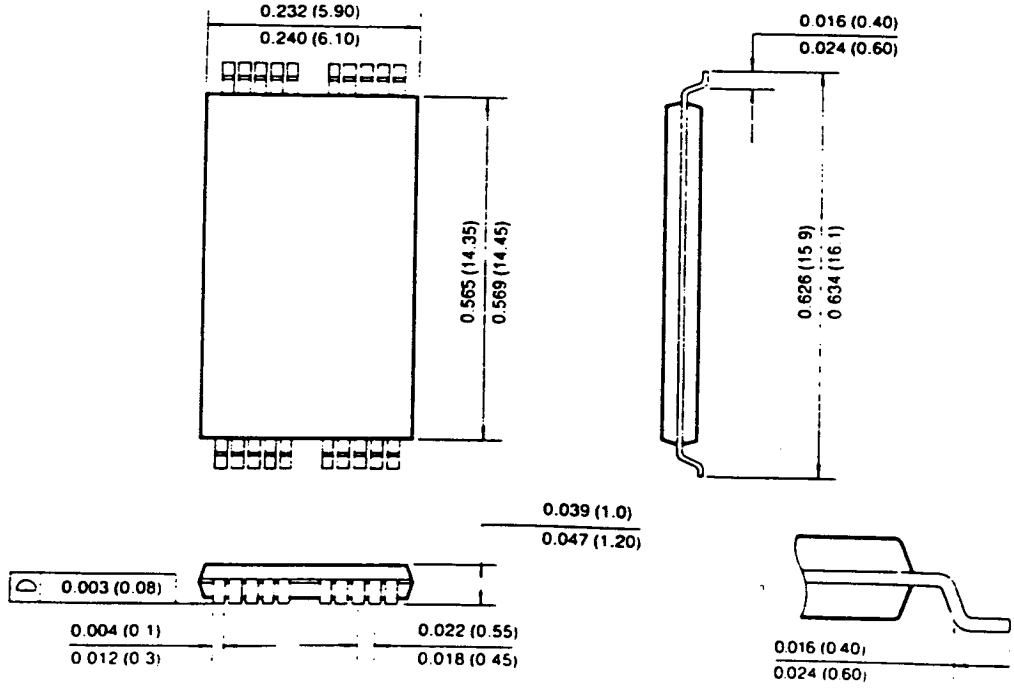
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II) (Forward and Reverse Type)

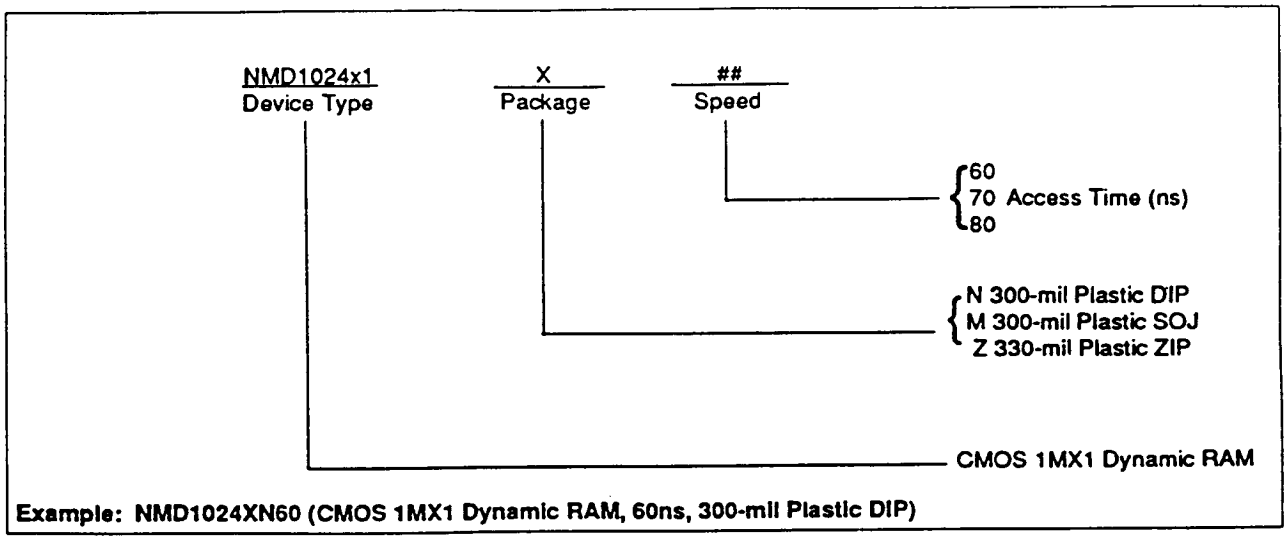
Units: Inches (millimeters)



20-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (I) (Forward and Reverse Type)



ORDERING INFORMATION



Example: NMD1024XN60 (CMOS 1MX1 Dynamic RAM, 60ns, 300-mil Plastic DIP)

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: (408) 721-5000
TWX: (910) 339-9240

National Semiconductor GmbH
Industriestrasse 10
D-8080 Furstenfeldbruck
West Germany
Tel: (0-81-41) 103-0
Telex: 527-649
Fax: (08141) 103554

National Semiconductor Japan Ltd.
Sanseido Bldg. 5F
4-15 Nish. Shinjuku
Shinjuku-Ku
Tokyo 160, Japan
Tel: 3-299 7001
Fax: 3-299-7000

National Semiconductor Hong Kong Ltd.
Suite 513, 5th Floor
Chinachem Golden Plaza
77 Mody Road, Tsimshatsui East
Kowloon, Hong Kong
Tel: 3-7231290
Telex: 52996 NSSEA HX
Fax: 3-3112536

National Semiconductores Do Brasil Ltda.
Av. Brig. Faria Lima, 1383
6 0 Andor-Conj. 62
01451 Sao Paulo, SP, Brasil
Tel: (55/11) 212-5066
Fax: (55/11) 211-1181 NSBR BR

National Semiconductor (Australia) PTY, Ltd.
1st Floor, 441 St. Kilda Rd
Melbourne, 3004
Victory, Australia
Tel: (03) 267-5000
Fax: 61-3-2677458