National Semiconductor

PRELIMINARY
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GTL16612
CMOS 18-Bit GTL/TTL Universal Bus Transceiver

General Description

The GTL16612 is one in a series of transceivers designed specifically for GTL logic levels. The device is a CMOS GTL 18-Bit registered bus transceivers which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked mode.

National's GTL has internal edge-rate control and is Process, Voltage, and Temperature (PVT) compensated technology. Its function is similar to BTL or conventional GTL but with different driver output levels and receiver threshold.

The device provides TTL to GTL translation. The A port and control pins operate at LVTTL or 5V TTL logic levels. The B port operates at GTL levels. The direction of the data flow is determined by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latched-enable (LEAB and LEBA), and clock (CLKAB and CLKBA). The clock or latch-enable can be controlled by the clock-enable ($\overline{CEAB}$ and $\overline{CEBA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{CEAB}$ is low and CLKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch/flip-flop on the low-to-high transition of CLKAB if $\overline{CEAB}$ is also low. Output-enable $\overline{OEAB}$ is active-low. When $\overline{OEAB}$ is low, the outputs are active. When $\overline{OEAB}$ is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.

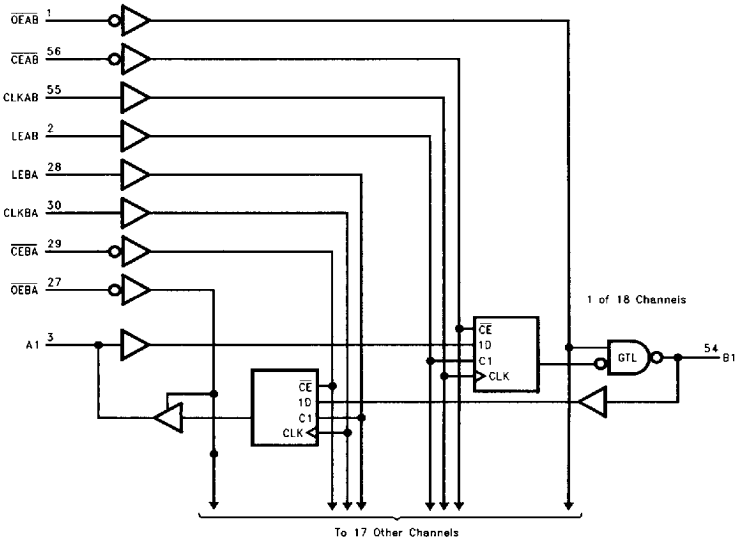
Driver and Receiver I/O pins are automatically disabled during power up and power down by internal control circuit.

National's GTL16612 is 100% I/O Spec compatible to conventional GTL.

Features

- Bidirectional interface between GTL and TTL logic levels
- Designed with Edge Rate Control Circuit to reduce output noise
- V_{REF} pin provides external supply reference voltage for receiver threshold
- Submicron Core CMOS technology for low power dissipation
- Special PVT Compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- 5V tolerant inputs and outputs on A-port
- Configurable A-port and B-port supply voltage, 3.3V or 5.0V
- Bus-Hold data inputs on A-port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down high impedance
- TTL compatible Driver and Control inputs
- A-port outputs source/sink −32 mA/+64 mA
- Flow-through architecture optimizes PCB layout
- Available in SSOP and TSSOP

Logic Diagram



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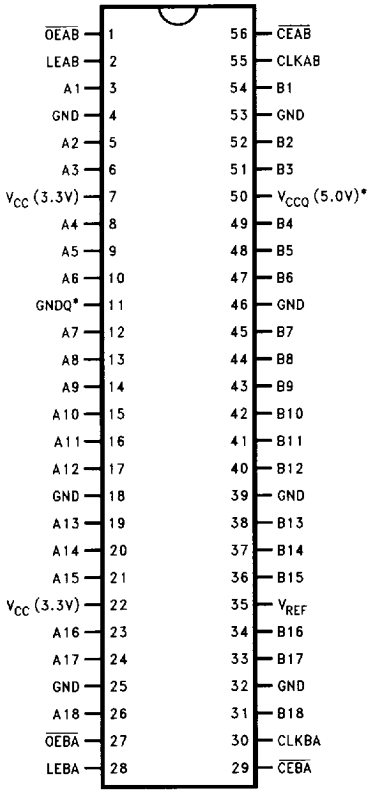
RRD B20M65/Printed in U S A

Connection Diagram

Pin Assignment for SSOP and TSSOP



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Order Number GTL16612MTD or GTL16612MEA
See NS Package Number MS56A or MTD56

***Note 1:** V_{CCQ} and GNDQ are the analog supply pins In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GNDQ/GND can be connected together respectively However, it is recommended that these supply pins are separated from each other to provide better bus performance

Truth Table (Note 1)

Inputs					Output B	Mode
$\overline{CEAB}$	$\overline{OEAB}$	LEAB	CLKAB	A		
X	H	X	X	X	Z	Latched storage of A data
L	L	L	H	X	B_0(2)	
L	L	L	L	X	B_0(3)	
X	L	H	X	L	L	Transparent
X	L	H	X	H	H	
L	L	L	↑	L	L	Clocked storage of A data
L	L	L	↑	H	H	
H	L	L	X	X	B_0(3)	Clock inhibit

Note 1: A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, GLKBA, and CEBA.

Note 2: Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

Note 3: Output level before the indicated steady-state input conditions were established

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}, V_{CCQ})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
DC Output Voltage (V_O)	
Outputs TRI-STATE®	−0.5V to +7.0V
Outputs Active (Note 2)	−0.5V to V_{CC} + 0.5V
DC Output Sink Current into A-port I_{OL}	128 mA
DC Output Source Current from A-port I_{OH}	−64 mA
DC Output Sink Current into B-port in the Low State, I_{OL}	100 mA
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{CC}	+50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed The device should not be operated at these limits The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation

Note 2: I_O Absolute Maximum Rating must be observed

Note 3: V_{CCQ} and GNDQ are the quiet supply pins. In the case that V_{CCQ} and V_{CC} are the same voltage level, V_{CCQ}/V_{CC} and GNDQ/GND can be connected together respectively. However, it is recommended that these supply pins are separated from each other to provide lower noise performance

Recommended Operating Conditions

Supply Voltage V_{CC}	
V_{CC}	3.15V to 3.45V
V_{CCQ}[3]	4.75V to 5.25V
V_{REF}	0.8V
Bus Termination Voltage (V_{TT})	1.14V to 1.26V
Input Voltage (V_I)	0.0V to 5.5V
On A-Port and Control Pins	
Input High Voltage (V_{IH})	
B-Port	V_{REF} + 50 mV to V_{TT}
Others	2.0V (min)
Input Low Voltage (V_{IL})	
B-Port	0.0V to V_{REF} − 50 mV
Others	0.8V (max)
High Level Output Current (I_{OH})	
A-Port	−32 mA
Low Level Output Current (I_{OL})	
A-Port	+64 mA
B-Port	+40 mA
Operating Temperature	
T_A	−40°C to +85°C

DC Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 0.8V (Unless Otherwise Noted)

Symbol		Test Conditions		Min	Typ (Note 1)	Max	Units
V_{IK}		V_{CC} = 3.15V, V_{CCQ} = 4.75V	I_I = −18 mA			−1.2	V
V_{OH}	A-Port	V_{CC}, V_{CCQ} = Min to Max (Note 2)	I_{OH} = −100 μA	V_{CC} − 0.2			V
		V_{CC} = 3.15V V_{CCQ} = 4.75V	I_{OH} = −8 mA	2.4			
			I_{OH} = −32 mA	2.0			
V_{OL}	A-Port	V_{CC}, V_{CCQ} = Min to Max (Note 2)	I_{OL} = 100 μA			0.2	V
		V_{CC} = 3.15V V_{CCQ} = 4.75V	I_{OL} = 24 mA			0.5	
			I_{OL} = 64 mA			0.55	
	B-Port	V_{CC} = 3.15V V_{CCQ} = 4.75V	I_{OL} = 40 mA		0.3	0.4	V
I_I	Control Pins	V_{CC}, V_{CCQ} = 0 or Max	V_I = 0 or 5.5V			±10	μA
	A-Port	V_{CC} = 3.45V V_{CCQ} = 5.25V	V_I = 5.5V			20	μA
			V_I = V_{CCQ}			1	
			V_I = 0			−20	
	B-Port	V_{CC} = 3.45V V_{CCQ} = 5.25V	V_I = V_{CCQ}			5	μA
			V_I = 0			−5	
I_{OFF}	A-Port	V_{CC} = V_{CCQ} = 0	V_I or V_O = 0 to 4.5V			100	μA
$I_{I(hold)}$	A-Port	V_{CC} = 3.15V, V_{CCA} = 4.75V	V_I = 0.5V	75			μA
			V_I = 3V	−75			

DC Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 0.8V (Unless Otherwise Noted) (Continued)

Symbol		Test Conditions		Min	Typ (Note 1)	Max	Units
I_{OZH}	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 3.0V			1	μA
	B-Port		V_O = 1.2V			10	
I_{OZL}	A-Port	V_{CC} = 3.45V, V_{CCQ} = 5.25V	V_O = 0			−1	μA
	B-Port		V_O = 0.4V			−10	
I_{CCQ} (V_{CCQ})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, V_I = V_{CCQ} or GND	Outputs High		20	30	mA
			Outputs Low		20	30	
			Outputs Disabled		20	30	
I_{CC} (V_{CC})	A or B Ports	V_{CC} = 3.45V, V_{CCQ} = 5.25V, I_O = 0, V_I = V_{CCQ} or GND	Outputs High		0.2	1	mA
			Outputs Low		0.2	1	
			Outputs Disabled		0.2	1	
ΔI_{CC} (Note 3)	A Port and Control Pins	V_{CC} = 3.45V, V_{CCQ} = 5.25V, A or Control Inputs at V_{CC} or GND	One Input at 2.7V			1	mA
C_i	Control Pins		V_I = V_{CCQ} or 0		3.5		pF
C_{io}	A-Port		V_I = V_{CCQ} or 0		11.5		
C_{io}	B-Port		Per IEEE1194-1991			5	

Note 1: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5.0V, and T_A = 25°C

Note 2: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions

Note 3: This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND

AC Electrical Characteristics

GTL B-port Output Edge Rate over recommended range of supply voltage and operating free-air temperature, V_{REF} = 0.8V (unless otherwise noted)

Symbol	Min	Typ (Note 1)	Max	Unit	Conditions
t_{RISE} 0.5V to 1.0V		1.5	1.9	ns	C_L = 5 pF
t_{FALL} 1.0V to 0.5V		1.2	1.6		

AC Operating Requirements

Over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 0.8V (unless otherwise noted)

Symbol			Min	Max	Unit
f_{clock}	Max Clock Frequency		0	100	MHz
t_{width}	Pulse Duration	LEAB or LEBA High	3.0		ns
		CLKAB or CLKBA High or Low	4.8		
t_{SU}	Setup Time	A before CLKAB ↑	0.5		ns
		B before CLKBA ↑	2.1		
		A before LEAB ↓	0.5		
		B before LEBA ↓	2.1		
		$\overline{CEAB}$ before CLKAB ↑	0.5		
		$\overline{CEBA}$ before CLKBA ↑	0.5		
t_{Hold}	Hold Time	A after CLKAB ↑	2.0		ns
		B after CLKBA ↑	0		
		A after LEAB ↓	2.0		
		B after LEBA ↓	0		
		$\overline{CEAB}$ after CLKAB ↑	0.5		
		$\overline{CEBA}$ after CLKBA ↑	0		

AC Electrical Characteristics

Over recommended range of supply voltage and operating free-air temperature, V_{REF} = 0.8V (unless otherwise noted). C_L = 5 pF for B-Port and C_L = 50 pF for A-Port.

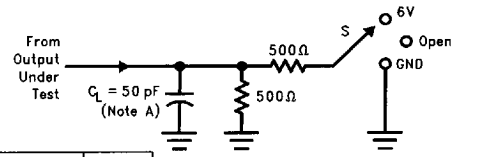
Symbol	From (Input)	To (Output)	Min	Typ (Note 2)	Max	Unit
f_{MAX}			100			MHz
t_{PLH}	A	B	1.0	2.5	4.0	ns
t_{PHL}			1.0	2.5	3.9	
t_{PLH}	LEAB	B	1.2	3.0	4.7	ns
t_{PHL}			1.2	3.0	4.7	
t_{PLH}	CLKAB	B	1.0	2.5	4.2	ns
t_{PHL}			1.0	2.5	4.0	
t_{PLH}	$\overline{OEAB}$	B	1.2	3.0	4.6	ns
t_{PHL}			1.2	2.4	3.8	
t_{PLH}	B	A	2.3	4.8	6.0	ns
t_{PHL}			2.0	4.0	5.0	
t_{PLH}	LEBA	A	1.8	3.5	4.5	ns
t_{PHL}			1.7	3.3	4.0	
t_{PLH}	CLKBA	A	1.8	2.8	4.0	ns
t_{PHL}			1.5	2.6	3.5	
t_{PLH}	$\overline{OEBA}$	A	2.2	3.5	4.5	ns
t_{PHL}			2.0	3.2	4.0	
t_{OSHLA}, t_{OSLHA}	A Port: Output to Output Skew (Note 2)				1.0	ns
t_{OSHLB}, t_{OSLHB}	B Port: Output to Output Skew (Note 2)				1.0	ns

Note 1: All typical values are at V_{CC} = 3.3V, V_{CCQ} = 5V, and T_A = 25°C.

Note 2: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}) Parameters guaranteed by design

Test Circuits and Timing Waveforms

Test Circuit for A Outputs



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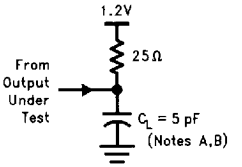
Test	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

Test Circuit for B Outputs



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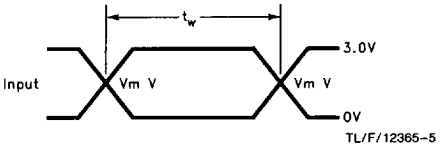
Voltage Waveforms Pulse Duration
(Vm = 1.5V for A Port and 0.8V for B Port)



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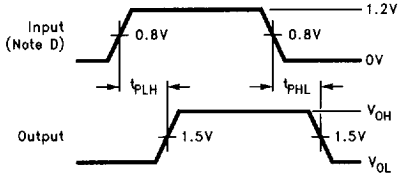
Voltage Waveforms Propagation Delay Times
(B Port to A Port)



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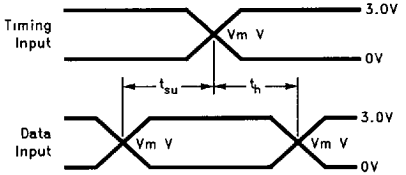
Voltage Waveforms Setup and Hold Times
(Vm = 1.5V for A Port and 0.8V for B Port)



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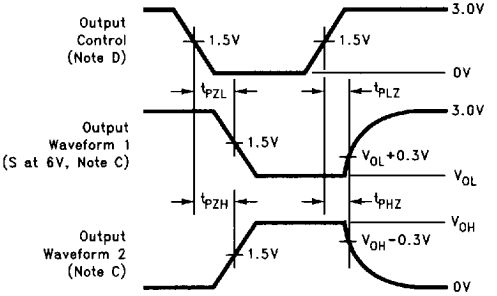
Voltage Waveforms Enable and Disable Times
(A Port)



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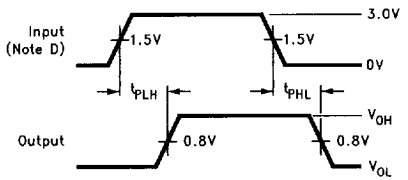
Voltage Waveforms Propagation Delay Times
(A Port to B Port)



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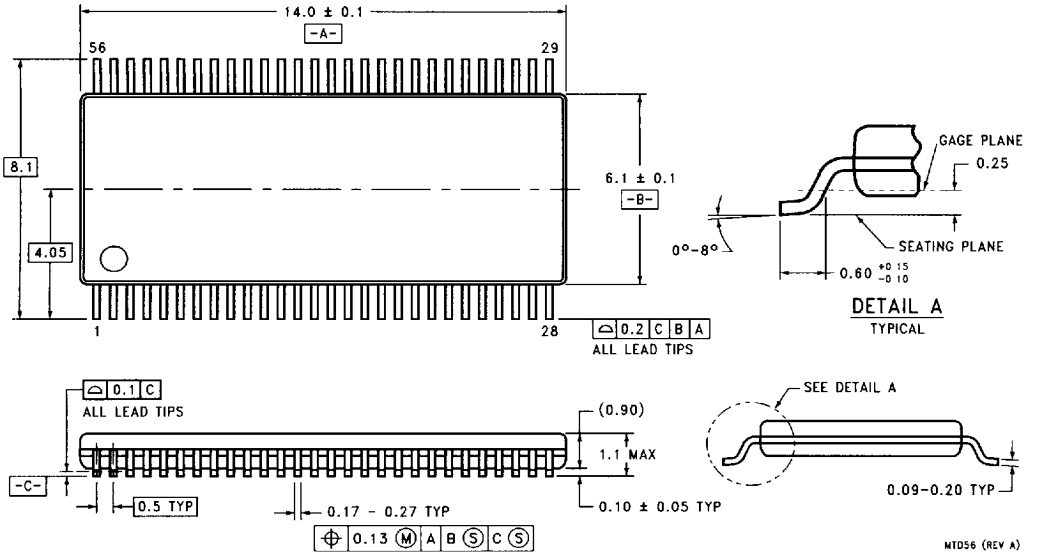
Note A: C_L includes probes and jig capacitance.

Note B: For B port outputs, C_L = 5 pF is used for worst case edge rate.

Note C: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

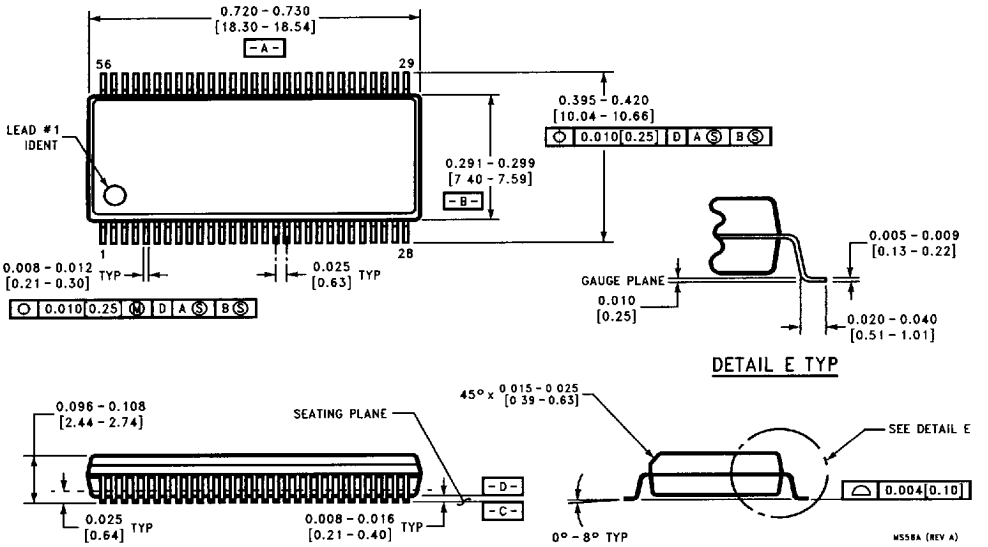
Note D: All input pulses have the following characteristics: frequency = 10 MHz, $t_r = t_f$ = 2 ns, Z_O = 50Ω The outputs are measured one at a time with one transition per measurement

Physical Dimensions (millimeters)



56-Lead Molded Thin Shrink Small Outline Package (JEDEC)
Order Number GTL16612MTD
NS Package Number MTD56

Physical Dimensions inches (millimeters) (Continued)



56-Lead (0.300" Wide) Molded Shrink Small Outline Package (JEDEC)
Order Number GTL16612MEA
NS Package Number MS56A

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