# CMOS 18-Bit TTL/GTLP Universal Bus Transceiver

## Features

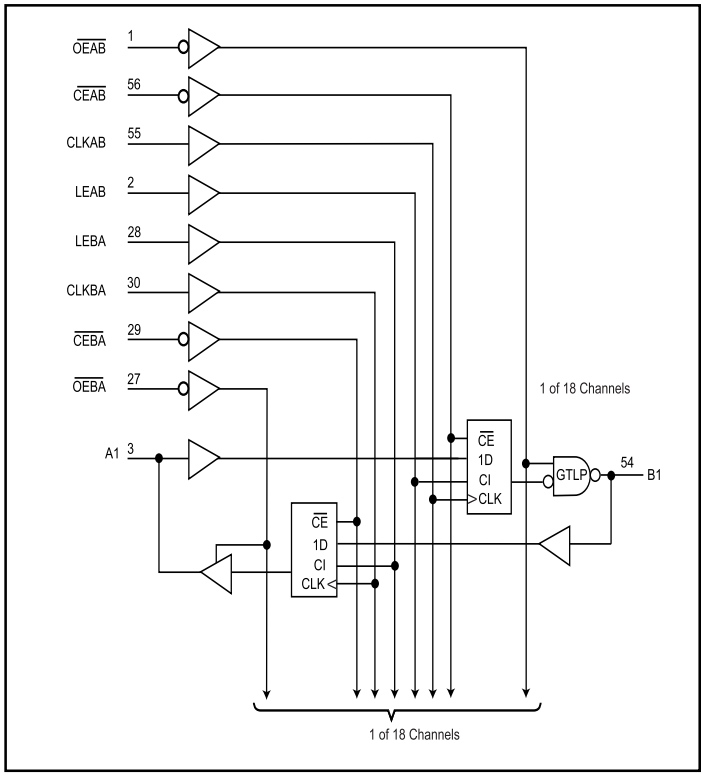
- Bidirectional interface between GTLP and TTL logic levels
- Designed with Edge Rate Control Circuit to reduce output noise
- $V_{REF}$ pin provides external supply reference voltage for receiver threshold
- 5V tolerant inputs and outputs on A-Port
- Increased B-Port Drive, 50mA
- Bus-Hold data inputs on A-Port to eliminate the need for pull-up resistors for unused inputs
- Power up/down high impedance
- TTL compatible Driver and Control inputs
- A-Port Balanced Drive: –32mA/+32mA
- Flow-through architecture
- Open drain on GTLP to support wired-or connection
- Package:
  — 56-pin 240 Mil Wide Plastic TSSOP (A)

## Product Description

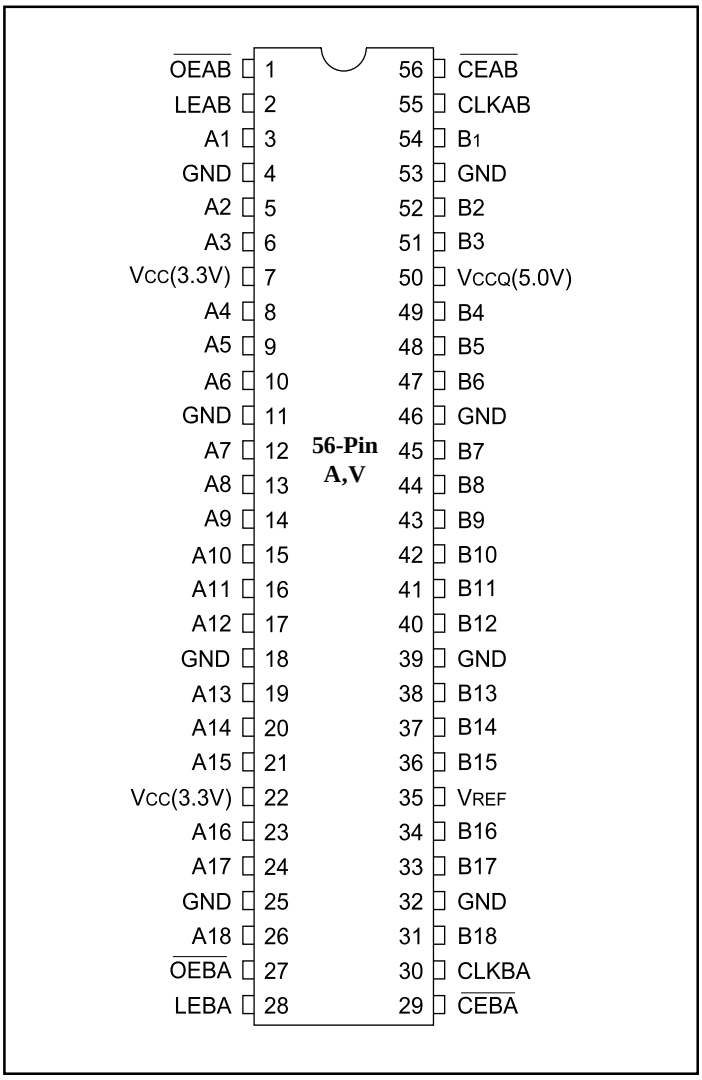
Pericom Semiconductor's GTLP series of logic circuits are produced using the Company's advanced 0.5 micron CMOS technology, achieving industry leading performance.

The GTLP16612A 18-bit universal transceiver provides TTL to GTLP signal level translation. The device is designed to provide high-speed interface between cards operating at TTL logic levels and a back plane operating at GTLP logic levels. High-speed back plane operation is a direct result of GTLP's reduced output swing (<1V), reduced input threshold levels, and output edge-rate control which minimizes signal settling times. Its function is similar to BTL or GTL but with modified driver output levels and receiver threshold. GTLP output low voltage is typically less than 0.5V, the output high is 1.5V, and the receiver threshold is 1.0V.

## Logic Block Diagram




## Pin Configuration



## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OEAB}$ | A-to-B Output Enable (Active LOW) |
| $\overline{OEBA}$ | B-to-A Output Enable (Active LOW) |
| $\overline{CEAB}$ | A-to-B Clock Enable (Active LOW) |
| $\overline{CEBA}$ | B-to-A Clock Enable (Active LOW) |
| LEAB | A-to-B Latch Enable (Transparent HIGH) |
| LEBA | B-to-A Latch Enable (Transparent HIGH) |
| CLKAB | A-to-B Clock Pulse |
| CLKBA | B-to-A Clock Pulse |
| VREF | GTLP Input Reference Voltage |
| A1-A18 | A-to-B TTL Data Inputs or<br>B-to-A 3-State Outputs |
| B1-B18 | B-to-A GTLP Data Inputs or<br>A-to-B Open Drain Outputs |

## Functional Description

The PI74GTLP16612A combines a universal transceiver function with a TTL to GTLP translation. The A-Port and control pins operate at LVTTL or 5V TTL levels while the B-Port operates at GTLP levels. The transceiver logic includes D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clock mode. The functional operation is described below:

## Truth Table(1)

| Inputs | | | | | Output B | Mode |
|---|---|---|---|---|---|---|
| $\overline{CEAB}$ | $\overline{OEAB}$ | LEAB | CLKAB | A | | |
| X | H | X | X | X | Z | Latched Storage of A Data |
| L | L | L | H | X | $B_0$(2) | |
| L | L | L | L | X | $B_0$(3) | |
| X | L | H | X | L | L | Transparent |
| X | L | H | X | H | H | |
| L | L | L | ↑ | L | L | Clocked Storage of A Data |
| L | L | L | ↑ | H | H | |
| H | L | L | X | X | $B_0$(3) | Clock Inhibit |

**Notes:**
1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA, and $\overline{CEBA}$.
2. Output level before indicated steady-state input conditions were established, provided CLKAB was HIGH before LEAB went LOW.
3. Output level before indicated steady-state input conditions were established.

## Absolute Maximum Ratings[4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

| | |
|---|---|
| Storage Temperature ($T_{STG}$) | –65°C to +150°C |
| Supply Voltage ($V_{CC}$, $V_{CCQ}$) | –0.5V to +7.0V |
| DC Input Voltage ($V_I$) | –0.5V to +7.0V |
| DC Output Voltage ($V_O$) | |
| Outputs 3-State | –0.5V to +7.0V |
| Outputs Active[5] | –0.5V to $V_{CC}$ +0.5V |
| DC Output Current into A-Port $I_{OH}/I_{OL}$ | –64mA/+64mA |
| DC Output Sink Current into B-Port in LOW State $I_{OL}$ | 100mA |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I < 0V$ | –50mA |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O < 0V$ | –50mA |
| $V_O > V_{CC}$ | +50mA |
| ESD Performance | >2000V |

## Recommended Operating Condition[6]

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | |
| $V_{CC}$ | 3.15V to 3.45V |
| $V_{CCQ}$ | 4.75V to 5.25V |
| Bus Termination Voltage ($V_{TT}$) | 1.35V to 1.65V |
| Input Voltage ($V_I$) on A-Port and Control Pins | 0.0V to 5.5V |
| HIGH Level Output Current ($I_{OH}$) | |
| A-Port | –32mA |
| LOW Level Output Current ($I_{OL}$) | |
| A-Port | +32mA |
| B-Port | +50mA |
| Operating Temperature ($T_A$) | –40°C to +85°C |

**Notes:**

4. The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristic tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.
5. $I_O$ Absolute Maximum Rating must be observed
6. Unused inputs must be held HIGH or LOW.

## DC Electrical Characteristics

(Over the Operating Free-Air Temperature Range, $V_{REF}$ = 1.0 (Unless otherwise noted)

| Symbol | | Test Conditions | | Min. | Typ[7] | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | B-Port | | | $V_{REF}$ +0.1 | | $V_{TT}$ | V |
| | Others | | | 2.0 | | | |
| $V_{IL}$ | B-Port | | | 0.0 | | $V_{REF}$ –0.1 | |
| | Others | | | | | 0.8 | |
| $V_{REF}$ | | | | | 1.0 | | |
| $V_{IK}$ | | $V_{CC}$ = 3.15V, $V_{CCQ}$ = 4.75V | $I_I$ = –18mA | | | –1.2 | |
| $V_{OH}$ | A-Port | $V_{CC}$, $V_{CCQ}$ = Min. to Max[8] | $I_{OH}$ = –100µA | $V_{CC}$ –0.2 | | | |
| | | $V_{CC}$ = 3.15V, $V_{CCQ}$ = 4.75V | $I_{OH}$ = –8mA | 2.4 | | | |
| | | | $I_{OH}$ = –32mA | 2.0 | | | |
| $V_{OL}$ | A-Port | $V_{CC}$, $V_{CCQ}$ = Min. to Max[8] | $I_{OL}$ = 100µA | | | 0.2 | |
| | | $V_{CC}$ = 3.15V, $V_{CCQ}$ = 4.75V | $I_{OL}$ = 32mA | | | 0.5 | |
| | B-Port | $V_{CC}$ = 3.15V, $V_{CCQ}$ = 4.75V | $I_{OL}$ = 50mA | | | 0.65 | |
| $I_I$ | Control Pins | $V_{CC}$, $V_{CCQ}$ = 0 or Max | $V_I$ = 5.5V or 0V | | | ±10 | µA |
| | A-Port | $V_{CC}$ = 3.45V, $V_{CCQ}$ = 5.25V | $V_I$ = 5.5V | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | |
| | | | $V_I$ = 0 | | | –30 | |
| | B-Port | $V_{CC}$ = 3.45V | $V_I$ = $V_{CCQ}$ | | | 5 | |
| | | $V_{CCQ}$ = 5.25V | $V_I$ = 0 | | | –5 | |
| $I_{OFF}$ | A-Port | $V_{CC}$ = $V_{CCQ}$ = 0 | $V_I$ or $V_O$ = 0 to 4.5V | | | 100 | |
| $I_{I(HOLD)}$ | A-Port | $V_{CC}$ = 3.15V, $V_{CCQ}$ = 4.75V | $V_I$ = 0.8V | 75 | | | |
| | | | $V_I$ = 2.0V | –20 | | | |
| $I_{OZH}$ | A-Port | $V_{CC}$ = 3.45V, $V_{CCQ}$ = 5.25V | $V_O$ = 3.45V | | | 1 | |
| | B-Port | | $V_O$ = 1.5V | | | 5 | |
| $I_{OZL}$ | A-Port | $V_{CC}$ = 3.45V, $V_{CCQ}$ = 5.25V | $V_O$ = 0 | | | –20 | |
| | B-Port | | $V_O$ = 0.65V | | | –10 | |
| $I_{CCQ}$ ($V_{CCQ}$) | A or B Ports | $V_{CC}$ = 3.45V, $V_{CCQ}$ = 5.25V, $I_O$ = 0, $V_I$ = $V_{CCQ}$ or GND | Outputs HIGH | | 30 | 40 | mA |
| | | | Outputs LOW | | 30 | 40 | |
| | | | Outputs Disabled | | 30 | 40 | |
| $I_{CC}$ ($V_{CC}$) | A or B Ports | $V_{CC}$ = 3.45V, $V_{CCQ}$ = 5.25V, $I_O$ = 0, $V_I$ = $V_{CCQ}$ or GND | Outputs HIGH | | 0 | 1 | |
| | | | Outputs LOW | | 0 | 1 | |
| | | | Outputs Disabled | | 0 | 1 | |
| $\Delta I_{CC}$[9] | A-Port and Control Pins | $V_{CC}$ = 3.45V, $V_{CCQ}$ = 5.25V, A or Control Inputs at $V_{CC}$ or GND | One Input at 2.7V | | 0 | 1 | |
| $C_{IN}$ | Control Pins | | $V_I$ = $V_{CCQ}$ or 0 | | 8 | | pF |
| $C_{I/O}$ | A-Port | | $V_I$ = $V_{CCQ}$ or 0 | | 9 | | |
| $C_{I/O}$ | B-Port | | $V_I$ = $V_{CCQ}$ or 0 | | 8 | | |

**Notes:**

7. All typical values are at $V_{CC}$ = 3.3V, $V_{CCQ}$ = 5.0V, and $T_A$ = 25°C
8. For conditions shown as Max. or Min., use the appropriate value specified under recommended operating conditions.
9. This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## AC Operating Requirements

(Over recommended ranges of supply voltage and operating free-air temperature, $V_{REF}$ = 1.0 (Unless otherwise noted)

| Symbol | | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $f_{CLOCK}$ | Max Clock Frequency | | 175 | | MHz |
| $t_W$ | Pulse Duration | LEAB or LEBA HIGH | 3.0 | | ns |
| | | CLKAB or CLKBA HIGH or LOW | 3.2 | | |
| $t_S$ | Setup Time | A before CLKAB↑ | 0.5 | | |
| | | B before CLKBA↑ | 3.1 | | |
| | | A before LEAB↓ | 1.3 | | |
| | | B before LEBA↓ | 3.7 | | |
| | | $\overline{CEAB}$ before CLKAB↑ | 0.4 | | |
| | | $\overline{CEBA}$ before CLKBA↑ | 1.0 | | |
| $t_H$ | Hold Time | A after CLKAB↑ | 1.5 | | |
| | | B after CLKBA↑ | 0.0 | | |
| | | A after LEAB↓ | 0.5 | | |
| | | B after LEBA↓ | 0.0 | | |
| | | $\overline{CEAB}$ after CLKAB↑ | 1.5 | | |
| | | $\overline{CEBA}$ after CLKBA↑ | 1.7 | | |

## AC Electrical Characteristics

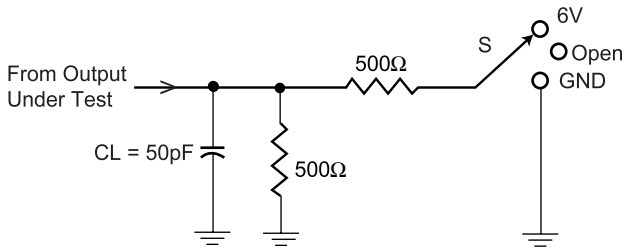
(Over recommended ranges of supply voltage and operating free-air temperature, $V_{REF}$ = 1.0 (Unless otherwise noted)
$C_L$ = 30pF for B-Port and $C_L$ = 50pF for A-Port.

| Symbol | From (Input) | To (Output) | Min. | Typ.(10) | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | A | B | 1.0 | 4.3 | 6.5 | ns |
| $t_{PHL}$ | | | 1.0 | 5.0 | 8.2 | |
| $t_{PLH}$ | LEAB | B | 1.8 | 4.5 | 6.7 | |
| $t_{PHL}$ | | | 1.5 | 5.3 | 8.6 | |
| $t_{PLH}$ | CLKAB | B | 1.8 | 4.6 | 6.7 | |
| $t_{PHL}$ | | | 1.5 | 5.4 | 8.7 | |
| $t_{PLH}$ | $\overline{OEAB}$ | B | 1.6 | 4.4 | 6.2 | |
| $t_{PHL}$ | | | 1.3 | 6.1 | 9.8 | |
| $t_{RISE}$ | Transition time, B outputs (20% to 80%) | | | 2.6 | | |
| $t_{FALL}$ | Transition time, B outputs (20% to 80%) | | | 2.6 | | |
| $t_{PLH}$ | B | A | 2.0 | 5.6 | 8.2 | |
| $t_{PHL}$ | | | 1.4 | 5.0 | 7.2 | |
| $t_{PLH}$ | LEBA | A | 2.1 | 4.2 | 6.3 | |
| $t_{PHL}$ | | | 1.9 | 3.3 | 5.0 | |
| $t_{PLH}$ | CLKBA | A | 2.3 | 4.4 | 6.8 | |
| $t_{PHL}$ | | | 2.2 | 3.5 | 5.2 | |
| $t_{PZH}$, $t_{PZL}$ | $\overline{OEBA}$ | A | 1.5 | 5.0 | 6.2 | |
| $t_{PHZ}$, $t_{PLZ}$ | | | 1.9 | 3.9 | 7.9 | |

**Note 10 :** All typical values are at $V_{CC}$ = 3.3V, $V_{CCQ}$ = 5.0V, and TA= 25°C

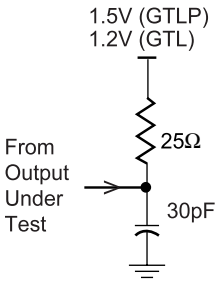
## Test Circuits and Timing Waveforms

### Test Circuit for A Outputs



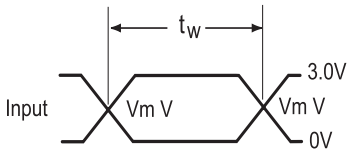

CL includes probes and jig capacitance.

### Test Circuit for B Outputs

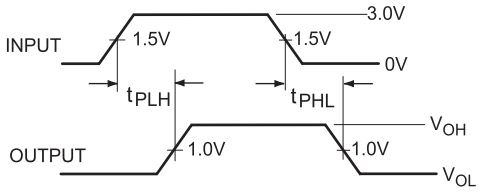



CL includes probes and jig capacitance.
For B-Port outputs, $C_L$ = 30pF is used for worst case edge rate

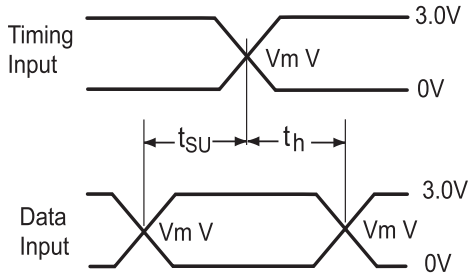
### Voltage Waveforms Pulse Duration (Vm = 1.5V for A-Port and 1.0V for B-Port)




### Voltage Waveforms Propagation Delay Times (A-Port to B-Port)

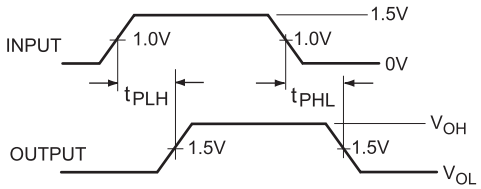



### Voltage Waveforms Setup and Hold Times (Vm = 1.5V for A-Port and 1.0V for B-Port)



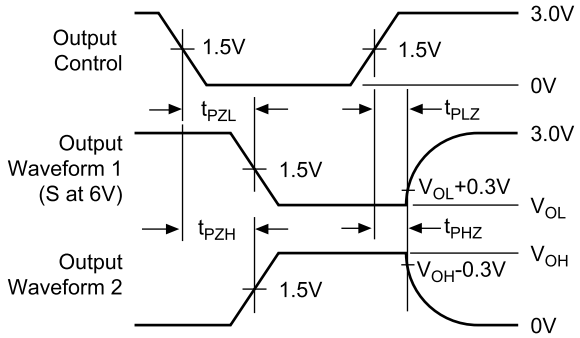

All input pulses have the following characteristics: frequency = 10 MHz, $t_r = t_f$ = 2ns, $Z_O$ = 50Ω. The outputs are measured one at a time with one transition per measurement.

### Voltage Waveforms Propagation Delay Times (B-Port to A-Port)



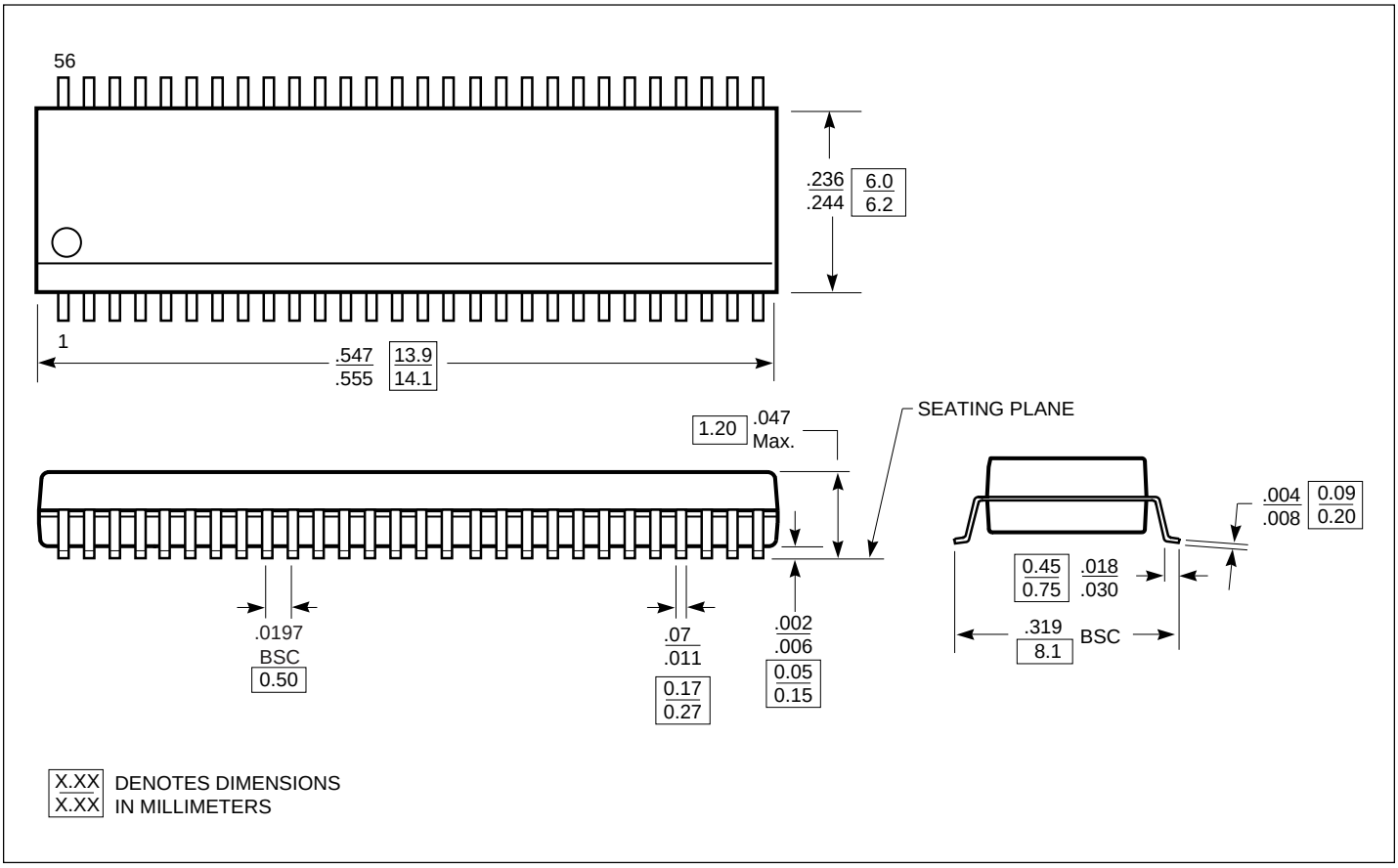

All input pulses have the following characteristics: frequency = 10 MHz, tp = 4 = 2ns, $Z_O$ = 50Ω. The outputs are measured one at a time with one transition per measurement.

### Voltage Waveforms Enable and Disable Times (A-Port)




Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high when disabled by the output control. All input pulses have the following characteristics: frequency = 10 MHz, $t_r = t_f$ = 2ns, $Z_O$ = 50Ω. The outputs are measured one at a time with one transition per measurement.

## 56-Pin TSSOP (240 MIL WIDE) - Package Code: A56




## Ordering Information

| P/N | Description |
|---|---|
| GTLP16612AA | 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |