

DESCRIPTION

The NN511664 series is a high performance CMOS Dynamic Random Access Memory organized as 65,536 words by 16 bits. The NN511664 series is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN511664 series features a high speed page mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

The outputs are tri-stated by $\overline{\text{CAS}}$ which, in essence, acts as an output enable independent of $\overline{\text{RAS}}$ with very fast $\overline{\text{CAS}}$ to output access time.

Refresh is accomplished by performing $\overline{\text{RAS}}$ only refresh cycles, hidden refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, or normal read or write cycles on the 256 address combinations of A0 to A7 during a 4 ms period.

Multiplexed address inputs permit NN511664 series to be packaged in a standard 40-pin plastic SOJ and 44-pin plastic TSOP TYPE II. The package sizes provide high system bit densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ±10% tolerance and direct interface with high performance TTL logic families.

FEATURES

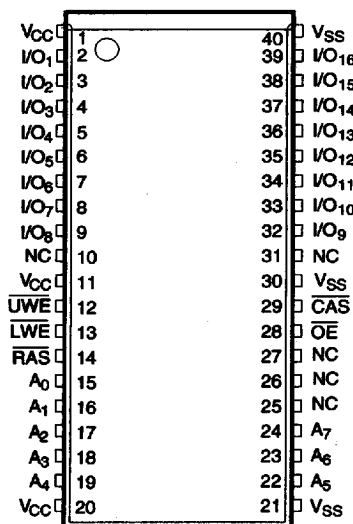
- 65,536 × 16 bit Organization
- Single 5V ±10% Power Supply
- Performance Ranges

Parameter	-40	-45	-50	-60	-70
Max. $\overline{\text{RAS}}$ Access Time (t_{RAC})	40ns	45ns	50ns	60ns	70ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	12ns	15ns	15ns	15ns	20ns
Max. Column Address Access Time (t_{AA})	20ns	25ns	25ns	30ns	35ns
Min. Read/Write Cycle Time (t_{RC})	70ns	80ns	90ns	110ns	130ns

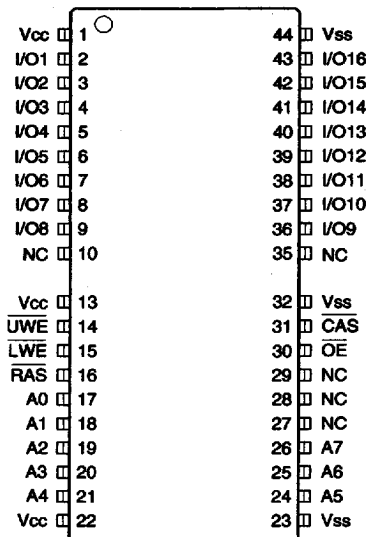
- Fast Page Mode Operation
- Separate $\overline{\text{WE}}$ (UWE, LWE) for Byte Selection
- Byte Write Mode Operation
- Low Power Operation
 - Low Standby Current (CMOS level input)
 - Standard 1mA
 - L version 50μA
- 256 Refresh Cycles
 - Standard distributed across 4ms
 - L version distributed across 32ms
- Self Refresh Mode (L version)
- All inputs/Outputs and Clocks fully TTL and CMOS compatible
- Refresh Modes
 - $\overline{\text{RAS}}$ only
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$
 - Hidden Refresh
- High Reliability Package
 - Plastic 40pin SOJ (P40SJ-2B)
 - Plastic 44 pin TSOP (TYPE II) (P44/40TP-3B)

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PIN CONFIGURATION (TOP VIEW)



40-pin SOJ (400mil)
P40SJ-2B



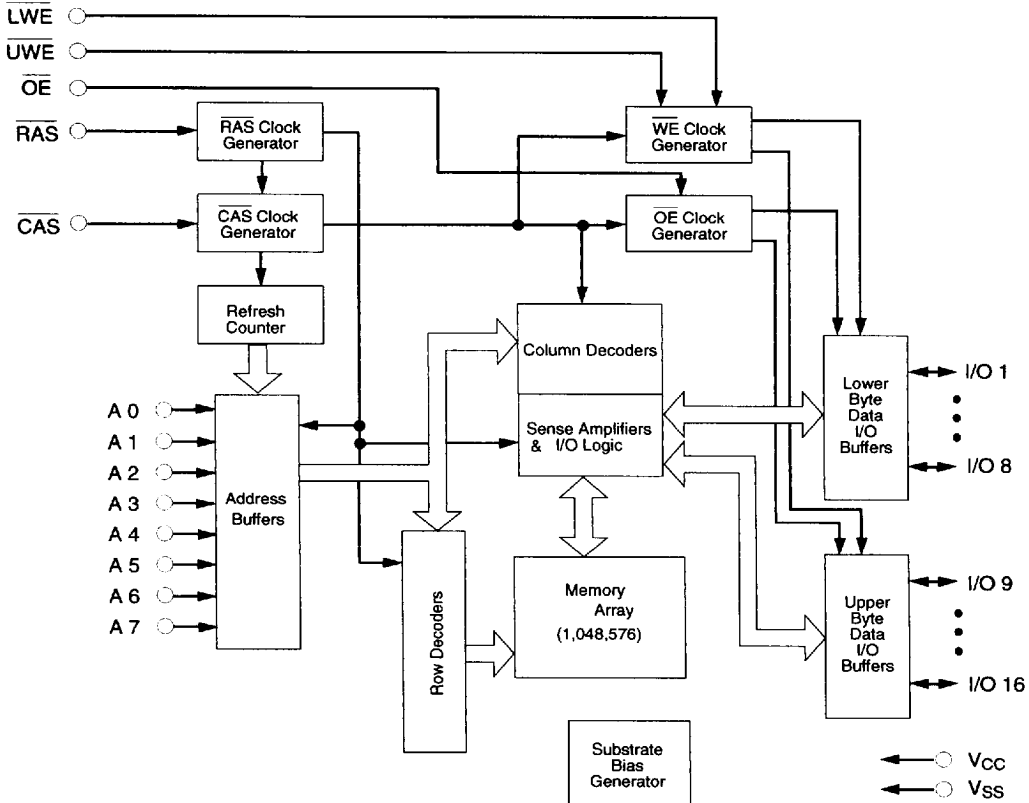
44/40-pin TSOP TYPE (II)
(400mil)
P44/40TP-3B

PIN NAMES

A0~A7	Address Inputs
<u>RAS</u>	Row Address Strobe
<u>CAS</u>	Column Address Strobe
<u>OE</u>	Output Enable
I/O1~I/O16	Data-in / Data-out
<u>UWE</u>	Write Enable Upper Byte Control
<u>LWE</u>	Write Enable Lower Byte Control
Vcc	+5.0V Supply
Vss	Ground
NC	No Connection

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FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	-1 to 7	V
Voltage on V_{CC} Relative to V_{SS}	V_{CC}	-1 to 7	V
Storage Temperature (Plastic)	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	1.0	W
Ambient Operating Temperature	T_a	0 to +70	°C
Short Circuit Output Current	I_{out}	50	mA

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage, All Inputs	2.4	—	6.5	V
V_{IL}	Input Low Voltage, All Inputs	-1.0	—	0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS} unless otherwise specified.

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DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I _{CC1}	Operating Current	-40		180	mA	t _{RC} = t _{RC} (min.) RAS, CAS, Address cycling	1, 2
		-45		160	mA		
		-50		140	mA		
		-60		120	mA		
		-70		100	mA		
I _{CC2}	Standby Current			1.0	mA	RAS = CAS ≥ (V _{CC} - 0.2V)	
				2.0	mA	RAS = CAS ≥ V _{IH}	
	Standby Current (L version)			50	μA	RAS = CAS ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC3}	Refresh Current (RAS only refresh)	-40		180	mA	t _{RC} = t _{RC} (min.) RAS cycling, CAS = V _{IH}	1
		-45		160	mA		
		-50		140	mA		
		-60		120	mA		
		-70		100	mA		
I _{CC4}	Fast Page Mode Current	-40		110	mA	t _{PC} = t _{PC} (min.) RAS = V _{IL} CAS, Address cycling	1,2
		-45		100	mA		
		-50		90	mA		
		-60		80	mA		
		-70		70	mA		
I _{CC5}	Refresh Current (CAS before RAS refresh)	-40		165	mA	t _{RC} = t _{RC} (min.) RAS, CAS cycling	1
		-45		145	mA		
		-50		125	mA		
		-60		105	mA		
		-70		85	mA		
I _{CC6}	Refresh Current (L version : CAS before RAS refresh)			150	μA	256 cycles / 32ms t _{RAS} ≤ 200ns, WE ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC7}	Self Refresh Mode Current (L version)			100	μA	RAS = CAS ≤ (V _{SS} + 0.2V) All other input high levels are (V _{CC} - 0.2V) or input low levels are (V _{SS} + 0.2V)	
I _{L1}	Input Leakage Current (Any input pin)		-10	10	μA	0V ≤ V _{IH} ≤ 5.5V, Others = 0V	
I _{L0}	Output Leakage Current (For high impedance state)		-10	10	μA	RAS ≥ V _{IH} (min.), CAS ≥ V _{IH} (min.) 0V ≤ V _{OUT} ≤ 5.5V	
V _{OH}	Output High Voltage		2.4		V	I _{OH} = -5.0 mA	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2 mA	

Notes: 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.

2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{IN1}	Address(A0~A7)	—	5	pF
C _{IN2}	RAS, CAS, UWE, LWE, OE	—	5	pF
C _{OUT}	I/O1~I/O16	—	7	pF

A.C. OPERATING CONDITIONS

Test conditions : $V_{IH} / V_{IL} = 2.4 / 0.8V$ $V_{OH} / V_{OL} = 2.0 / 0.8V$ output loading $C_L = 50pF + 1TTL$

Operating conditions : ($0^\circ C \leq T_a \leq 70^\circ C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$) (NOTES 3, 4, 5)

NO.	NOTES		PARAMETER	-40		-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	12	—	15	—	15	—	15	—	20	ns	6,13
2	t_{CH2QV}	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	28	—	30	—	30	—	35	—	40	ns	13,14
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	20	—	25	—	25	—	30	—	35	ns	7,13
4	t_{RL1QV}	t_{RAC}	Access Time from RAS	—	40	—	45	—	50	—	60	—	70	ns	6,7
5	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	40	—	45	—	50	—	60	—	70	—	ns	
6	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	8	—	8	—	8	—	10	—	10	—	ns	
7	t_{RL1CH1}	t_{CHS}	$\overline{CAS}$ Hold Time (Self Refresh Mode)	-50	—	-50	—	-50	—	-50	—	-50	—	ns	
8	t_{CH2CL2}	t_{CPN}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before RAS Refresh)	10	—	10	—	10	—	10	—	10	—	ns	
9	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	5	—	5	—	5	—	5	—	5	—	ns	14
10	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	12	100K	13	100K	13	100K	15	100K	20	100K	ns	
11	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before RAS Refresh)	5	—	5	—	5	—	5	—	5	—	ns	
12	t_{CL1QX}	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to RAS Precharge Time	5	—	5	—	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40	—	45	—	45	—	45	—	50	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	5	—	8	—	8	—	10	—	15	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to RAS	30	—	30	—	35	—	40	—	40	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns	14
18	t_{AVRH1}	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	20	—	22	—	27	—	30	—	35	—	ns	
19	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	47	—	52	—	57	—	60	—	65	—	ns	11
20	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	5	—	8	—	10	—	10	—	15	—	ns	12
21	t_{DVCL2} t_{DVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	0	—	0	—	ns	12
22	t_{OL1QV}	t_{OEA}	$\overline{OE}$ Access Time	—	12	—	13	—	15	—	15	—	20	ns	
23	t_{WL1OL2}	t_{OEH}	$\overline{OE}$ Command Hold Time	8	—	8	—	15	—	15	—	20	—	ns	
24	t_{CH2QV}	t_{OED}	$\overline{OE}$ to Data Delay Time	6	—	7	—	10	—	10	—	10	—	ns	
25	t_{CH2QZ}	t_{OFF}	Output Buffer Turn-off Delay Time	0	10	0	13	0	13	0	15	0	20	ns	10
26	t_{OH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{OE}$	0	8	0	10	0	10	0	15	0	15	ns	
27	t_{CL1RH1}	t_{RSH}	RAS Hold Time	12	—	13	—	15	—	15	—	20	—	ns	
28	t_{OL1RH1}	t_{ROH}	RAS Hold Time Referenced to $\overline{OE}$	8	—	8	—	10	—	10	—	10	—	ns	
29	t_{RH2RL2}	t_{RP}	RAS Precharge Time	25	—	25	—	25	—	30	—	40	—	ns	
30	t_{RH2RL2}	t_{RPS}	RAS Precharge Time (Self Refresh Mode)	70	—	80	—	90	—	110	—	130	—	ns	
31	t_{RL1RH1}	t_{RAS}	RAS Pulse Width	40	100K	45	100K	50	100K	60	100K	70	100K	ns	
32	t_{RL1RH1}	t_{RASP}	RAS Pulse Width (Fast Page Mode)	40	100K	45	100K	50	100K	60	100K	70	100K	ns	
33	t_{RL1RH1}	t_{RASS}	RAS Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	300	—	300	—	μs	
34	t_{RL1CL1}	t_{RCD}	RAS to $\overline{CAS}$ Delay Time	12	28	13	30	13	35	13	45	13	50	ns	6
35	t_{RH2CL2}	t_{RPC}	RAS to $\overline{CAS}$ Precharge Time	10	—	10	—	10	—	10	—	10	—	ns	

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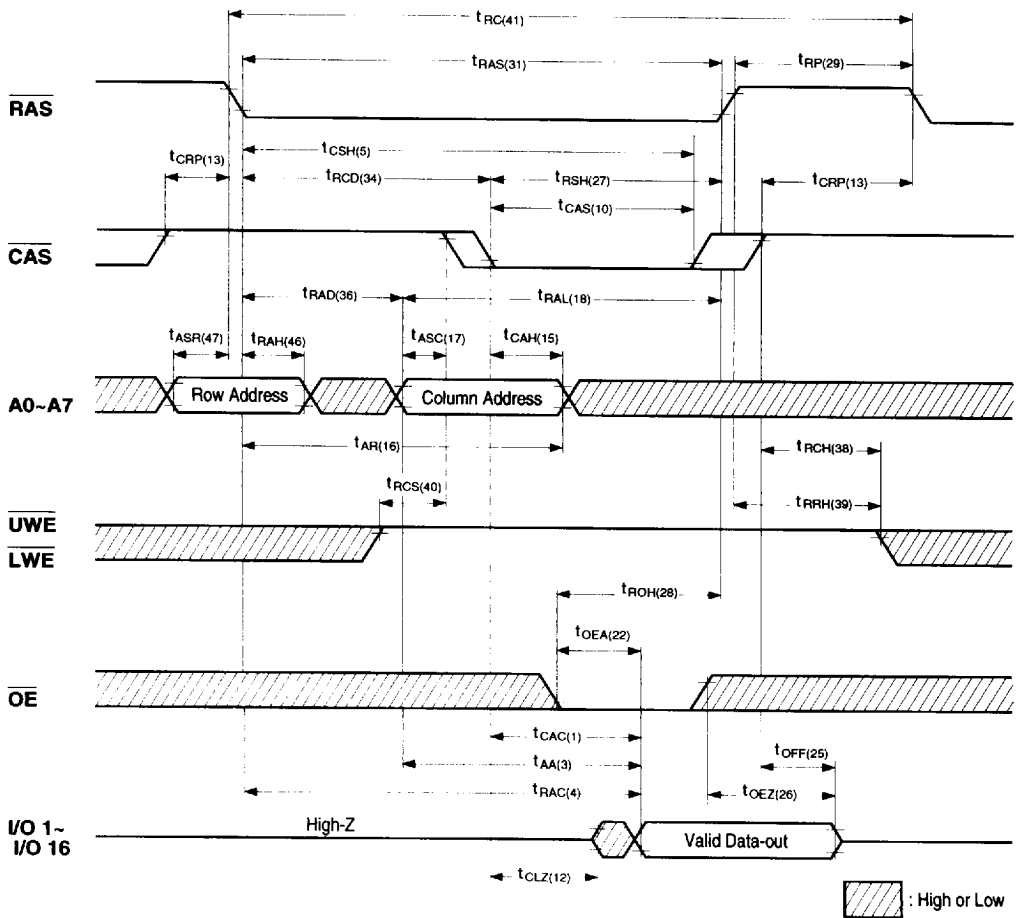
NO.	NOTES		PARAMETER	-40		-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t_{RL1AV}	t_{RAD}	RAS to Column Address Delay Time	10	19	11	20	11	23	11	30	11	35	ns	7
37	t_{RL1WL2}	t_{RWD}	RAS to WE Delay Time	58	—	75	—	80	—	90	—	100	—	ns	11
38	t_{CH2WL2}	t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	0	—	0	—	ns	9
39	t_{RH2WL2}	t_{RRH}	Read Command Hold Time Referenced to RAS	5	—	5	—	5	—	5	—	10	—	ns	9
40	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	0	—	0	—	ns	
41	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	70	—	80	—	90	—	110	—	130	—	ns	
42	t_{CL2CL2}	t_{PC}	Read or Write Cycle Time (Fast Page Mode)	23	—	30	—	33	—	40	—	45	—	ns	13,14
43	t_{RL2RL2}	t_{RMW}	Read-Modify-Write Cycle Time	115	—	120	—	125	—	135	—	185	—	ns	
44	t_{CL2CL2}	t_{PRMW}	Read-Modify-Write Cycle Time (Fast Page Mode)	55	—	57	—	57	—	66	—	100	—	ns	13,14
45	t_{REF}	t_{REF}	Refresh Period	—	4	—	4	—	4	—	4	—	4	ms	15
46	t_{RL1AX}	t_{RAH}	Row Address Hold Time	7	—	8	—	8	—	8	—	8	—	ns	
47	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns	
48	t_T	t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	2	50	2	50	ns	4,5
49	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	5	—	8	—	8	—	10	—	15	—	ns	
50	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	5	—	8	—	8	—	10	—	15	—	ns	
51	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0	—	0	—	0	—	0	—	0	—	ns	11
52	t_{WL1CH1}	t_{CWL}	Write Command to CAS Lead Time	12	—	13	—	13	—	15	—	20	—	ns	
53	t_{WL1RH1}	t_{RWL}	Write Command to RAS Lead Time	12	—	13	—	13	—	15	—	20	—	ns	

Notes:

- Eight Initialization Cycles are required following a 200 μ s pause after Power Up.
 These Initialization Cycles may consist of any combination of the following : RAS only refresh Cycles, Read Cycles, Write Cycles, CAS before RAS refresh Cycles.
- AC measurements assume $t_f=3$ ns.
- $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
- Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
- Assumes three state test load (5pF and a 220 ohm to 1.3V Thevenin equivalent).
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- $t_{OFF}(\text{max.})$ defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
- t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$ and $t_{AWD} \geq t_{AWD}(\text{min.})$, the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
- These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in read-modify-write cycles.
- Access time is determined by the longer of t_{AA} , t_{CAC} , or t_{CPA} .
- $t_{ASC} \geq t_{CP}$ to achieve $t_{PC}(\text{min.})$ and $t_{CPA}(\text{max.})$ values.
- $t_{REF}=32$ msec for Long Refresh version (L version).

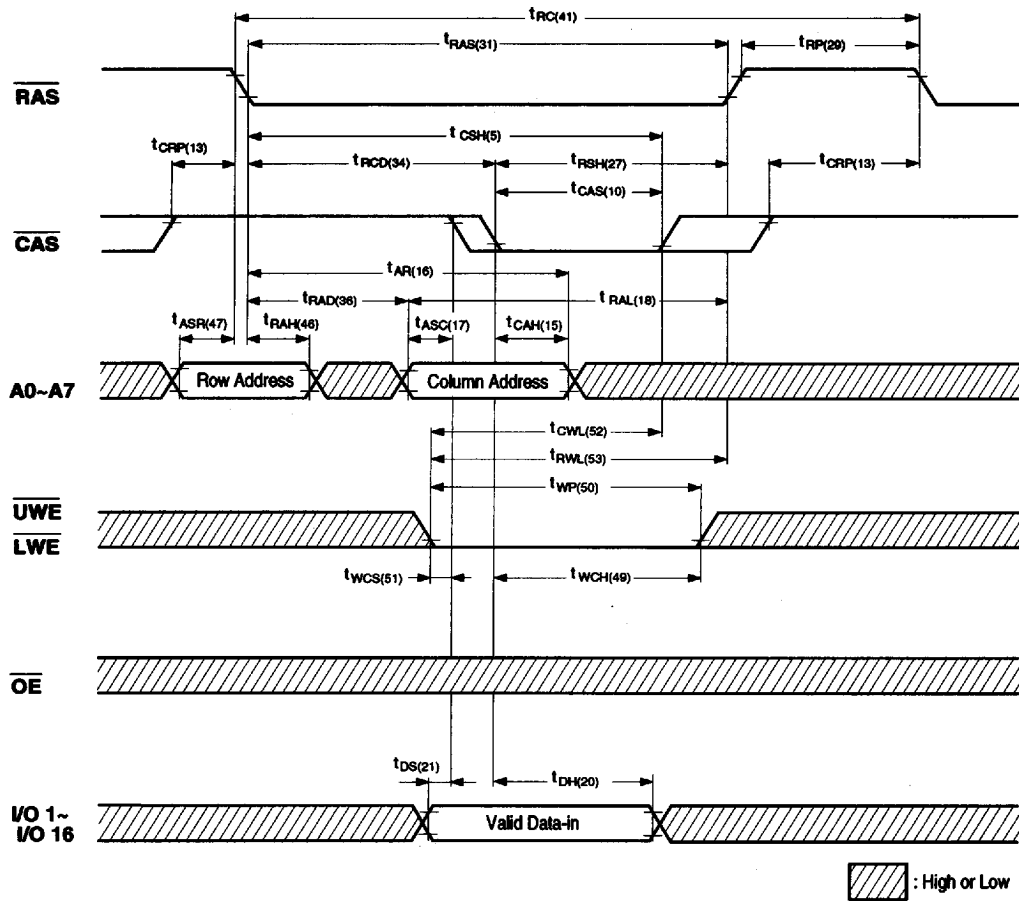
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WORD READ CYCLE



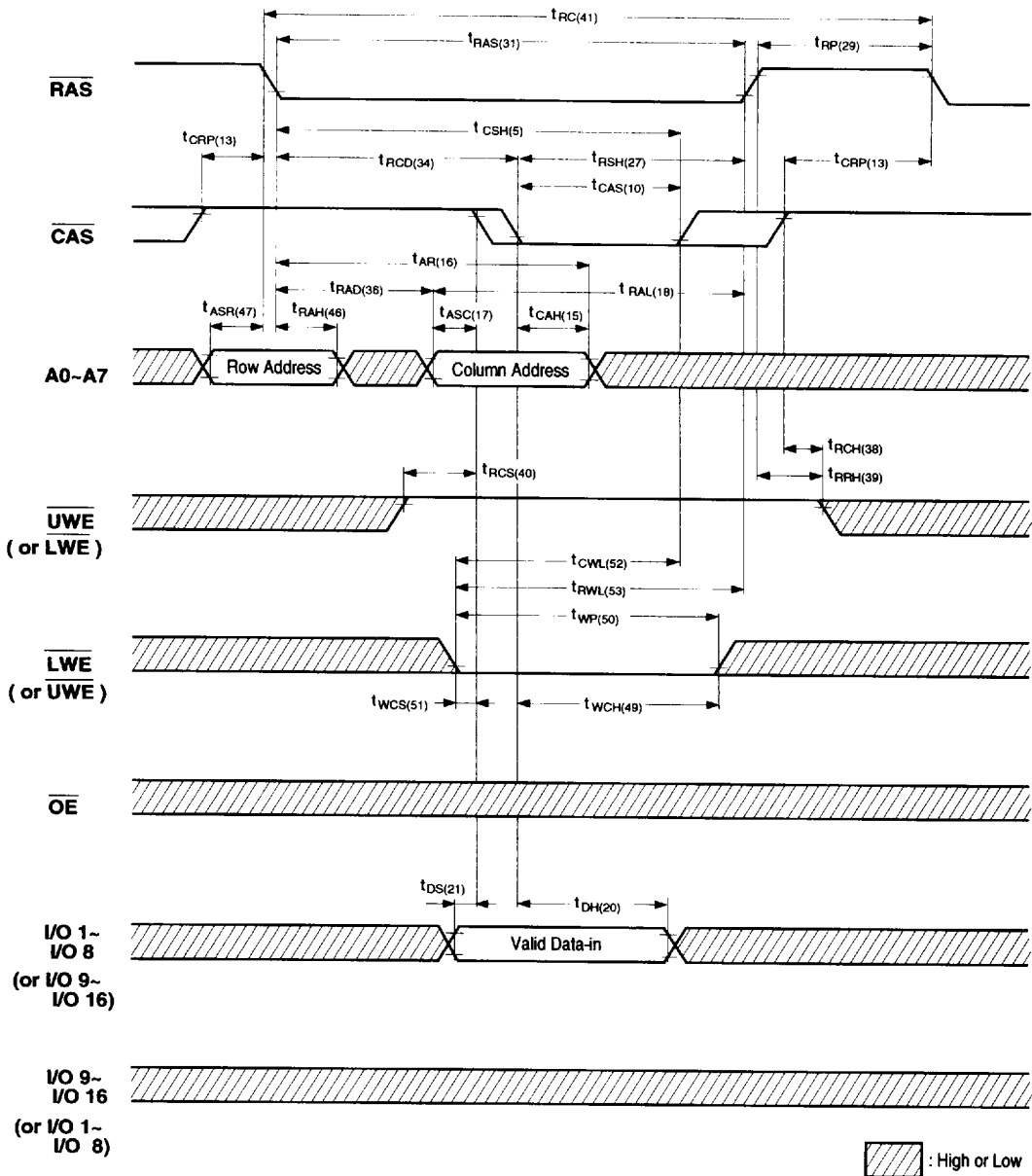
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WORD WRITE CYCLE (EARLY WRITE)



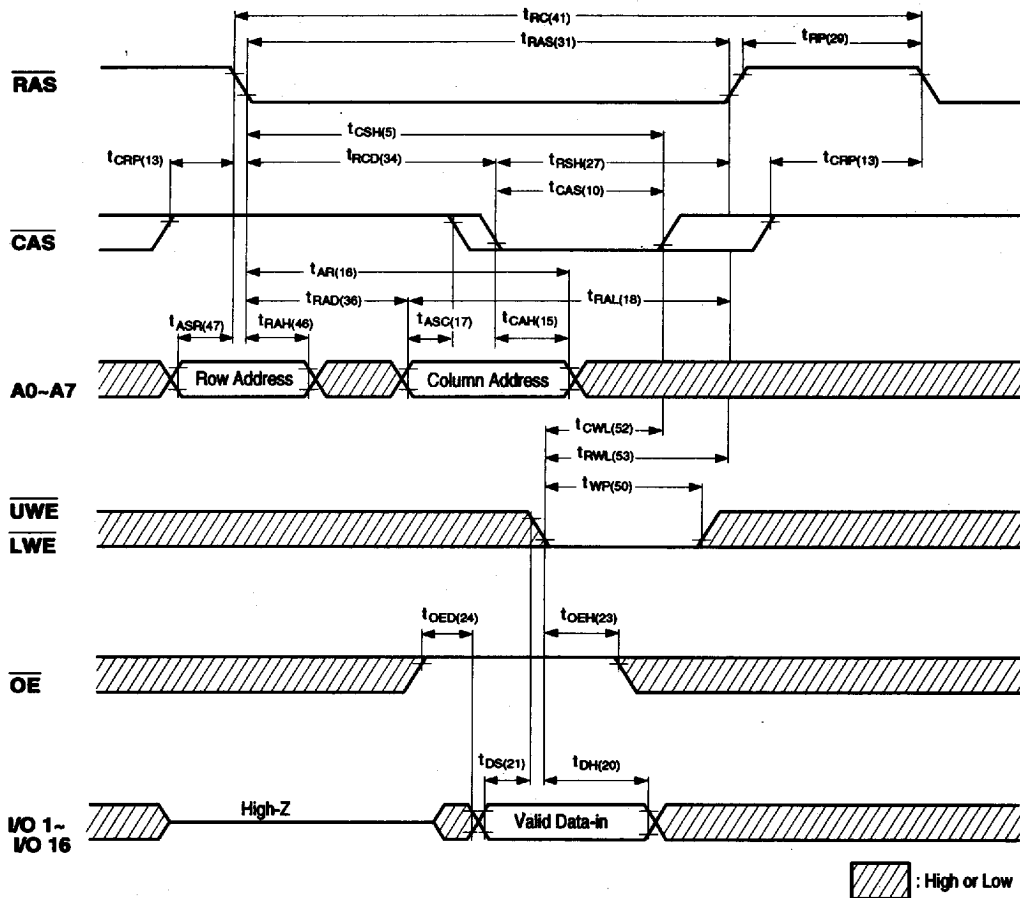
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BYTE WRITE CYCLE (EARLY WRITE)



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WORD WRITE CYCLE ($\overline{\text{OE}}$ -CONTROLLED WRITE)

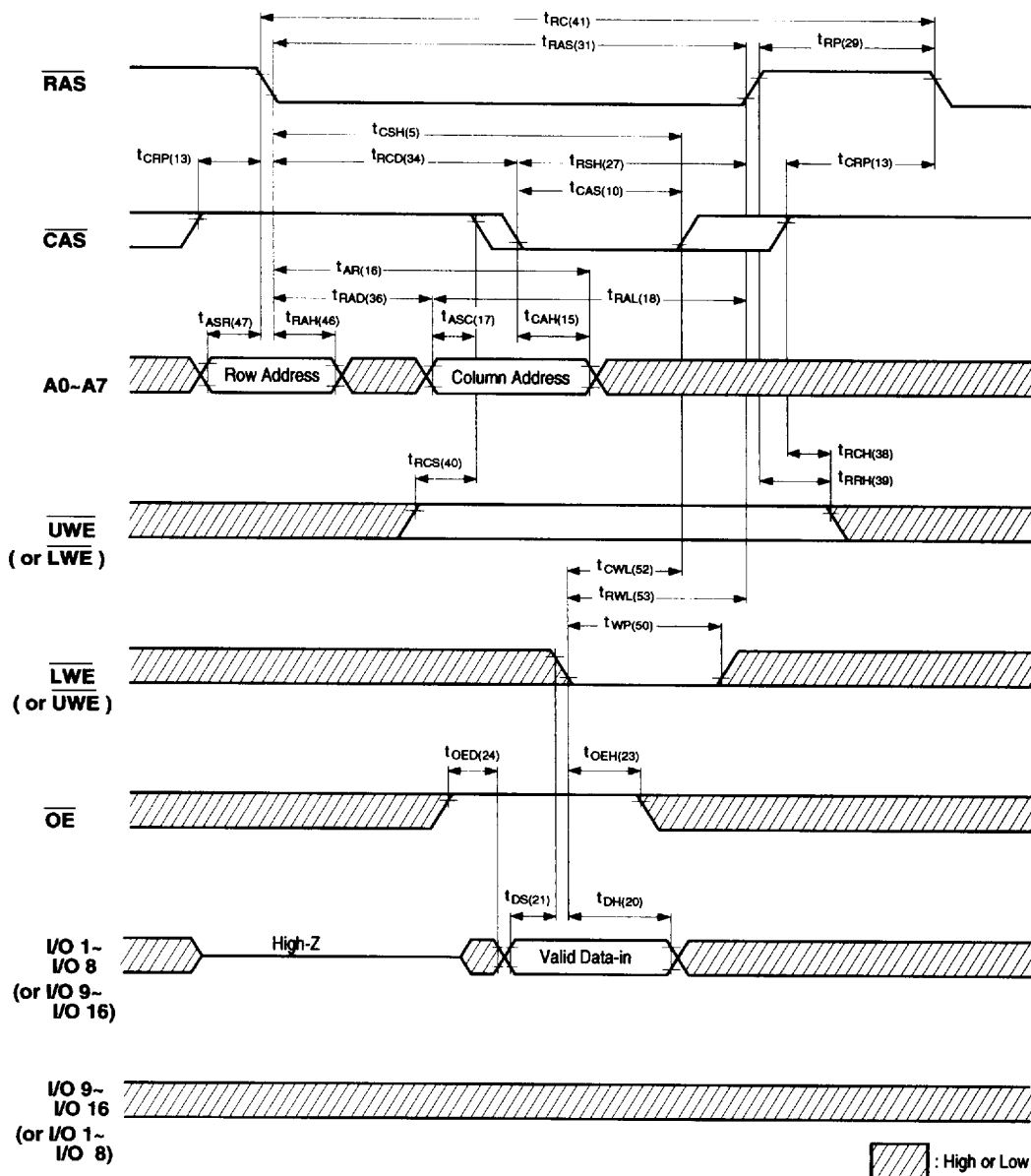


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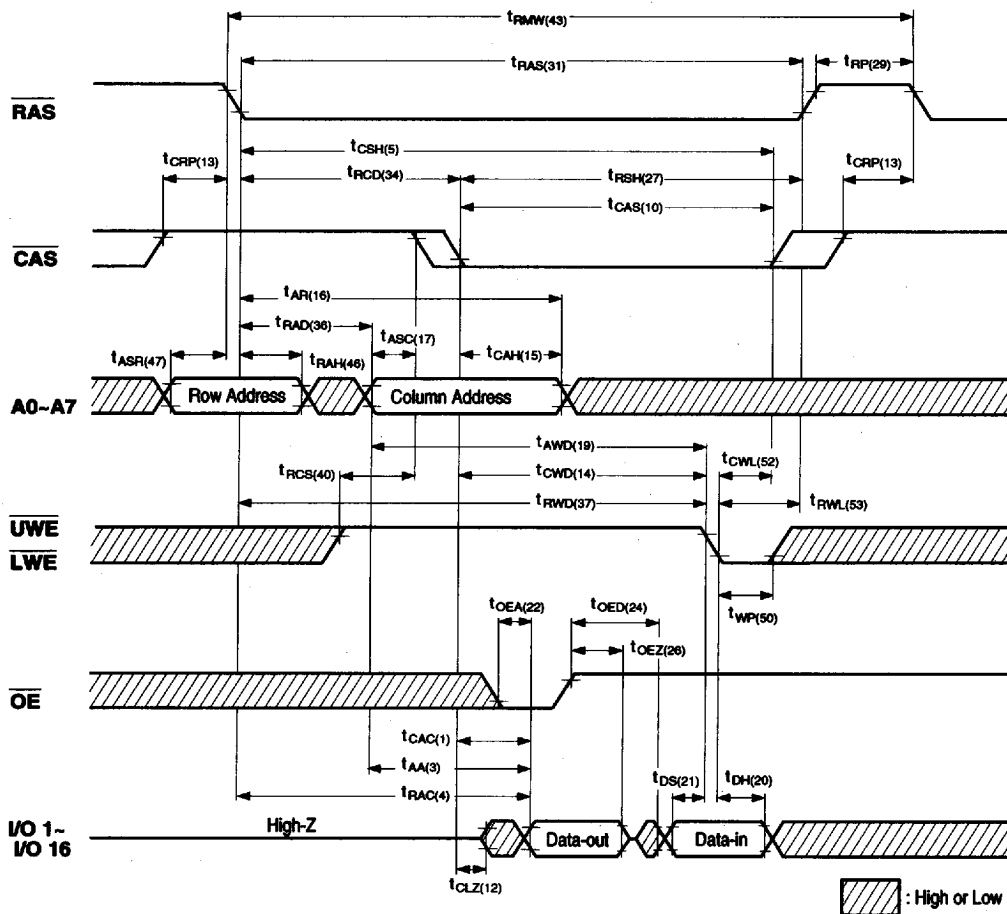
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BYTE WRITE CYCLE ($\overline{\text{OE}}$ -CONTROLLED WRITE)



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WORD READ-MODIFY-WRITE CYCLE

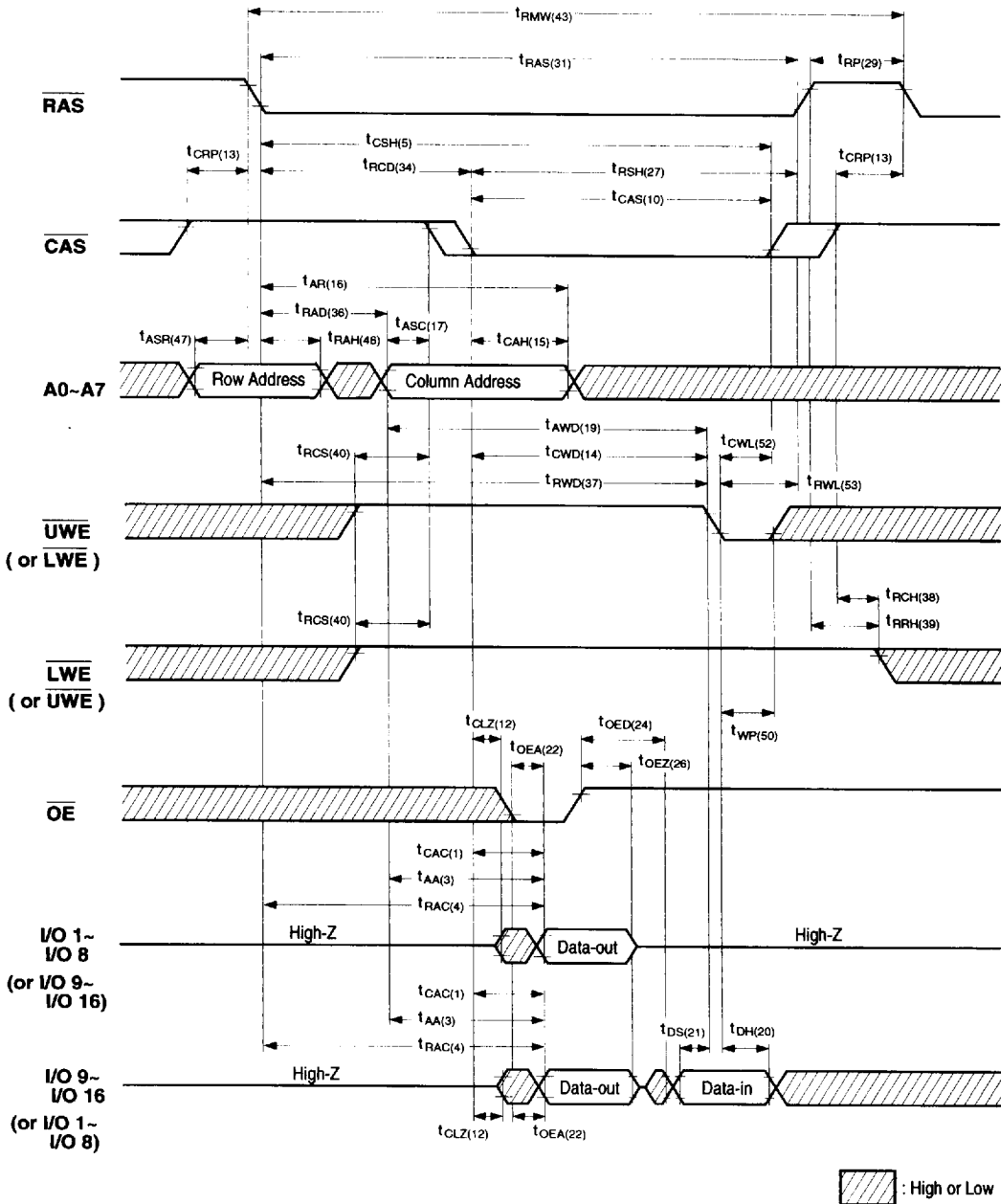


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NPNX

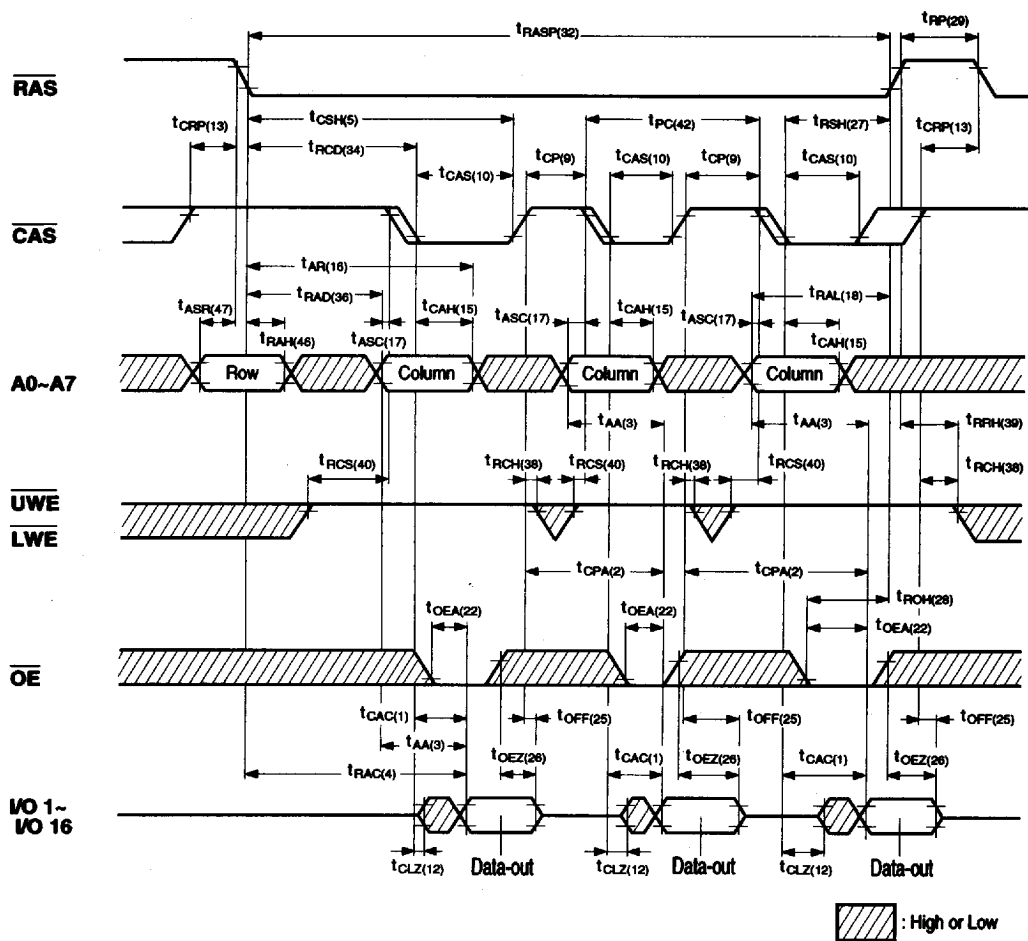
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BYTE READ-MODIFY-WRITE CYCLE



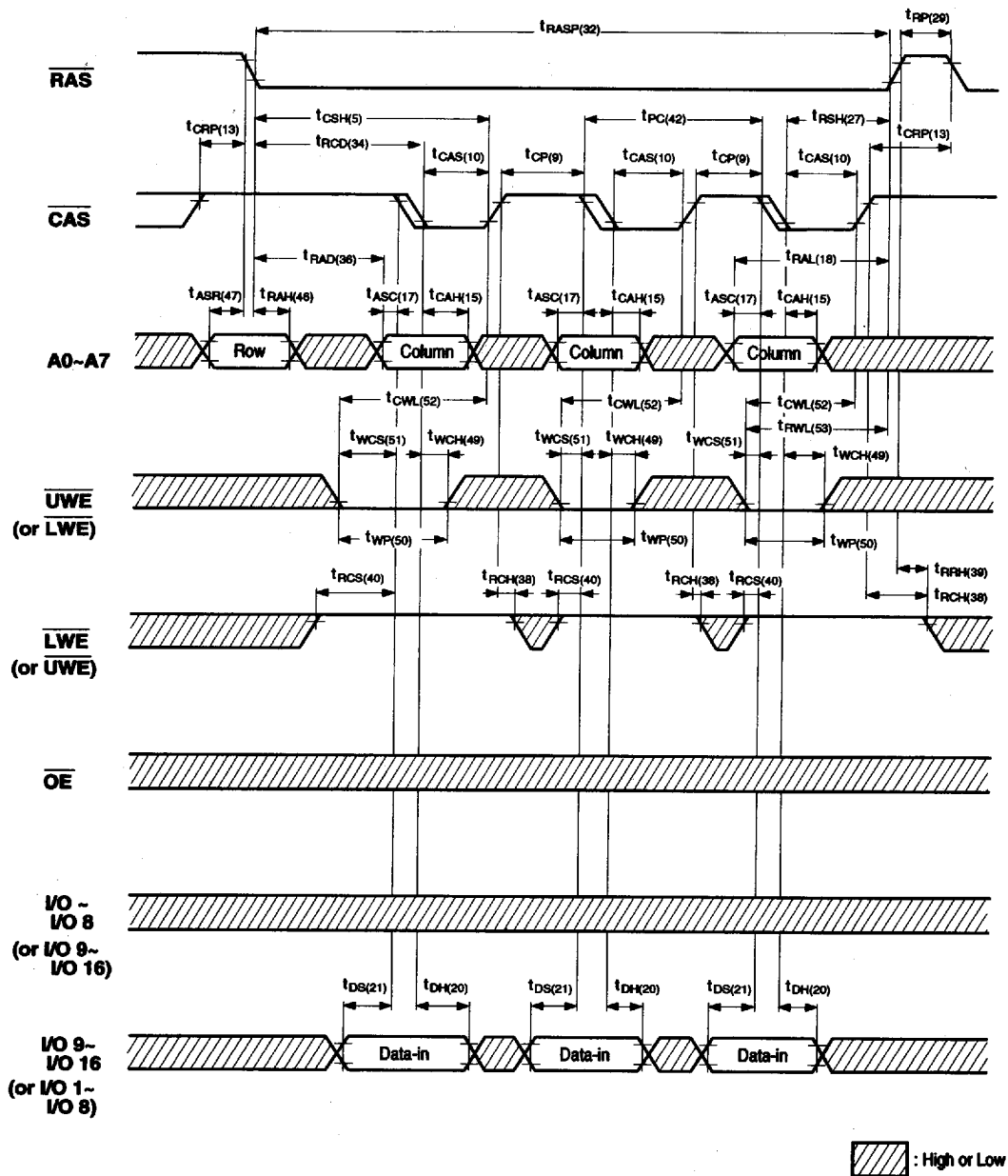
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FAST PAGE MODE WORD READ CYCLE

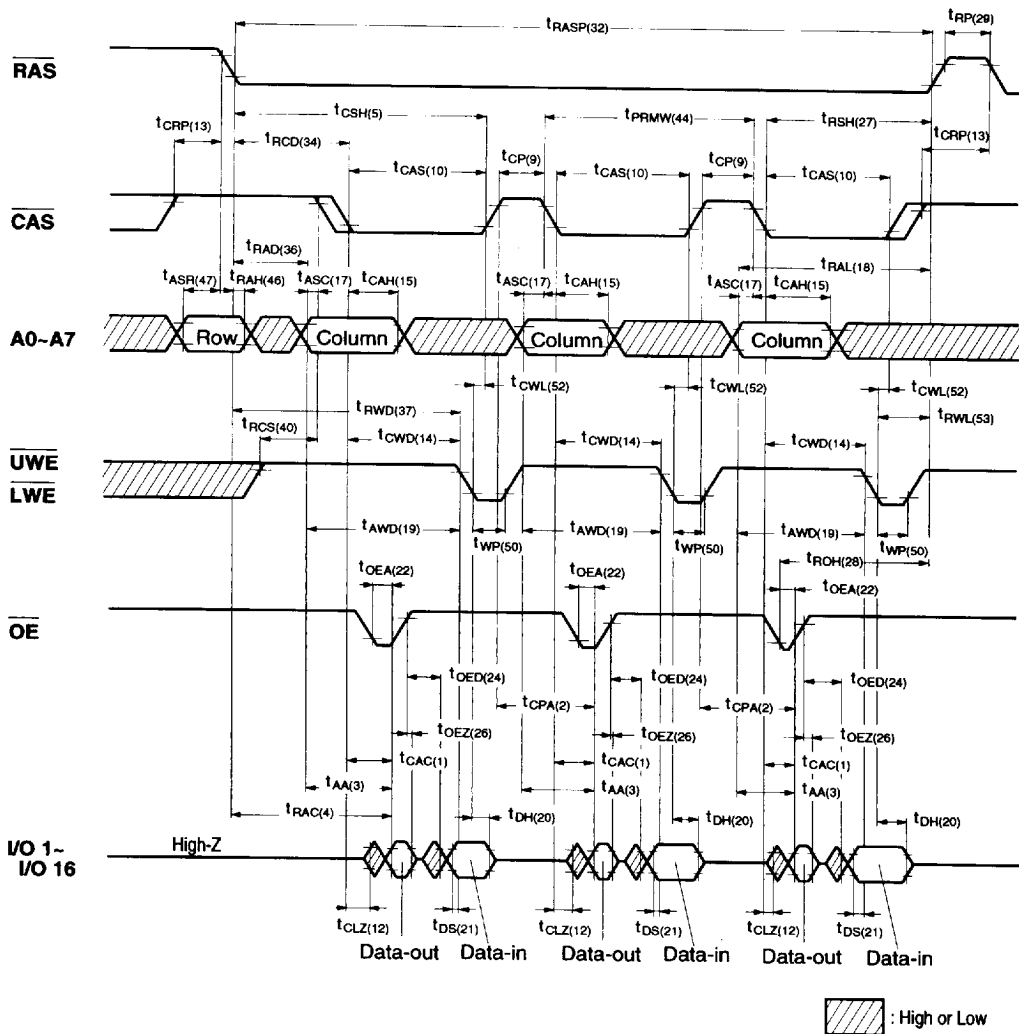




FAST PAGE MODE EARLY BYTE WRITE CYCLE

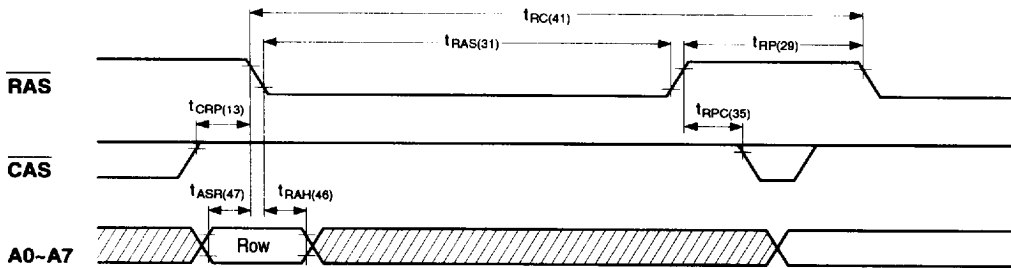


FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



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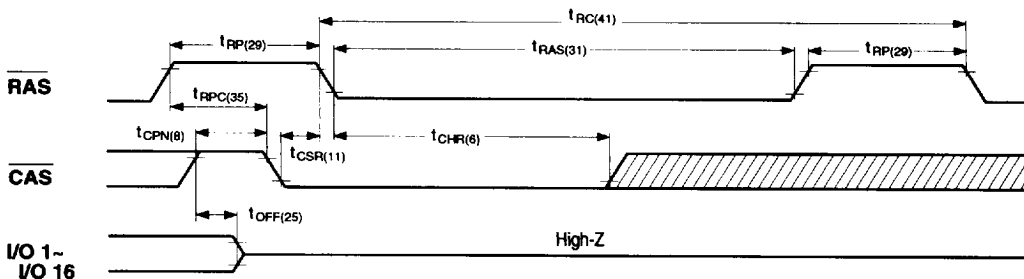
RAS ONLY REFRESH CYCLE



Note: $\overline{LWE}$, $\overline{UWE}$, $\overline{OE}$ = Don't care.

 : High or Low

CAS BEFORE RAS REFRESH CYCLE



Note: $\overline{LWE}$, $\overline{UWE}$, $\overline{OE}$, A0~A7 = Don't care.

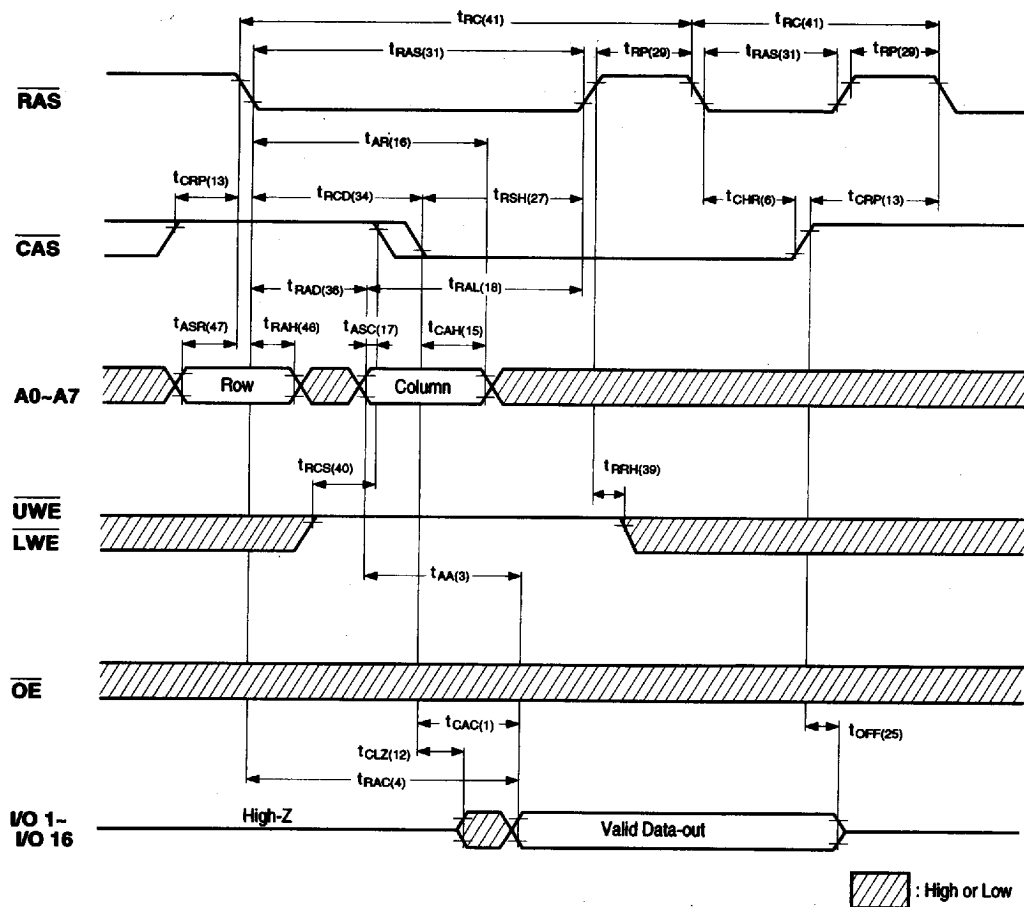
 : High or Low

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NPNX

HIDDEN REFRESH CYCLE (READ)

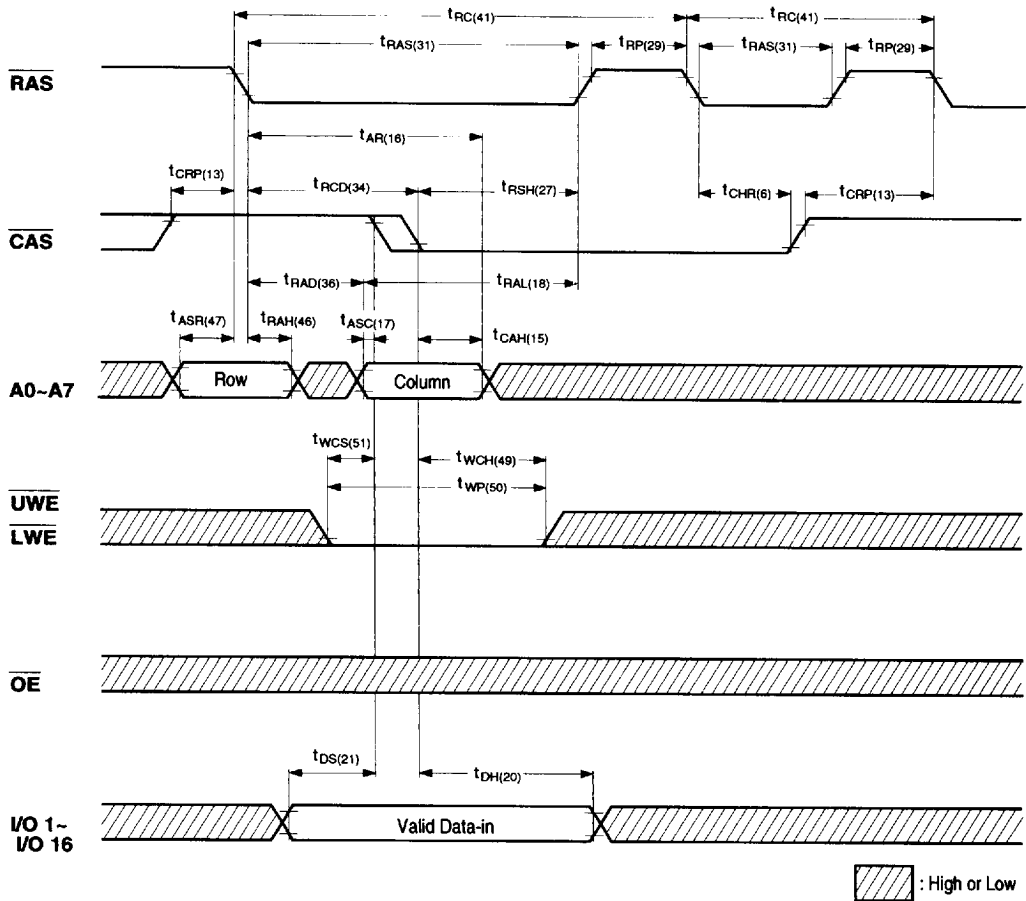


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NPNXX

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HIDDEN REFRESH CYCLE (EARLY WORD WRITE)



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ORDERING INFORMATION

NN511664XX(X) - XX

SPEED

40 : 40ns
45 : 45ns
50 : 50ns
60 : 60ns
70 : 70ns

PACKAGE

J : Plastic SOJ
TT : Plastic TSOP TYPEII

VERSION

BLANK : Standard Version
L : Long Refresh Version
32ms Refresh

MODE

1664 : Fast Page
2WE, 64K x 16 ,256 refresh cycle

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NPNX

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