

DESCRIPTION

The NN514260/A series is a high performance CMOS Dynamic Random Access Memory organized as 262,144 words by 16 bits. The NN514260/A series is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN514260/A series features a high speed page mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

The outputs are tri-stated by $\overline{\text{CAS}}$ which, in essence, acts as an output enable independent of $\overline{\text{RAS}}$ with very fast $\overline{\text{CAS}}$ to output access time.

Refresh is accomplished by performing $\overline{\text{RAS}}$ only refresh cycles, hidden refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, or normal read or write cycles on the 512 address combinations of A0 to A8 during a 8 ms period.

Multiplexed address inputs permit the NN514260/A series to be packaged in a standard 40-pin plastic SOJ, 44-pin plastic TSOP TYPEII. The package sizes provide high system bit densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V $\pm 10\%$ tolerance and direct interface with high performance TTL logic families.

FEATURES

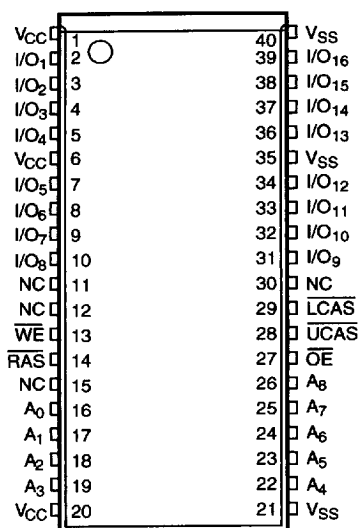
- 262,144 × 16 bit Organization
- Single 5V $\pm 10\%$ Power Supply
- Performance Ranges

Parameter	-45	-50	-60	-70
Max. $\overline{\text{RAS}}$ Access Time (t_{RAC})	45ns	50ns	60ns	70ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	15ns	15ns	15ns	20ns
Max. Column Address Access Time (t_{AA})	25ns	27ns	30ns	35ns
Min. Read/Write Cycle Time (t_{RC})	80ns	90ns	110ns	130ns

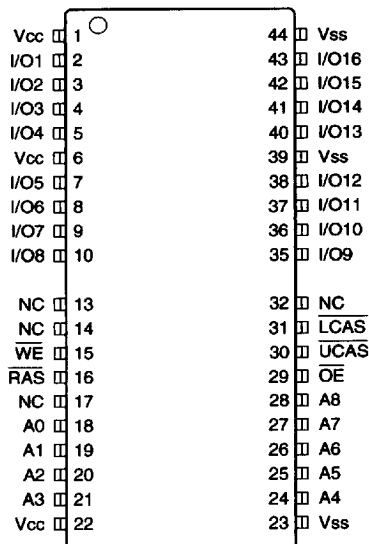
- Fast Page Mode Operation
- Separate $\overline{\text{CAS}}$ ($\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$) for Byte Selection
- Byte Read/Write Mode Operation
- Low Power Operation
 - Low Standby Current (CMOS level inputs)
 - Standard 1mA
 - L version 100 μ A
- 512 Refresh Cycles
 - Standard distributed across 8ms
 - L version distributed across 128ms
- Self Refresh Mode (L version)
- All inputs/Outputs and Clocks fully TTL and CMOS compatible
- Refresh Modes
 - $\overline{\text{RAS}}$ only
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$
 - Hidden Refresh
- High Reliability Package
 - Plastic 40pin SOJ (P40SJ-2B0)
 - Plastic 44pin TSOP TYPEII (P44TP-3B4)

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PIN CONFIGURATION (TOP VIEW)



40-pin SOJ (400mil)
P40SJ-2B0

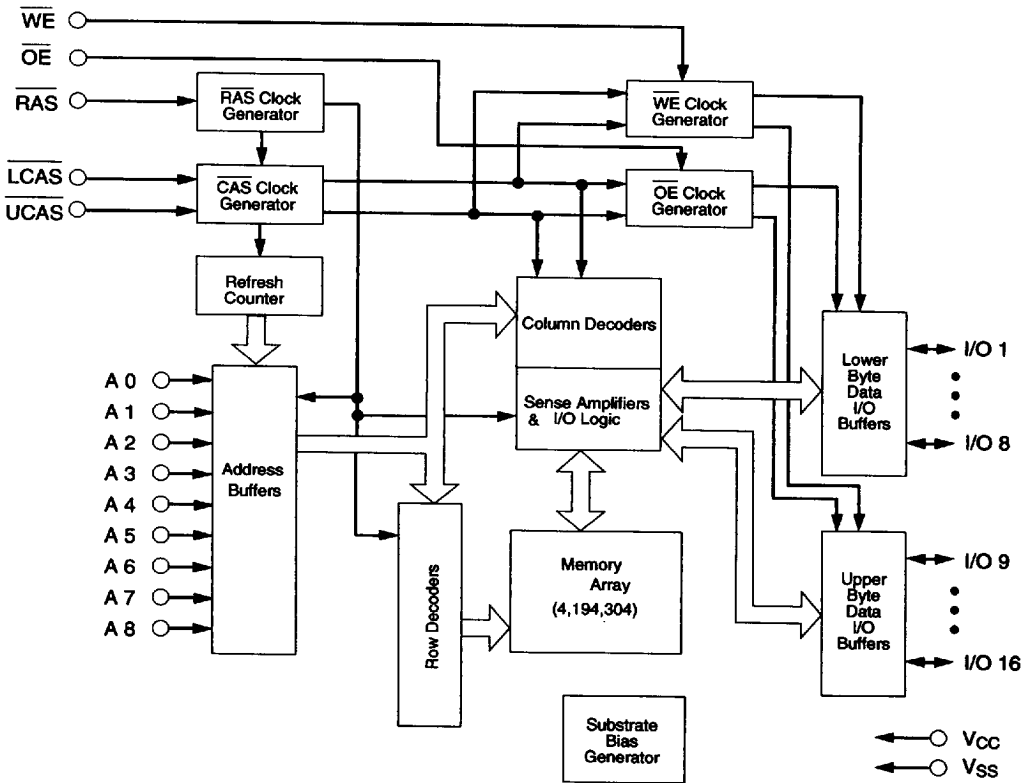


44/40-pin TSOP TYPE (II)
(400mil)
P44TP-3B4

PIN NAMES

A0~A8	Address Inputs
RAS	Row Address Strobe
UCAS	Column Address Strobe Upper Byte Control
LCAS	Column Address Strobe Lower Byte Control
OE	Output Enable
I/O1~I/O16	Data-in / Data-out
WE	Write Enable
V _{CC}	+5V Supply
V _{SS}	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	-1 to 7	V
Voltage on V_{CC} Relative to V_{SS}	V_{CC}	-1 to 7	V
Storage Temperature (Plastic)	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	1.0	W
Ambient Operating Temperature	T_a	0 to +70	°C
Short Circuit Output Current	I_{out}	50	mA

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage, All Inputs	2.4	—	6.5	V
V_{IL}	Input Low Voltage, All Inputs	-0.5	—	0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS} unless otherwise specified.

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DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I _{CC1}	Operating Current	-45 -50 -60 -70		180 160 150 130	mA mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS, Address cycling	1, 2
I _{CC2}	Standby Current			1.0	mA	RAS = CAS ≥ (V _{CC} - 0.2V)	
				2.0	mA	RAS = CAS ≥ V _{IH}	
I _{CC3}	Refresh Current (RAS only refresh)			100	μA	RAS = CAS ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC4}	Fast Page Mode Current	-45 -50 -60 -70		180 160 150 130	mA mA mA mA	t _{RC} = t _{RC} (min.) RAS = V _{IL} CAS, Address cycling	1, 2
I _{CC5}	Refresh Current (CAS before RAS refresh)	-45 -50 -60 -70		180 160 150 130	mA mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS cycling	1
I _{CC6}	Refresh Current (L version : CAS before RAS refresh)			150	μA	512 cycles / 128ms t _{RAS} ≤ 200ns, WE ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC7}	Self Refresh Mode Current (L version)			150	μA	RAS = CAS ≤ (V _{SS} + 0.2V) All other input high levels are (V _{CC} - 0.2V) or input low levels are (V _{SS} + 0.2V)	
I _{L1}	Input Leakage Current (Any input pin)		-10	10	μA	0V ≤ V _{IH} ≤ 5.5V, Others = 0V	
I _{L0}	Output Leakage Current (For high impedance state)		-10	10	μA	RAS ≥ V _{IH} (min.), CAS ≥ V _{IH} (min.) 0V ≤ V _{OUT} ≤ 5.5V	
V _{OH}	Output High Voltage		2.4		V	I _{OH} = -5.0 mA	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2 mA	

Notes: 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.

2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{IN1}	Address(A0 ~ A8)	—	5	pF
C _{IN2}	RAS, UCAS, LCAS, WE, OE	—	5	pF
C _{OUT}	I/O1 ~ I/O16	—	7	pF

A.C. OPERATING CONDITIONS (0 °C ≤ Ta ≤ 70 °C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (NOTES 3, 4, 5)

NO.	NOTES		PARAMETER	-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t _{CL1QV}	t _{CAC}	Access Time from $\overline{\text{CAS}}$	—	15	—	15	—	15	—	20	ns	6,13
2	t _{CH2QV}	t _{CPA}	Access Time from $\overline{\text{CAS}}$ Precharge	—	30	—	32	—	35	—	40	ns	13,14
3	t _{AVQV}	t _{AA}	Access Time from Column Address	—	25	—	27	—	30	—	35	ns	7,13
4	t _{RL1QV}	t _{RAC}	Access Time from $\overline{\text{RAS}}$	—	45	—	50	—	60	—	70	ns	6,7
5	t _{RL1CH1}	t _{CSH}	$\overline{\text{CAS}}$ Hold Time	45	—	50	—	60	—	70	—	ns	
6	t _{RL1CH1}	t _{CHR}	$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	10	—	10	—	10	—	10	—	ns	
7	t _{RL1CX}	t _{CHS}	$\overline{\text{CAS}}$ Precharge Time (Self Refresh Mode)	-50	—	-50	—	-50	—	-50	—	ns	
8	t _{CH2CL2}	t _{CPN}	$\overline{\text{CAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	10	—	10	—	10	—	10	—	ns	
9	t _{CH2CL2}	t _{CP}	$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	5	—	5	—	5	—	5	—	ns	14
10	t _{CL1CH1}	t _{CAS}	$\overline{\text{CAS}}$ Pulse Width	15	100K	15	100K	15	100K	20	100K	ns	
11	t _{CL1RL2}	t _{CSR}	$\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	5	—	5	—	5	—	5	—	ns	
12	t _{CL1QX}	t _{CLZ}	$\overline{\text{CAS}}$ to Output in Low-Z	0	—	0	—	0	—	0	—	ns	8
13	t _{CH2RL2}	t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	—	5	—	5	—	5	—	ns	
14	t _{CL1WL2}	t _{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	45	—	45	—	45	—	50	—	ns	11
15	t _{CL1AX}	t _{CAH}	Column Address Hold Time	10	—	10	—	15	—	15	—	ns	
16	t _{RL1AX}	t _{AR}	Column Address Hold Time Referenced to $\overline{\text{RAS}}$	30	—	35	—	40	—	40	—	ns	
17	t _{AVCL2}	t _{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	ns	14
18	t _{AVRH1}	t _{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	25	—	27	—	30	—	35	—	ns	
19	t _{AVWL2}	t _{AWD}	Column Address to $\overline{\text{WE}}$ Delay Time	55	—	57	—	60	—	65	—	ns	11
20	t _{CL1DX} t _{WL1DX}	t _{DH}	Data Hold Time	10	—	10	—	10	—	10	—	ns	12
21	t _{DVCL2} t _{DVWL2}	t _{DS}	Data Setup Time	0	—	0	—	0	—	0	—	ns	12
22	t _{OL1QV}	t _{OEa}	$\overline{\text{OE}}$ Access Time	—	15	—	15	—	15	—	20	ns	
23	t _{WL1OL2}	t _{OEh}	$\overline{\text{OE}}$ Command Hold Time	15	—	15	—	15	—	20	—	ns	
24	t _{CH2QV}	t _{OED}	$\overline{\text{OE}}$ to Data Delay Time	10	—	10	—	10	—	10	—	ns	
25	t _{CH2QZ}	t _{OFF}	Output Buffer Turn-off Delay Time	0	13	0	13	0	15	0	20	ns	10
26	t _{OH2QX}	t _{OEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{\text{OE}}$	0	10	0	10	0	15	0	15	ns	
27	t _{CL1RH1}	t _{RSH}	$\overline{\text{RAS}}$ Hold Time	15	—	15	—	15	—	20	—	ns	
28	t _{OL1RH1}	t _{ROH}	$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{OE}}$	10	—	10	—	10	—	10	—	ns	
29	t _{RH2RL2}	t _{RP}	$\overline{\text{RAS}}$ Precharge Time	25	—	25	—	30	—	40	—	ns	
30	t _{RH2RL2}	t _{RPS}	$\overline{\text{RAS}}$ Precharge Time (Self Refresh Mode)	80	—	90	—	110	—	130	—	ns	
31	t _{RL1RH1}	t _{RAS}	$\overline{\text{RAS}}$ Pulse Width	45	100K	50	100K	60	100K	70	100K	ns	
32	t _{RL1RH1}	t _{RASP}	$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	45	100K	50	100K	60	100K	70	100K	ns	
33	t _{RL1RH1}	t _{RASS}	$\overline{\text{RAS}}$ Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	300	—	μs	
34	t _{RL1CL1}	t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	13	30	13	35	13	45	13	50	ns	6
35	t _{RH2CL2}	t _{RPC}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	10	—	10	—	10	—	10	—	ns	
36	t _{RL1AV}	t _{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	11	20	11	23	11	30	11	35	ns	7
37	t _{RL1WL2}	t _{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	75	—	80	—	90	—	100	—	ns	11
38	t _{CH2WL2}	t _{RCH}	Read Command Hold Time	0	—	0	—	0	—	0	—	ns	9

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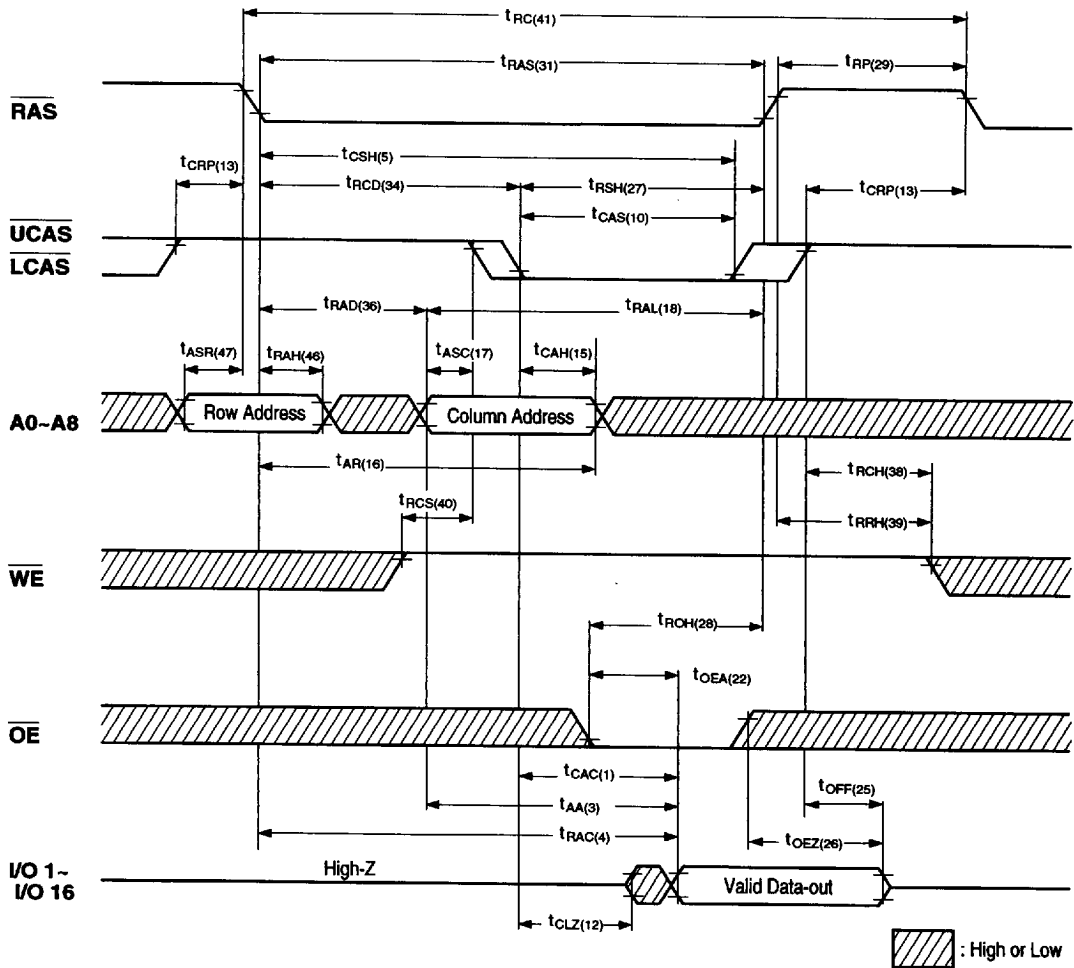
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NO.	SYMBOL		PARAMETER	-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
39	t_{RH2WL2}	t_{RRH}	Read Command Hold Time Referenced to RAS	10	—	10	—	10	—	10	—	ns	9
40	t_{WH2CL2}	t_{RCS}	Random Command Setup Time	0	—	0	—	0	—	0	—	ns	
41	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	80	—	90	—	110	—	130	—	ns	
42	t_{CL2CL2}	t_{PC}	Read or Write Cycle Time (Fast Page Mode)	30	—	33	—	40	—	45	—	ns	13,14
43	t_{RL2RL2}	t_{RMW}	Read-Modify-Write Cycle Time	135	—	145	—	165	—	185	—	ns	
44	t_{CL2CL2}	t_{PRMW}	Read-Modify-Write Cycle Time (Fast Page Mode)	90	—	90	—	95	—	100	—	ns	13,14
45	t_{REF}	t_{REF}	Refresh Period	—	8	—	8	—	8	—	8	ms	15
46	t_{RL1AX}	t_{RAH}	Row Address Hold Time	8	—	8	—	8	—	8	—	ns	
47	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	0	—	ns	
48	t_T	t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	2	50	ns	4,5
49	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10	—	10	—	10	—	15	—	ns	
50	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	10	—	10	—	10	—	15	—	ns	
51	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0	—	0	—	0	—	0	—	ns	11
52	t_{WL1CH1}	t_{CWL}	Write Command to CAS Lead Time	15	—	15	—	15	—	20	—	ns	
53	t_{WL1RH1}	t_{RWL}	Write Command to RAS Lead Time	15	—	15	—	15	—	20	—	ns	

Notes:

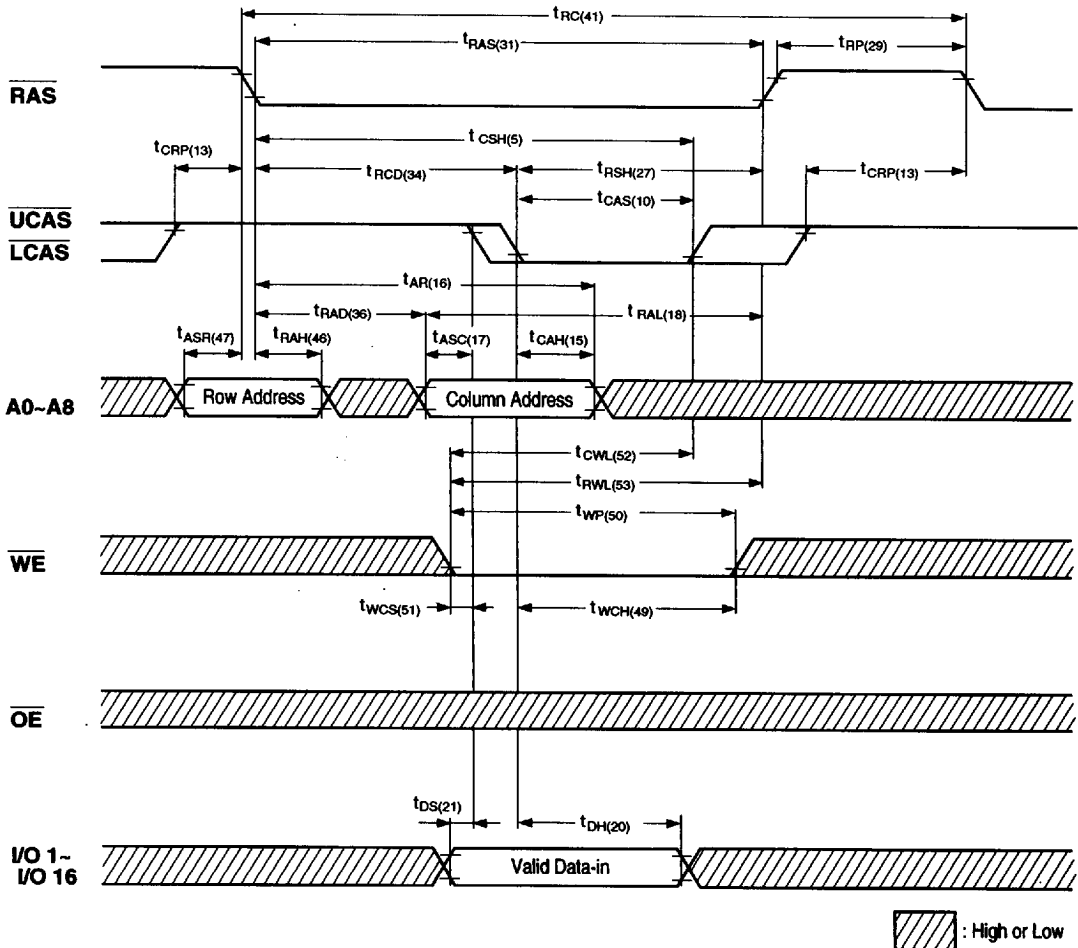
- Eight Initialization Cycles are required following a 200 μ s pause after Power Up. These Initialization Cycles may consist of any combination of the following : RAS only refresh Cycles, Read Cycles, Write Cycles, CAS before RAS refresh Cycles.
- AC measurements assume $t_T=3$ ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$ and with a load equivalent to two TTL loads and 100pF.
- $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
- Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
- Assumes three state test load (5pF and a 220 ohm to 1.3V Thevenin equivalent).
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- $t_{OFF}(\text{max.})$ defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
- t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$ and $t_{AWD} \geq t_{AWD}(\text{min.})$, the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
- These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in read-modify-write cycles.
- Access time is determined by the longer of t_{AA} , t_{CAC} , or t_{CPA} .
- $t_{ASC} \geq t_{CP}$ to achieve $t_{PC}(\text{min.})$ and $t_{CPA}(\text{max.})$ values.
- $t_{REF}=128$ msec for Long Refresh version (L version).

WORD READ CYCLE

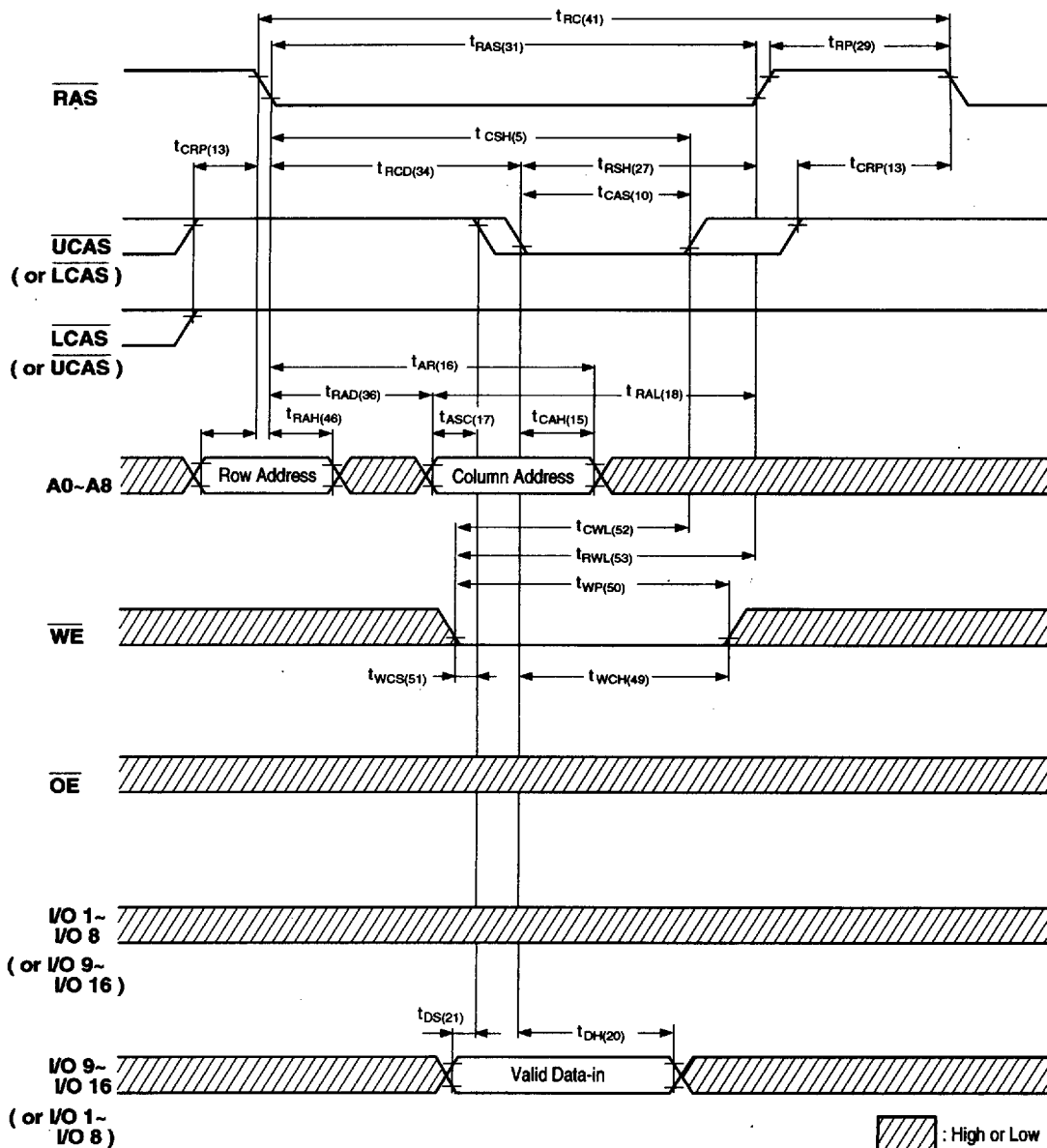


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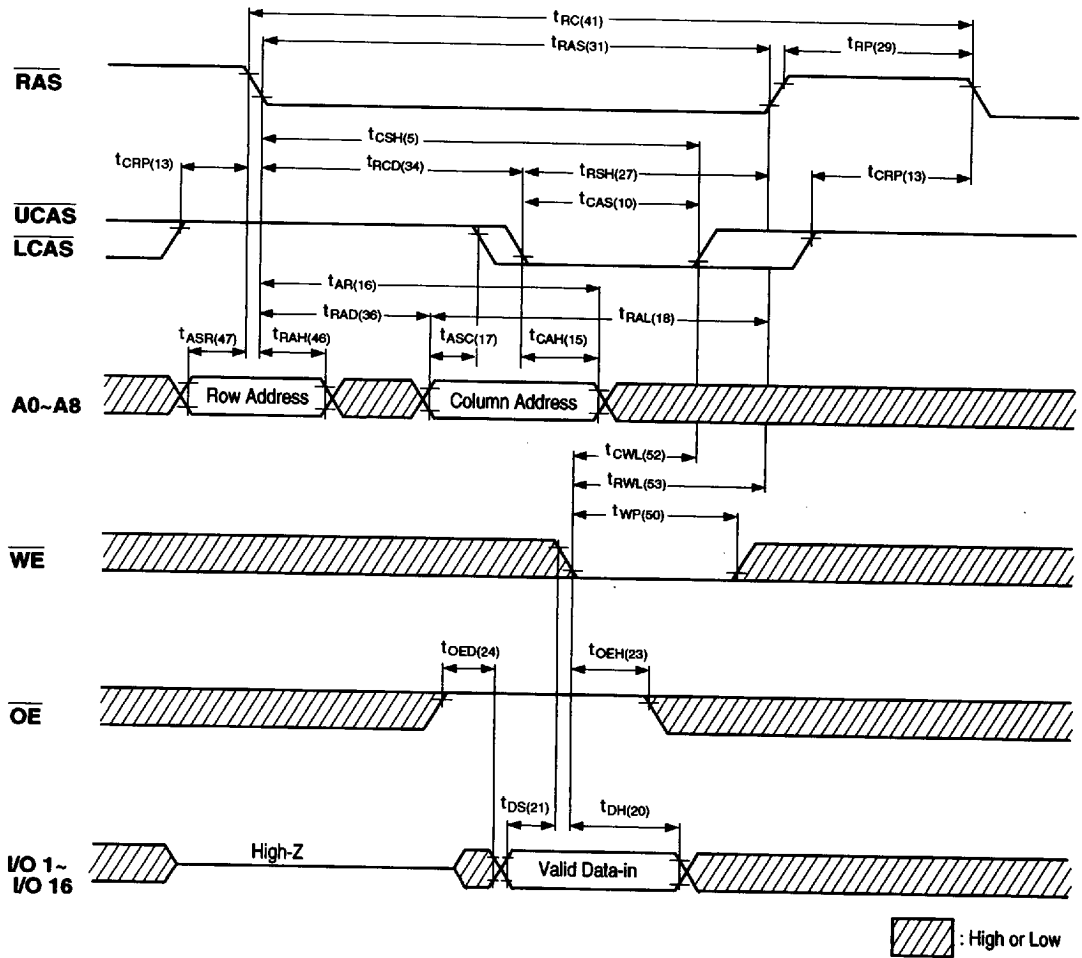
WORD WRITE CYCLE (EARLY WRITE)



BYTE WRITE CYCLE (EARLY WRITE)



WORD WRITE CYCLE (OE-CONTROLLED WRITE)

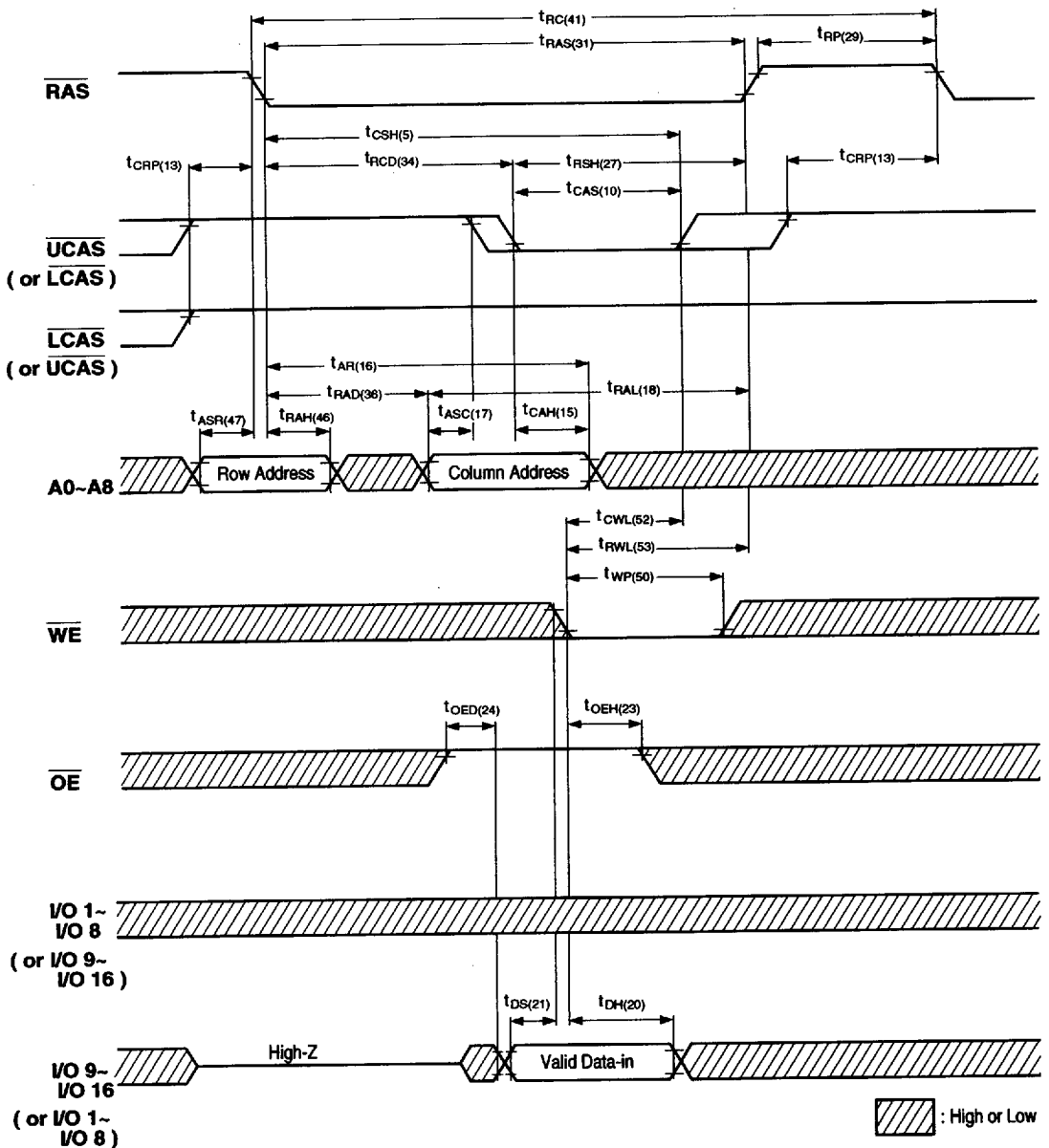


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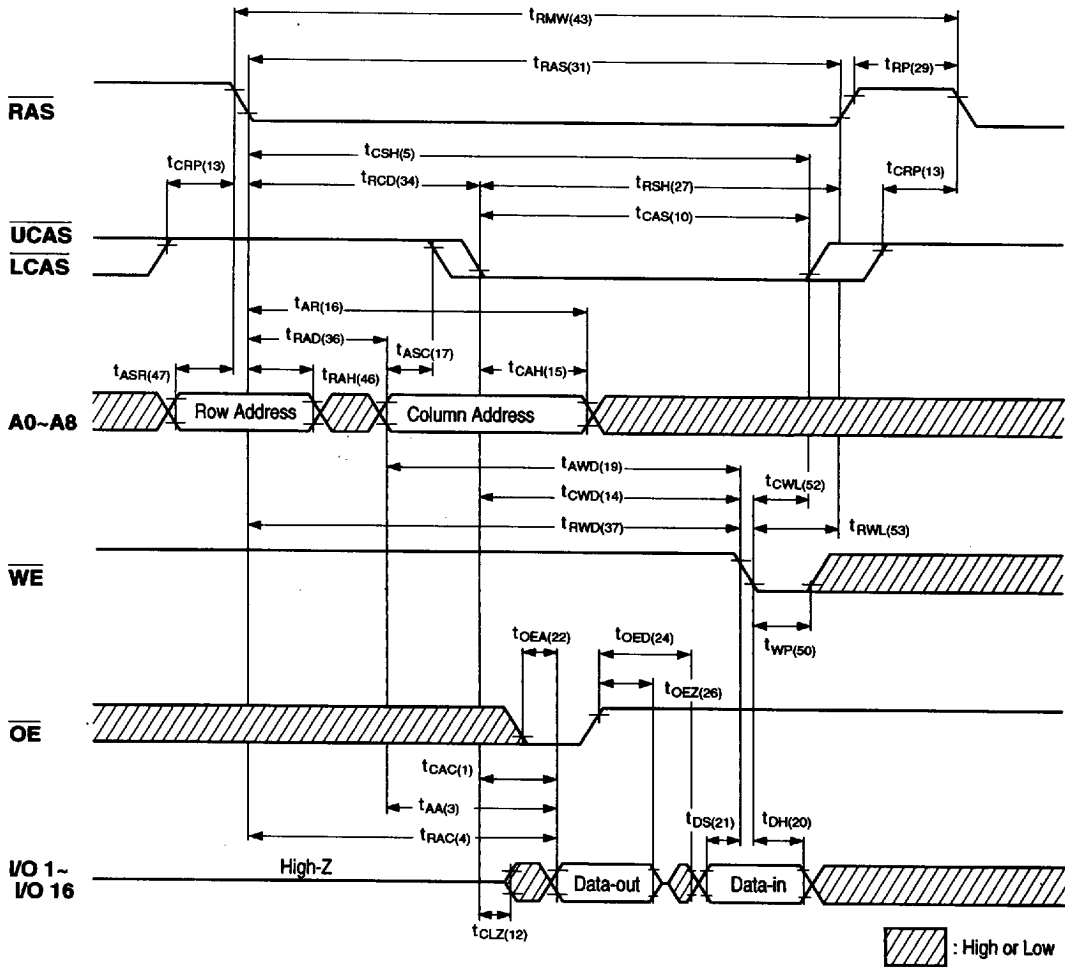
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BYTE WRITE CYCLE (OE-CONTROLLED WRITE)

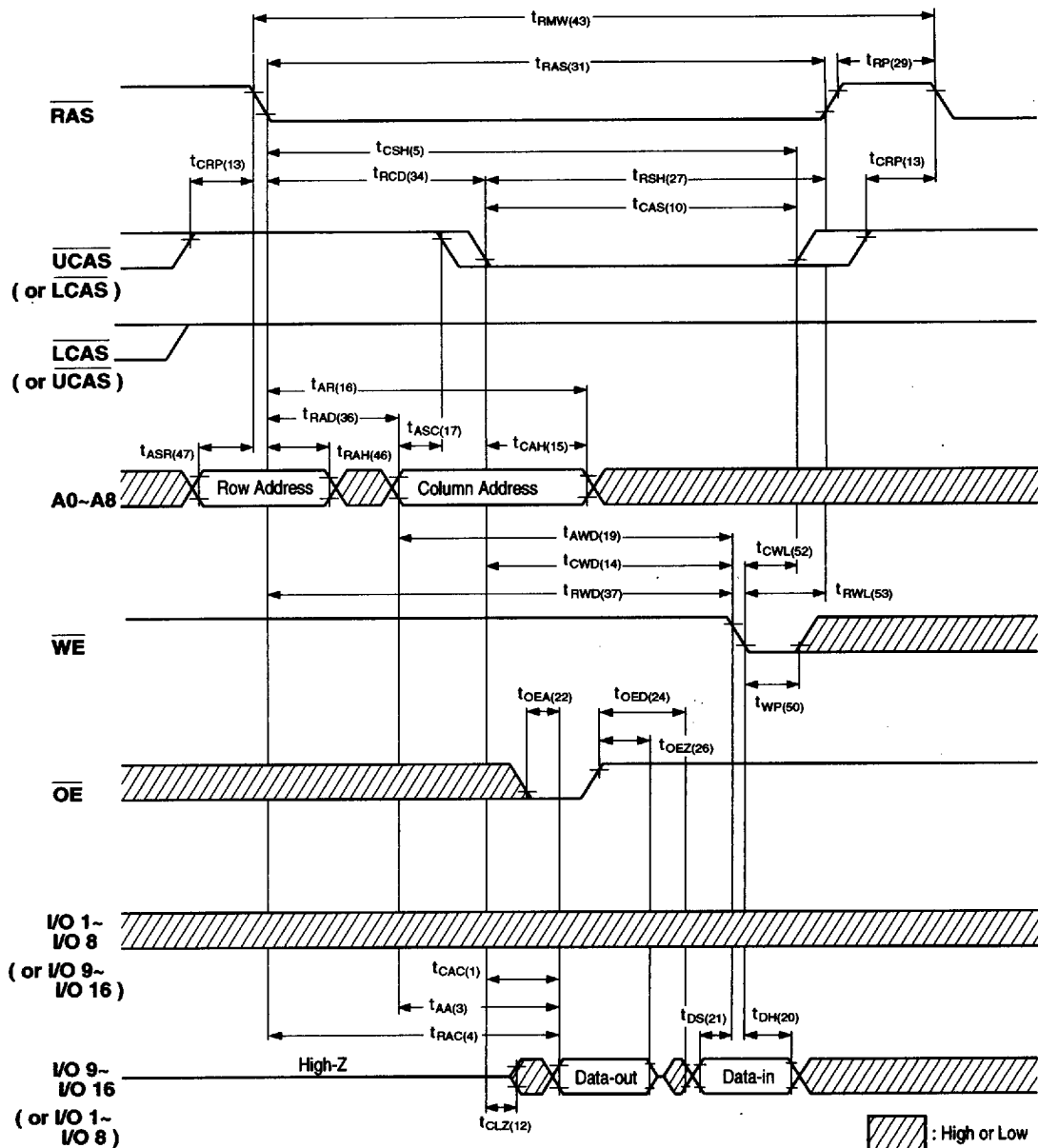


WORD READ-MODIFY-WRITE CYCLE

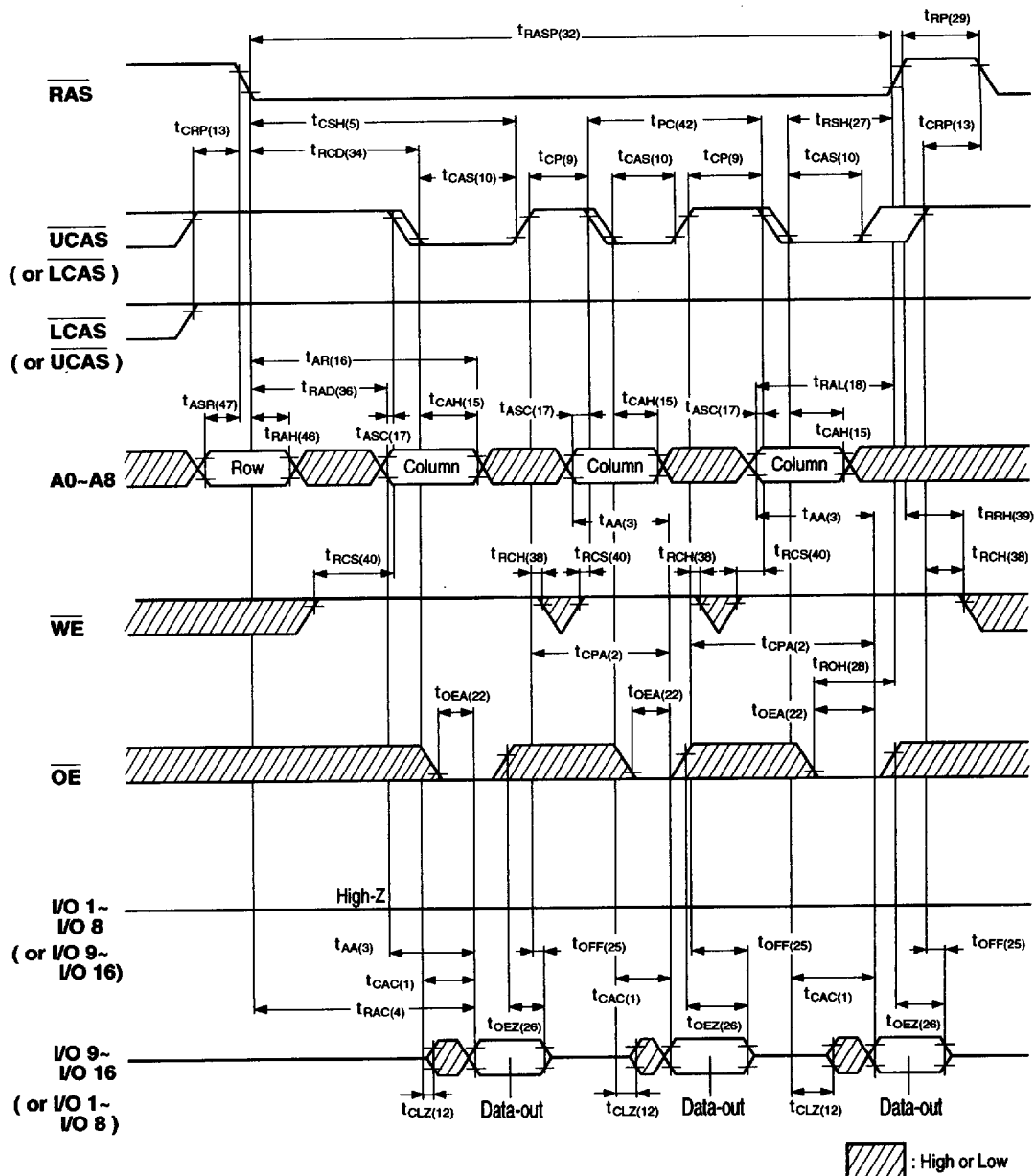


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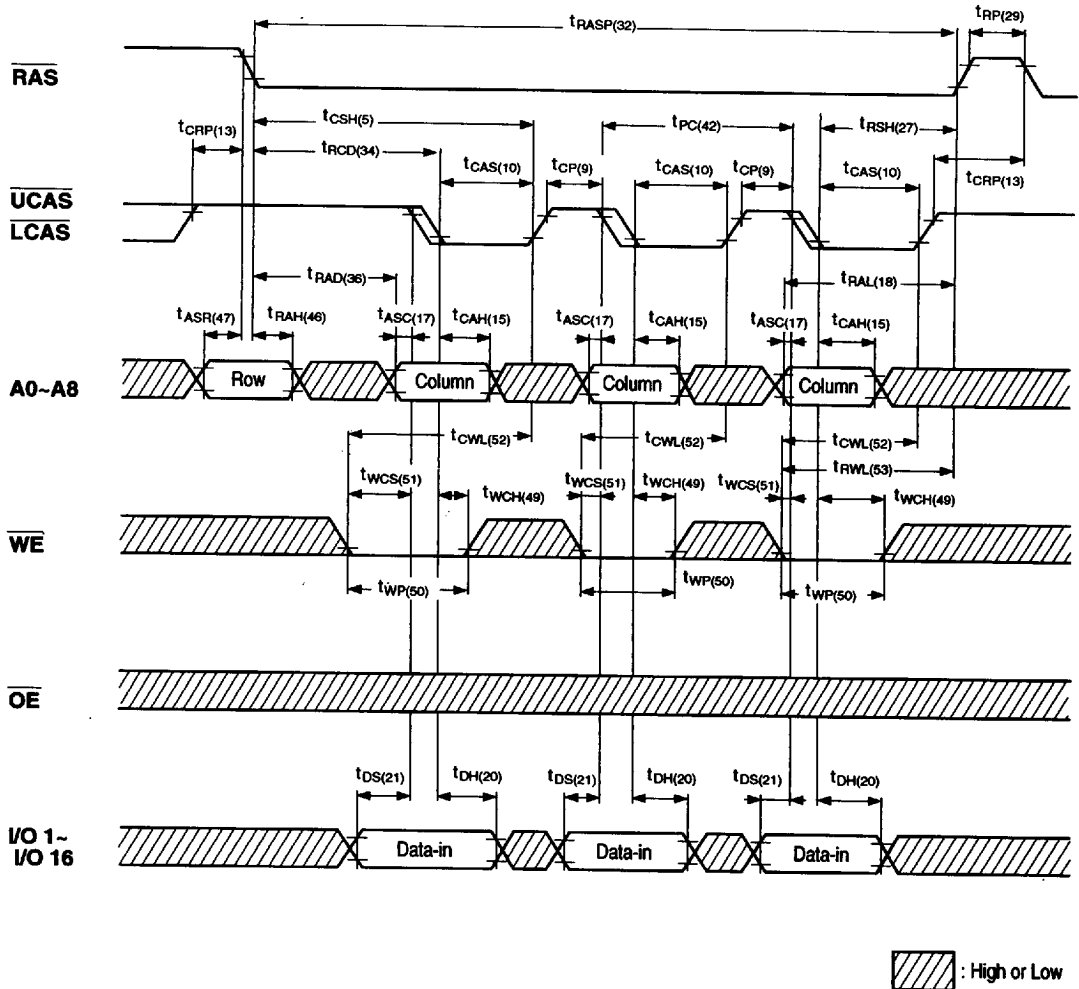
BYTE READ-MODIFY-WRITE CYCLE



FAST PAGE MODE BYTE READ CYCLE

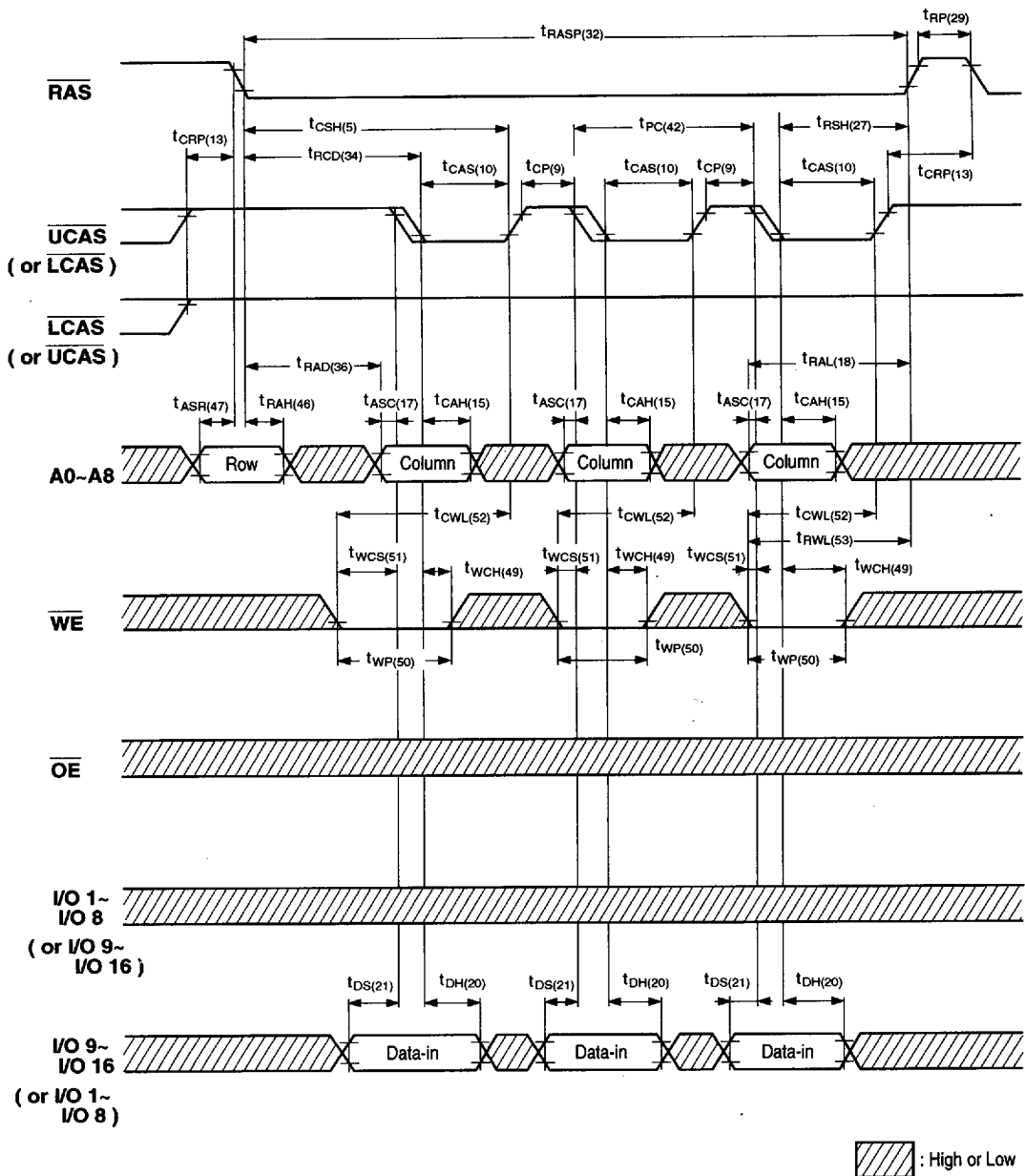


FAST PAGE MODE EARLY WORD WRITE CYCLE

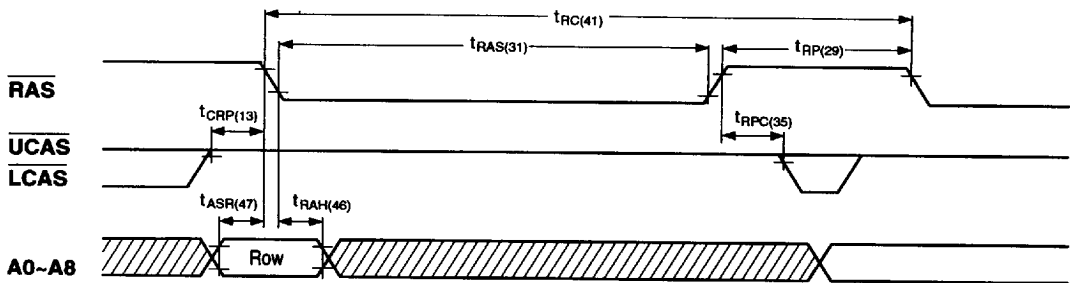


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FAST PAGE MODE EARLY BYTE WRITE CYCLE



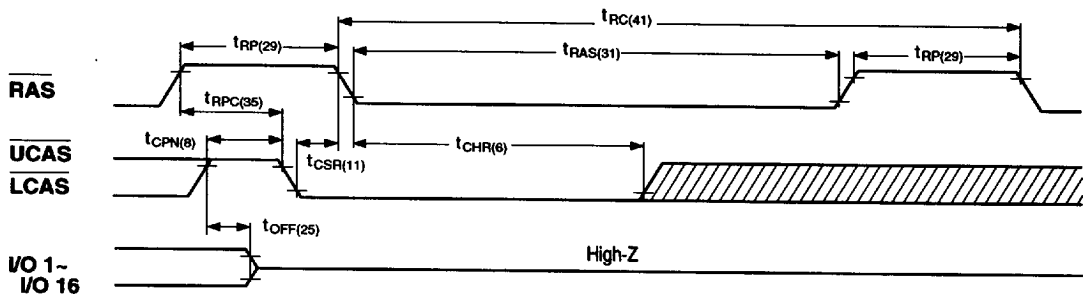
RAS ONLY REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

 : High or Low

CAS BEFORE RAS REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$, A0~A8 = Don't care.

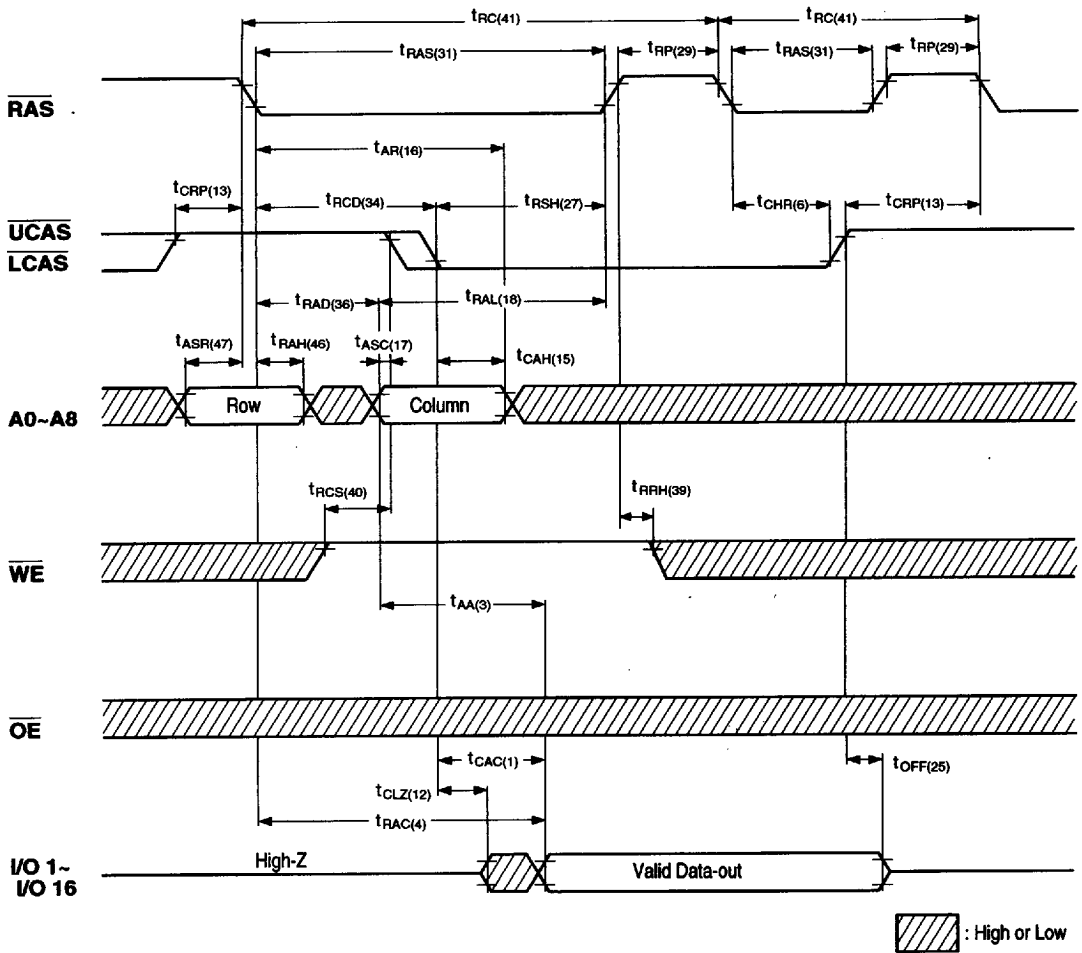
 : High or Low

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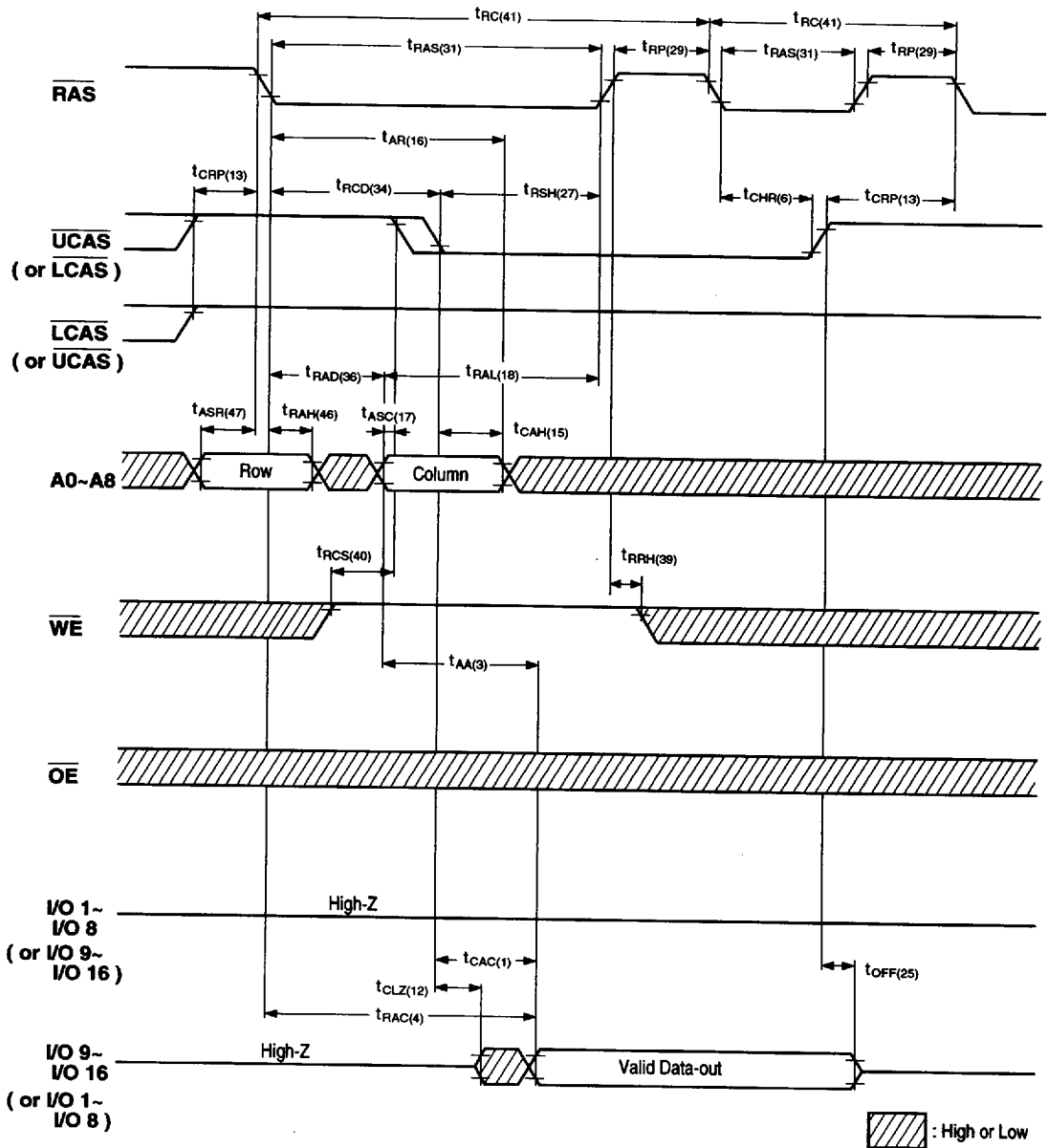
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HIDDEN REFRESH CYCLE (WORD READ)

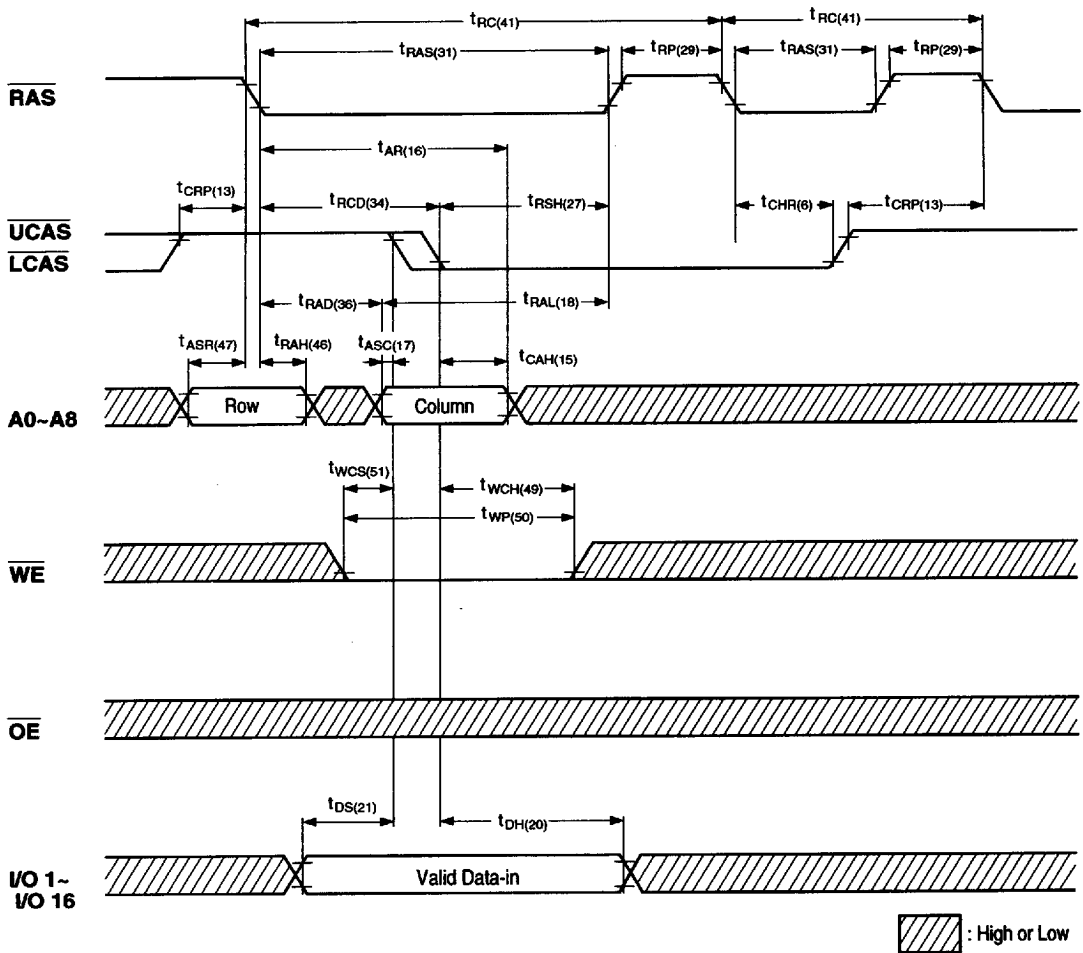


HIDDEN REFRESH CYCLE (BYTE READ)

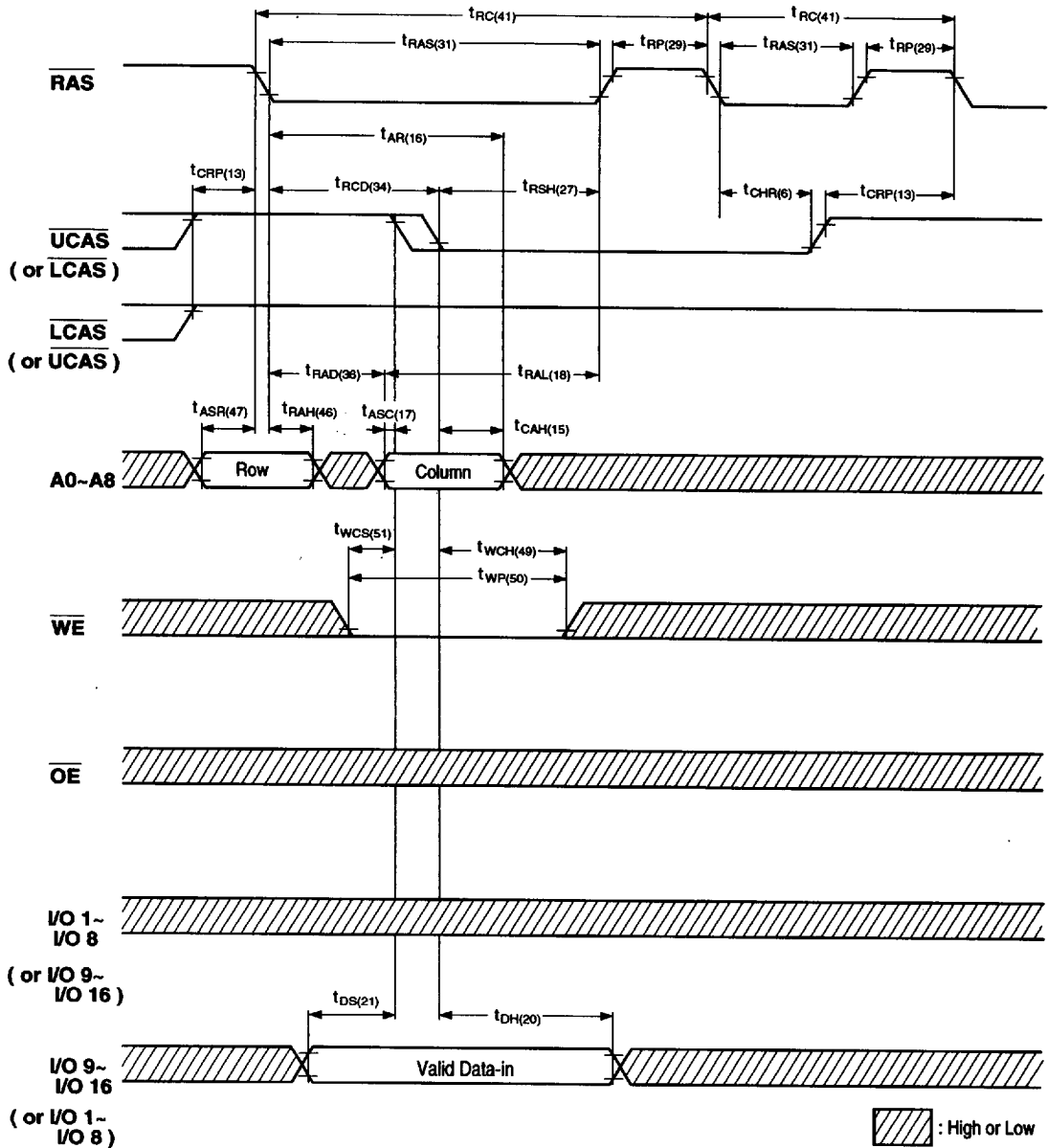


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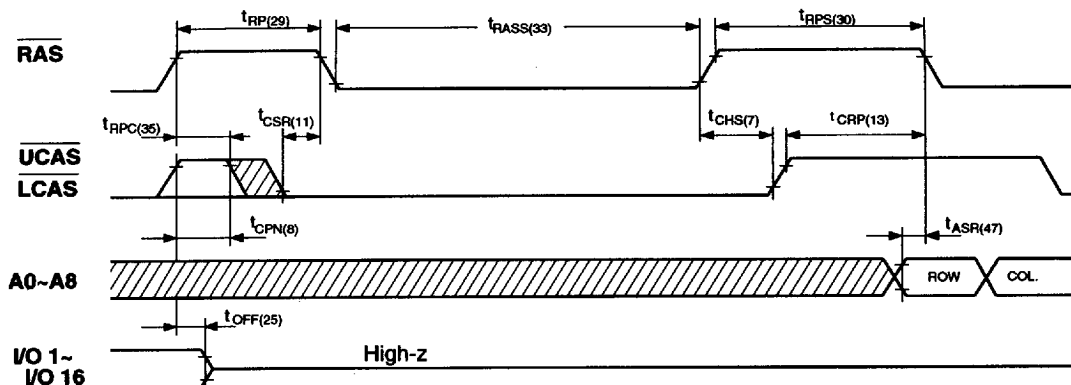
HIDDEN REFRESH CYCLE (EARLY WORD WRITE)



HIDDEN REFRESH CYCLE (EARLY BYTE WRITE)



SELF REFRESH MODE



Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$ = Don't care.

 : High or Low

■ The NN514260L/AL version has a Self Refresh Mode.

a. Entering the Self Refresh Mode:

The NN514260L/AL Self Refresh Mode is entered by using $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle and holding $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signal "low" longer than 300 μ s.

b. Continuing the Self Refresh Mode:

The Self Refresh Mode is continued by holding $\overline{\text{RAS}}$ "low" after entering the Self Refresh Mode. It does not depend on $\overline{\text{CAS}}$ being "high" or "low" after entering the Self Refresh Mode to continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:

The NN514260L/AL exits the Self Refresh Mode when the $\overline{\text{RAS}}$ signal is brought "high".

ORDERING INFORMATION

NN514260XXX(X) - XX

<u>SPEED</u>	45 : 45ns 50 : 50ns 60 : 60ns 70 : 70ns
<u>PACKAGE</u>	J : Plastic SOJ TT : Plastic TSOP TYPEII
<u>VERSION</u>	BLANK : Standard Version L : Long Refresh Version 128ms Refresh
<u>DESIGN CODE</u>	BLANK : NN514260 series A : NN414260A series
<u>MODE</u>	4260 : Fast Page 2CAS ,256K x 16 ,512refresh cycle

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