

DESCRIPTION

The NN514260/A series is a high performance CMOS Dynamic Random Access Memory organized as 262,144 words by 16 bits. The NN514260/A series is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN514260/A series features a high speed page mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

The outputs are tri-stated by $\overline{\text{CAS}}$ which, in essence, acts as an output enable independent of $\overline{\text{RAS}}$ with very fast $\overline{\text{CAS}}$ to output access time.

Refresh is accomplished by performing $\overline{\text{RAS}}$ only refresh cycles, hidden refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, or normal read or write cycles on the 512 address combinations of A0 to A8 during a 8 ms period.

Multiplexed address inputs permit The NN514260/A series to be packaged in a standard 40-pin plastic SOJ, 44-pin plastic TSOP TYPEII. The package sizes provide high system bit densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V $\pm$ 10% tolerance and direct interface with high performance TTL logic families.

FEATURES

- 262,144 × 16 bit Organization
- Single 5V $\pm$ 10% Power Supply
- Performance Ranges

(NN514260)

Parameter	-45	-50	-60	-70
Max. $\overline{\text{RAS}}$ Access Time (t_{RAC})	45ns	50ns	60ns	70ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	15ns	15ns	15ns	20ns
Max. Column Address Access Time (t_{AA})	25ns	27ns	30ns	35ns
Min. Read/Write Cycle Time (t_{RC})	80ns	90ns	110ns	130ns

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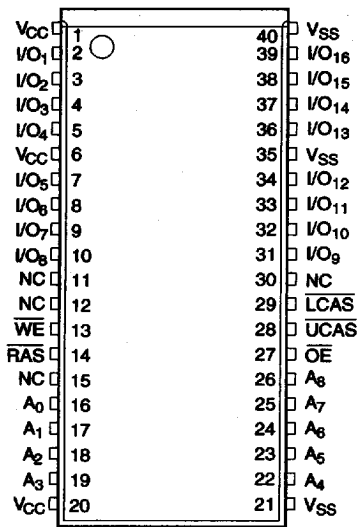
Parameter	-35	-40	-45	-50	-60
Max. $\overline{\text{RAS}}$ Access Time (t_{RAC})	35ns	40ns	45ns	50ns	60ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	10ns	12ns	13ns	13ns	15ns
Max. Column Address Access Time (t_{AA})	17ns	20ns	25ns	25ns	30ns
Min. Read/Write Cycle Time (t_{RC})	60ns	70ns	80ns	90ns	110ns

- Fast Page Mode Operation
- Separate $\overline{\text{CAS}}$ ($\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$) for Byte Selection
- Byte Read/Write Mode Operation
- Low Power Operation
 - Low Standby Current (CMOS level inputs)
 - Standard 1mA
 - L version 100 μ A
- 512 Refresh Cycles
 - Standard distributed across 8ms
 - L version distributed across 128ms
- Self Refresh Mode (L version)
- All inputs/Outputs and Clocks fully TTL and CMOS compatible
- Refresh Modes
 - $\overline{\text{RAS}}$ only
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$
 - Hidden Refresh
- High Reliability Package
 - Plastic 40pin SOJ (P40SJ-2B)
 - Plastic 44pin TSOP TYPEII (P44/40TP-3B)
 - (P44/40TP-3B-L)*

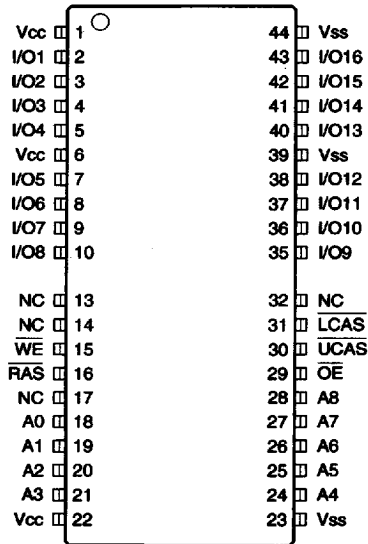
*Note: Only for NN514260A

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PIN CONFIGURATION (TOP VIEW)



40-pin SOJ (400mil)
 P40SJ-2B



44/40-pin TSOP TYPE (II)
 (400mil)
 P44/40TP-3B
 P44/40TP-3B-L*

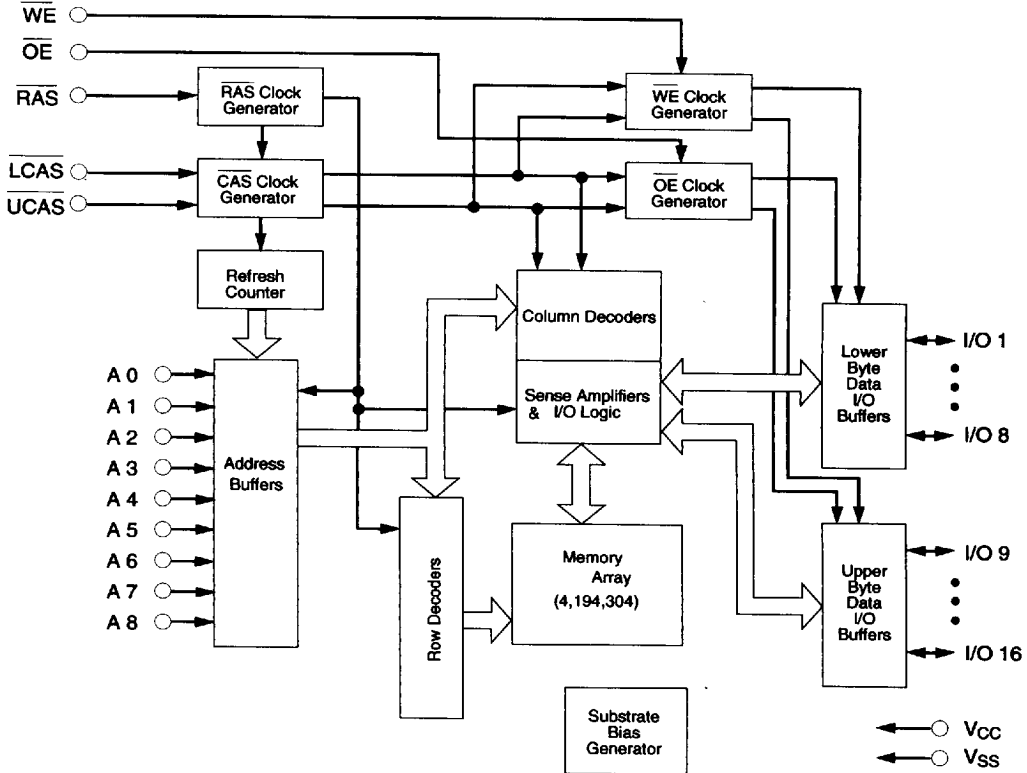
*Note: Only for NN514260A

PIN NAMES

A0-A8	Address Inputs
RAS	Row Address Strobe
UCAS	Column Address Strobe Upper Byte Control
LCAS	Column Address Strobe Lower Byte Control
OE	Output Enable
I/O1~I/O16	Data-in / Data-out
WE	Write Enable
V _{CC}	+5V Supply
V _{SS}	Ground
NC	No Connection

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FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V _{SS}	V _{in} , V _{out}	-1 to 7	V
Voltage on V _{CC} Relative to V _{SS}	V _{CC}	-1 to 7	V
Storage Temperature (Plastic)	T _{stg}	-55 to +125	°C
Power Dissipation	P _d	1.0	W
Ambient Operating Temperature	T _a	0 to +70	°C
Short Circuit Output Current	I _{out}	50	mA

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{SS}	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage, All Inputs	2.4	—	6.5	V
V _{IL}	Input Low Voltage, All Inputs	-0.5	—	0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS} unless otherwise specified.

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DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%)
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SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I _{CC1}	Operating Current	-45 -50 -60 -70		180 160 150 130	mA mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS, Address cycling	1, 2
I _{CC2}	Standby Current			1.0	mA	RAS = CAS ≥ (V _{CC} - 0.2V)	
				2.0	mA	RAS = CAS ≥ V _{IH}	
I _{CC3}	Refresh Current (RAS only refresh)			100	μA	RAS = CAS ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC3}	Refresh Current (RAS only refresh)	-45 -50 -60 -70		180 160 150 130	mA mA mA mA	t _{RC} = t _{RC} (min.) RAS cycling, CAS = V _{IH}	1
I _{CC4}	Fast Page Mode Current	-45		100	mA	t _{PC} = t _{PC} (min.)	1,2
		-50		90	mA	RAS = V _{IL}	
		-60		80	mA	CAS, Address cycling	
		-70		70	mA		
I _{CC5}	Refresh Current (CAS before RAS refresh)	-45		180	mA	t _{RC} = t _{RC} (min.)	1
		-50		160	mA	RAS, CAS cycling	
		-60		150	mA		
		-70		130	mA		
I _{CC6}	Refresh Current (L version : CAS before RAS refresh)			150	μA	512 cycles / 128ms t _{RAS} ≤ 200ns, WE ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC7}	Self Refresh Mode Current (L version)			150	μA	RAS = CAS ≤ (V _{SS} + 0.2V) All other input high levels are (V _{CC} - 0.2V) or input low levels are (V _{SS} + 0.2V)	
I _{IL1}	Input Leakage Current (Any input pin)		-10	10	μA	0V ≤ V _{IH} ≤ 5.5V, Others = 0V	
I _{IOL}	Output Leakage Current (For high impedance state)		-10	10	μA	RAS ≥ V _{IH} (min.), CAS ≥ V _{IH} (min.) 0V ≤ V _{OUT} ≤ 5.5V	
V _{OH}	Output High Voltage		2.4		V	I _{OH} = -5.0 mA	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2 mA	

Notes: 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.

2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{IN1}	Address(A0 ~ A8)	—	5	pF
C _{IN2}	RAS, UCAS, LCAS, WE, OE	—	5	pF
C _{OUT}	I/O1 ~ I/O16	—	7	pF

DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%)
(NN514260A)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I _{CC1}	Operating Current	-35 -40 -45 -50 -60		180 160 140 120 100	mA mA mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS, Address cycling	1, 2
I _{CC2}	Standby Current			1.0	mA	RAS = CAS ≥ (V _{CC} - 0.2V)	
				2.0	mA	RAS = CAS ≥ V _{IH}	
	Standby Current (L version)			150	μA	RAS = CAS ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC3}	Refresh Current (RAS only refresh)	-35 -40 -45 -50 -60		180 160 140 120 100	mA mA mA mA mA	t _{RC} = t _{RC} (min.) RAS cycling, CAS = V _{IH}	1
I _{CC4}	Fast Page Mode Current	-35 -40 -45 -50 -60		80 70 60 50 40	mA mA mA mA mA	t _{PC} = t _{PC} (min.) RAS = V _{IL} CAS, Address cycling	1, 2
I _{CC5}	Refresh Current (CAS before RAS refresh)	-35 -40 -45 -50 -60		180 160 140 120 100	mA mA mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS cycling	1
I _{CC6}	Refresh Current (L version : CAS before RAS refresh)			200	μA	512 cycles / 128ms t _{RAS} ≤ 200ns, WE ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC7}	Self Refresh Mode Current (L version)			200	μA	RAS = CAS ≤ (V _{SS} + 0.2V) All other input high levels are (V _{CC} - 0.2V) or input low levels are (V _{SS} + 0.2V)	
I _{IL1}	Input Leakage Current (Any input pin)		-10	10	μA	0V ≤ V _{IH} ≤ 5.5V, Others = 0V	
I _{IL0}	Output Leakage Current (For high impedance state)		-10	10	μA	RAS ≥ V _{IH} (min.), CAS ≥ V _{IH} (min.) 0V ≤ V _{OUT} ≤ 5.5V	
V _{OH}	Output High Voltage		2.4		V	I _{OH} = -5.0 mA	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 4.2 mA	

- Notes: 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 5.0V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{IN1}	Address(A0 ~ A8)	—	5	pF
C _{IN2}	RAS, UCAS, LCAS, WE, OE	—	5	pF
C _{OUT}	I/O1~I/O16	—	7	pF

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AC ELECTRICAL CHARACTERISTICS

Test conditions : $V_{IH}/V_{IL} = 2.4V / 0.8V$ $V_{OH}/V_{OL} = 2.0V / 0.8V$ output loading $C_L = 100pF + 2TTL$

Operating conditions : ($0^\circ C \leq T_a \leq 70^\circ C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$) (NOTES 3, 4, 5)

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NO.	NOTES		PARAMETER	-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from CAS	—	15	—	15	—	15	—	20	ns	6,13
2	t_{CH2QV}	t_{CPA}	Access Time from CAS Precharge	—	30	—	32	—	35	—	40	ns	13,14
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	25	—	27	—	30	—	35	ns	7,13
4	t_{RL1QV}	t_{RAC}	Access Time from RAS	—	45	—	50	—	60	—	70	ns	6,7
5	t_{RL1CH1}	t_{CSH}	CAS Hold Time	45	—	50	—	60	—	70	—	ns	
6	t_{RL1CH1}	t_{CHR}	CAS Hold Time (CAS before RAS Refresh)	8	—	8	—	10	—	10	—	ns	
7	t_{RL1CX}	t_{CHS}	CAS Precharge Time (Self Refresh Mode)	-50	—	-50	—	-50	—	-50	—	ns	
8	t_{CH2CL2}	t_{CPN}	CAS Precharge Time (CAS before RAS Refresh)	10	—	10	—	10	—	10	—	ns	
9	t_{CH2CL2}	t_{CP}	CAS Precharge Time (Fast Page Mode)	5	—	5	—	5	—	5	—	ns	14
10	t_{CL1CH1}	t_{CAS}	CAS Pulse Width	13	100K	13	100K	15	100K	20	100K	ns	
11	t_{CL1RL2}	t_{CSR}	CAS Setup Time (CAS before RAS Refresh)	5	—	5	—	5	—	5	—	ns	
12	t_{CL1QX}	t_{CLZ}	CAS to Output in Low-Z	0	—	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	CAS to RAS Precharge Time	5	—	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	CAS to WE Delay Time	35	—	35	—	35	—	50	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	8	—	8	—	10	—	15	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to RAS	30	—	35	—	40	—	40	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	ns	14
18	t_{AVRH1}	t_{RAL}	Column Address to RAS Lead Time	22	—	24	—	30	—	35	—	ns	
19	t_{AVWL2}	t_{AWD}	Column Address to WE Delay Time	48	—	50	—	50	—	65	—	ns	11
20	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	8	—	8	—	10	—	10	—	ns	12
21	t_{OVCL2} t_{OVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	0	—	ns	12
22	t_{OL1QV}	t_{OEA}	OE Access Time	—	13	—	15	—	15	—	20	ns	
23	t_{WL1OL2}	t_{OEH}	OE Command Hold Time	8	—	8	—	10	—	20	—	ns	
24	t_{CH2QV}	t_{OED}	OE to Data Delay Time	7	—	8	—	10	—	10	—	ns	
25	t_{CH2QZ}	t_{OFF}	Output Buffer Turn-off Delay Time	0	13	0	13	0	15	0	20	ns	10
26	t_{OH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to OE	0	10	0	10	0	15	0	15	ns	
27	t_{CL1RH1}	t_{RSH}	RAS Hold Time	13	—	13	—	15	—	20	—	ns	
28	t_{OL1RH1}	t_{ROH}	RAS Hold Time Referenced to OE	8	—	8	—	10	—	10	—	ns	
29	t_{RH2RL2}	t_{RP}	RAS Precharge Time	25	—	25	—	30	—	40	—	ns	
30	t_{RH2RL2}	t_{RPS}	RAS Precharge Time (Self Refresh Mode)	80	—	90	—	110	—	130	—	ns	
31	t_{RL1RH1}	t_{RAS}	RAS Pulse Width	45	100K	50	100K	60	100K	70	100K	ns	
32	t_{RL1RH1}	t_{RASP}	RAS Pulse Width (Fast Page Mode)	45	100K	50	100K	60	100K	70	100K	ns	
33	t_{RL1RH1}	t_{RASS}	RAS Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	300	—	μs	
34	t_{RL1CL1}	t_{RCD}	RAS to CAS Delay Time	13	30	13	35	13	45	13	50	ns	6
35	t_{RH2CL2}	t_{RPC}	RAS to CAS Precharge Time	10	—	10	—	10	—	10	—	ns	

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NO.	SYMBOL		PARAMETER	-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t _{RL1AV}	t _{RAD}	RAS to Column Address Delay Time	11	20	11	23	11	30	11	35	ns	7
37	t _{RL1WL2}	t _{RWD}	RAS to WE Delay Time	75	—	80	—	85	—	100	—	ns	11
38	t _{CH2WL2}	t _{RCH}	Read Command Hold Time	0	—	0	—	0	—	0	—	ns	9
39	t _{RH2WL2}	t _{RRH}	Read Command Hold Time Referenced to RAS	5	—	5	—	5	—	5	—	ns	9
40	t _{WH2CL2}	t _{RCS}	Random Command Setup Time	0	—	0	—	0	—	0	—	ns	
41	t _{RL2RL2}	t _{RC}	Random Read or Write Cycle Time	80	—	90	—	110	—	130	—	ns	
42	t _{CL2CL2}	t _{PC}	Read or Write Cycle Time (Fast Page Mode)	30	—	33	—	40	—	45	—	ns	13,14
43	t _{RL2RL2}	t _{RMW}	Read-Modify-Write Cycle Time	120	—	125	—	135	—	185	—	ns	
44	t _{CL2CL2}	t _{PRMW}	Read-Modify-Write Cycle Time (Fast Page Mode)	57	—	57	—	66	—	100	—	ns	13,14
45	t _{REF}	t _{REF}	Refresh Period	—	8	—	8	—	8	—	8	ms	15
46	t _{RL1AX}	t _{RAH}	Row Address Hold Time	8	—	8	—	8	—	8	—	ns	
47	t _{AVRL2}	t _{ASR}	Row Address Setup Time	0	—	0	—	0	—	0	—	ns	
48	t _T	t _T	Transition Time (Rise and Fall)	2	50	2	50	2	50	2	50	ns	4,5
49	t _{CL1WH1}	t _{WCH}	Write Command Hold Time	8	—	8	—	10	—	15	—	ns	
50	t _{WL1WH1}	t _{WP}	Write Command Pulse Width	8	—	8	—	10	—	15	—	ns	
51	t _{WL1CL2}	t _{WCS}	Write Command Setup Time	0	—	0	—	0	—	0	—	ns	11
52	t _{WL1CH1}	t _{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	13	—	13	—	15	—	20	—	ns	
53	t _{WL1RH1}	t _{RWL}	Write Command to $\overline{\text{RAS}}$ Lead Time	13	—	13	—	15	—	20	—	ns	

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A.C. ELECTRICAL CHARACTERISTICS

Test conditions : $V_{IH}/V_{IL} = 2.4V/0.8V$ $V_{OH}/V_{OL} = 2.0V/0.8V$ output loading $C_L = 50pF + 1TTL$

Operating conditions : ($0^\circ C \leq T \leq 70^\circ C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$) (NOTES 3, 4, 5)

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NO.	NOTES		PARAMETER	-35		-40		-45		-50		-60		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from CAS	—	10	—	12	—	15	—	15	—	15	ns	6,13
2	t_{CH2QV}	t_{CPA}	Access Time from CAS Precharge	—	25	—	28	—	30	—	32	—	35	ns	13,14
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	17	—	20	—	25	—	27	—	30	ns	7,13
4	t_{RL1QV}	t_{RAC}	Access Time from RAS	—	35	—	40	—	45	—	50	—	60	ns	6,7
5	t_{RL1CH1}	t_{CSH}	CAS Hold Time	35	—	40	—	45	—	50	—	60	—	ns	
6	t_{RL1CH1}	t_{CHR}	CAS Hold Time (CAS before RAS Refresh)	8	—	8	—	8	—	8	—	10	—	ns	
7	t_{RL1CX}	t_{CHS}	CAS Precharge Time (Self Refresh Mode)	-50	—	-50	—	-50	—	-50	—	-50	—	ns	
8	t_{CH2CL2}	t_{CPN}	CAS Precharge Time (CAS before RAS Refresh)	10	—	10	—	10	—	10	—	10	—	ns	
9	t_{CH2CL2}	t_{CP}	CAS Precharge Time (Fast Page Mode)	5	—	5	—	5	—	5	—	5	—	ns	14
10	t_{CL1CH1}	t_{CAS}	CAS Pulse Width	10	100K	12	100K	13	100K	13	100K	15	100K	ns	
11	t_{CL1RL2}	t_{CSR}	CAS Setup Time (CAS before RAS Refresh)	5	—	5	—	5	—	5	—	5	—	ns	
12	t_{CL1QX}	t_{CLZ}	CAS to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	CAS to RAS Precharge Time	5	—	5	—	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	CAS to WE Delay Time	30	—	32	—	35	—	35	—	35	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	5	—	5	—	8	—	8	—	10	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to RAS	25	—	30	—	30	—	35	—	40	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns	14
18	t_{AVRH1}	t_{RAL}	Column Address to RAS Lead Time	20	—	20	—	22	—	24	—	30	—	ns	
19	t_{AVWL2}	t_{AWD}	Column Address to WE Delay Time	35	—	38	—	48	—	50	—	50	—	ns	11
20	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	5	—	5	—	8	—	8	—	10	—	ns	12
21	t_{DVCL2} t_{DWWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	0	—	0	—	ns	12
22	t_{OL1QV}	t_{OEA}	OE Access Time	—	10	—	12	—	13	—	15	—	15	ns	
23	t_{WL1OL2}	t_{OEH}	OE Command Hold Time	8	—	8	—	8	—	8	—	10	—	ns	
24	t_{CH2QV}	t_{OED}	OE to Data Delay Time	6	—	6	—	7	—	8	—	10	—	ns	
25	t_{CH2QV}	t_{OFF}	Output Buffer Turn-off Delay Time	0	8	0	10	0	13	0	13	0	15	ns	10
26	t_{CH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to OE	0	8	0	8	0	10	0	10	0	15	ns	
27	t_{CL1RH1}	t_{RSH}	RAS Hold Time	12	—	12	—	13	—	13	—	15	—	ns	
28	t_{OL1RH1}	t_{ROH}	RAS Hold Time Referenced to OE	8	—	8	—	8	—	8	—	10	—	ns	
29	t_{RH2RL2}	t_{RP}	RAS Precharge Time	23	—	25	—	25	—	25	—	30	—	ns	
30	t_{RH2RL2}	t_{RPS}	RAS Precharge Time (Self Refresh Mode)	60	—	70	—	80	—	90	—	110	—	ns	
31	t_{RL1RH1}	t_{RAS}	RAS Pulse Width	35	100K	40	100K	45	100K	50	100K	60	100K	ns	
32	t_{RL1RH1}	t_{RASP}	RAS Pulse Width (Fast Page Mode)	35	100K	40	100K	45	100K	50	100K	60	100K	ns	
33	t_{RL1RH1}	t_{RASS}	RAS Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	300	—	300	—	μs	
34	t_{RL1CL1}	t_{RCD}	RAS to CAS Delay Time	10	25	12	28	13	30	13	35	13	45	ns	6

9005650 0001230 220

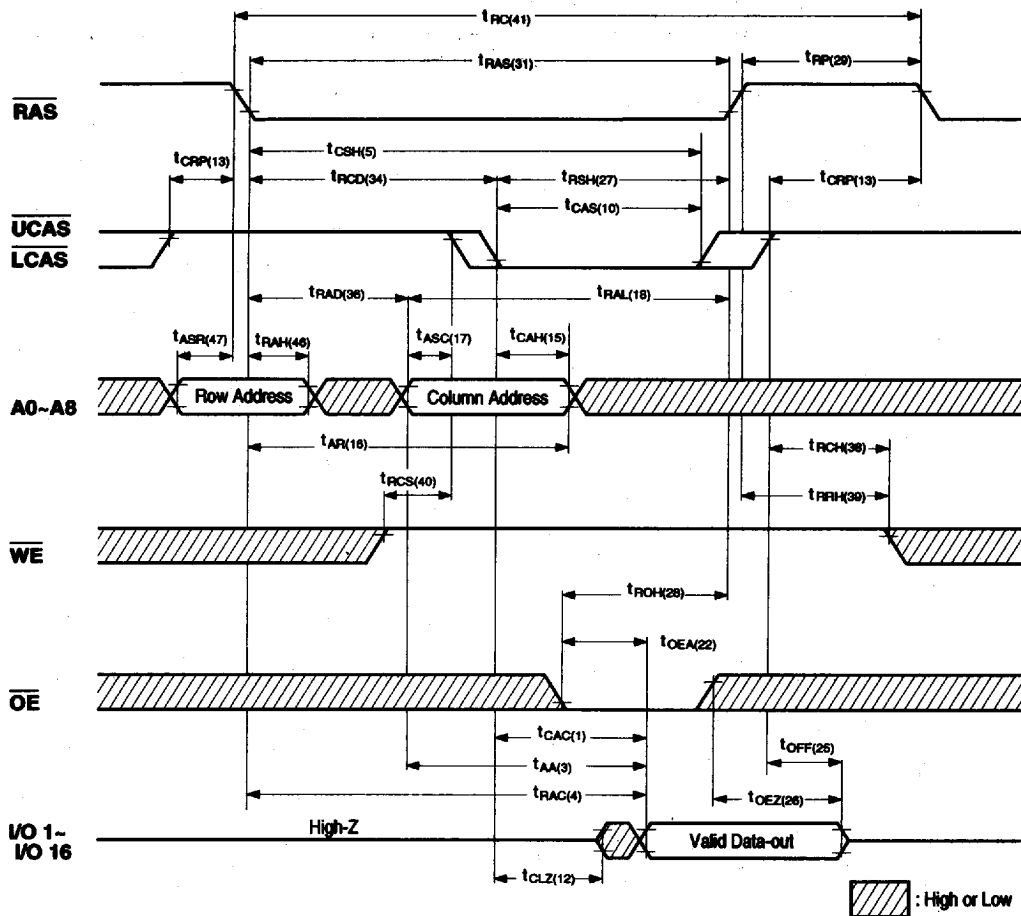
NO.	SYMBOL		PARAMETER	-35		-40		-45		-50		-60		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
35	t _{RH2CL2}	t _{RPC}	RAS to CAS Precharge Time	10	—	10	—	10	—	10	—	10	—	ns	
36	t _{RL1AV}	t _{RAD}	RAS to Column Address Delay Time	9	16	10	19	11	20	11	23	11	30	ns	7
37	t _{RL1WL2}	t _{RWD}	RAS to WE Delay Time	45	—	58	—	75	—	80	—	85	—	ns	11
38	t _{CH2WL2}	t _{RCH}	Read Command Hold Time	0	—	0	—	0	—	0	—	0	—	ns	9
39	t _{RH2WL2}	t _{RRH}	Read Command Hold Time Referenced to RAS	5	—	5	—	5	—	5	—	5	—	ns	9
40	t _{WH2CL2}	t _{RCS}	Random Command Setup Time	0	—	0	—	0	—	0	—	0	—	ns	
41	t _{RL2RL2}	t _{RC}	Random Read or Write Cycle Time	60	—	70	—	80	—	90	—	110	—	ns	
42	t _{CL2CL2}	t _{PC}	Read or Write Cycle Time (Fast Page Mode)	20	—	23	—	30	—	33	—	40	—	ns	13,14
43	t _{RL2RL2}	t _{RMW}	Read-Modify-Write Cycle Time	105	—	115	—	120	—	125	—	135	—	ns	
44	t _{CL2CL2}	t _{PRMW}	Read-Modify-Write Cycle Time (Fast Page Mode)	52	—	55	—	57	—	57	—	66	—	ns	13,14
45	t _{REF}	t _{REF}	Refresh Period	—	8	—	8	—	8	—	8	—	8	ms	15
46	t _{RL1AX}	t _{RAH}	Row Address Hold Time	7	—	7	—	8	—	8	—	8	—	ns	
47	t _{AVRL2}	t _{ASR}	Row Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns	
48	t _T	t _T	Transition Time (Rise and Fall)	2	50	2	50	2	50	2	50	2	50	ns	4,5
49	t _{CL1WH1}	t _{WCH}	Write Command Hold Time	5	—	5	—	8	—	8	—	10	—	ns	
50	t _{WL1WH1}	t _{WP}	Write Command Pulse Width	5	—	5	—	8	—	8	—	10	—	ns	
51	t _{WL1CL2}	t _{WCS}	Write Command Setup Time	0	—	0	—	0	—	0	—	0	—	ns	11
52	t _{WL1CH1}	t _{CWL}	Write Command to CAS Lead Time	12	—	12	—	13	—	13	—	15	—	ns	
53	t _{WL1RH1}	t _{RWL}	Write Command to RAS Lead Time	12	—	12	—	13	—	13	—	15	—	ns	

Notes: (NN514260/A/B)

- Eight Initialization Cycles are required following a 200μs pause after Power Up. These Initialization Cycles may consist of any combination of the following : RAS only refresh Cycles, Read Cycles, Write Cycles, CAS before RAS refresh Cycles.
- AC measurements assume t_T=3ns.
- V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
- Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
- Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
- Assumes three state test load (5pF and a 220 ohm to 1.3V Thevenin equivalent).
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- t_{OFF}(max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
- t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS}≥t_{WCS}(min.) , the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If t_{RWD}≥t_{RWD}(min.), t_{CWD}≥t_{CWD}(min.) and t_{AWD}≥t_{AWD}(min.), the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
- These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in read-modify-write cycles.
- Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{CPA}.
- t_{ASC}≥t_{CP} to achieve t_{PC}(min.) and t_{CPA}(max.) values.
- t_{REF}=128msec for Long Refresh version (L version).

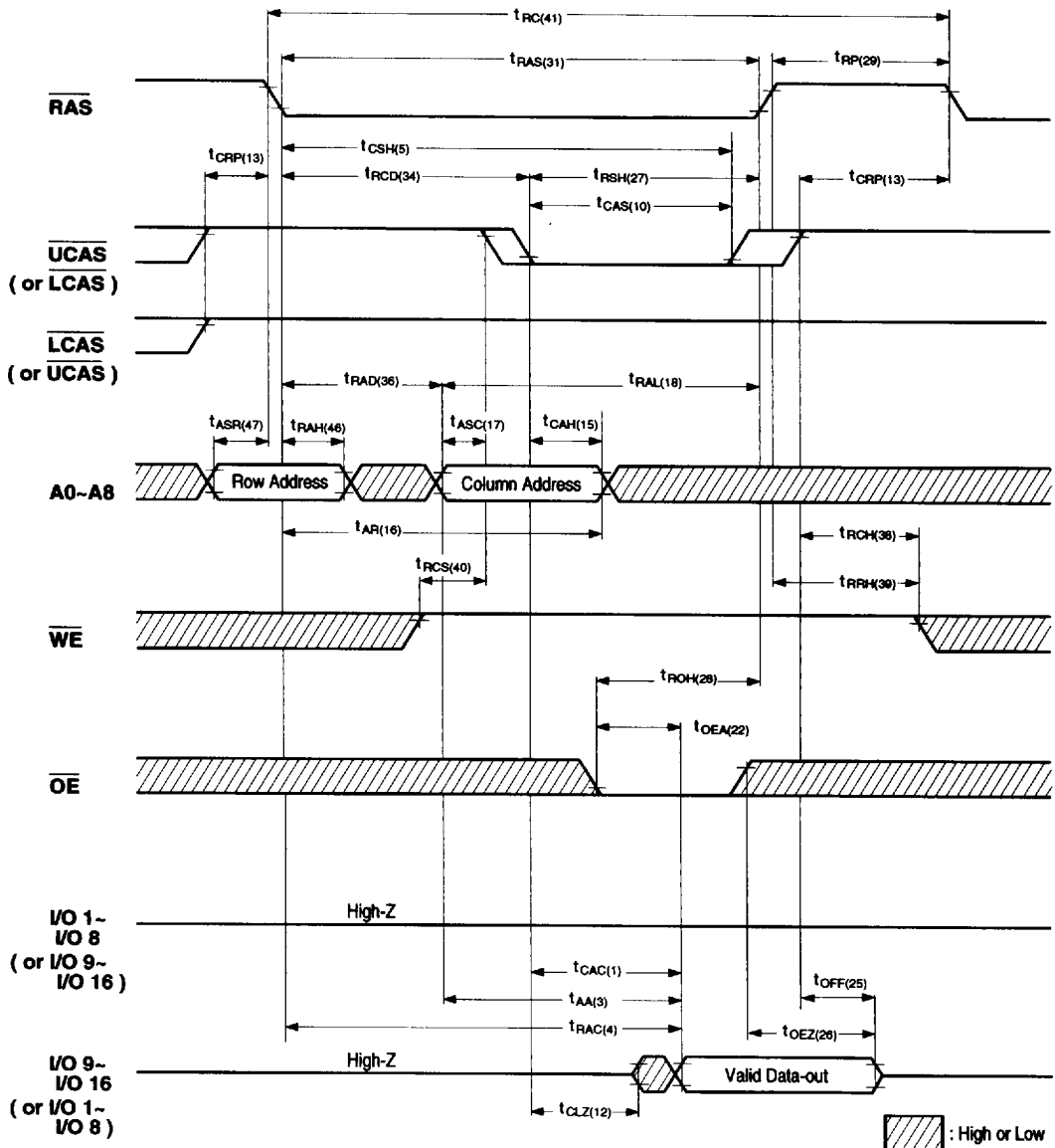
9005650 0001231 167

WORD READ CYCLE



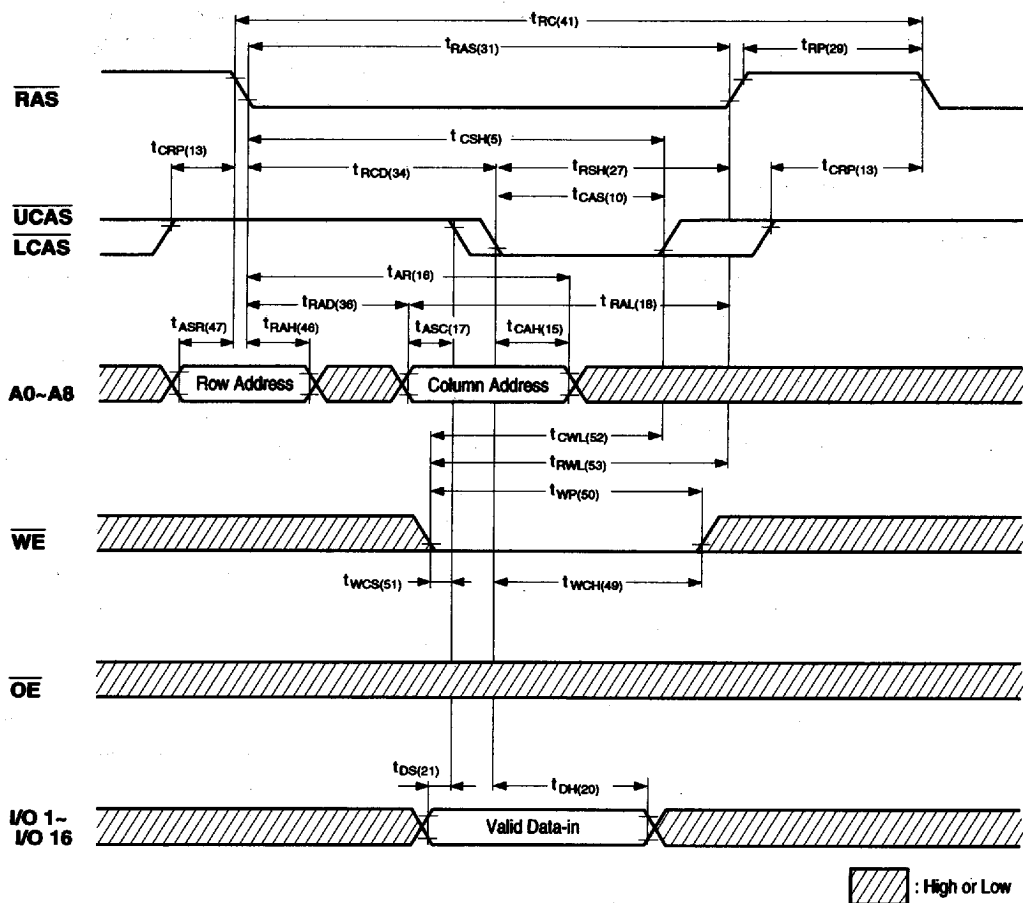
9005650 0001232 0T3

BYTE READ CYCLE



9005650 0001233 T3T

WORD WRITE CYCLE (EARLY WRITE)

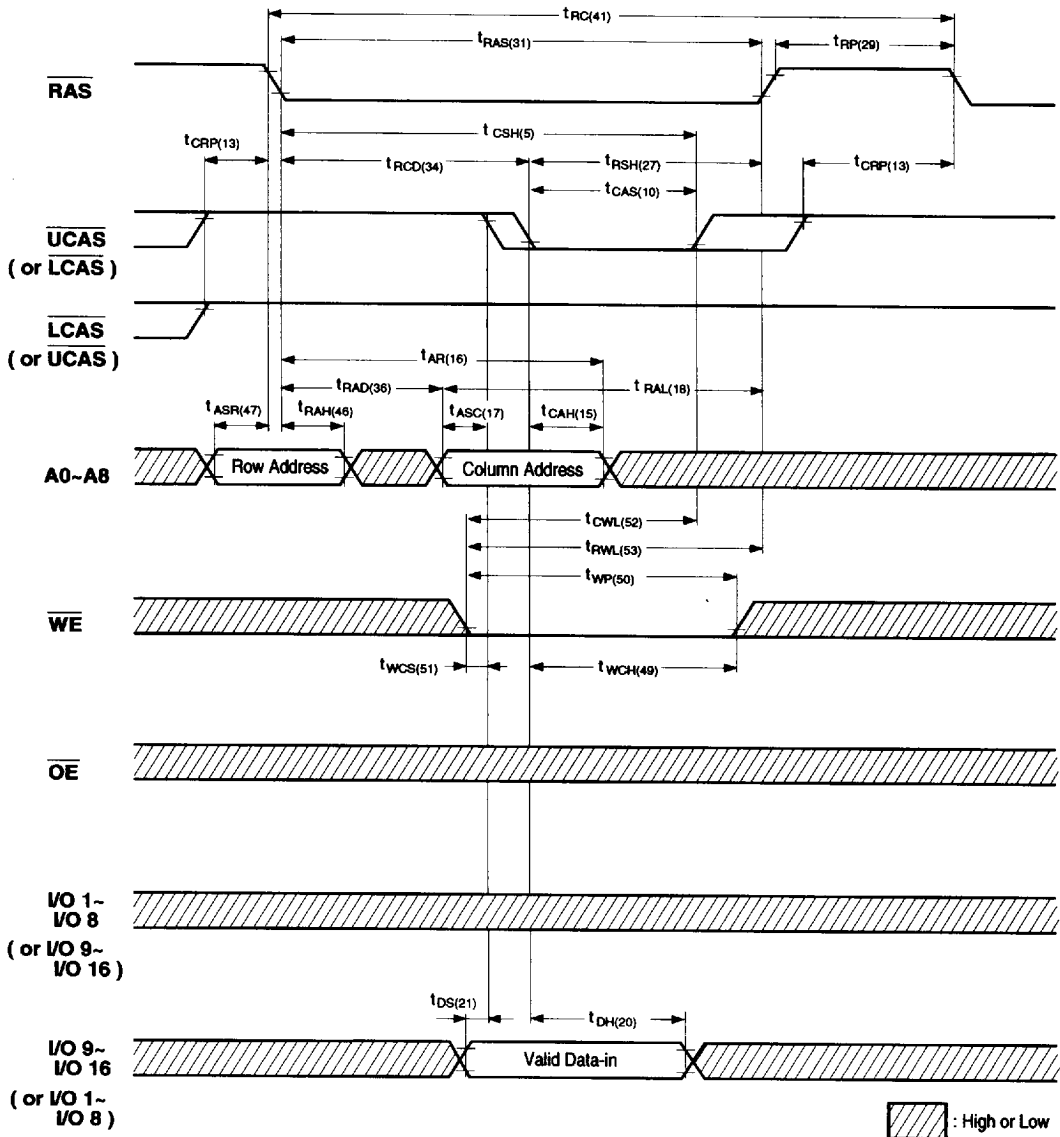


9005650 0001234 976

NPNX

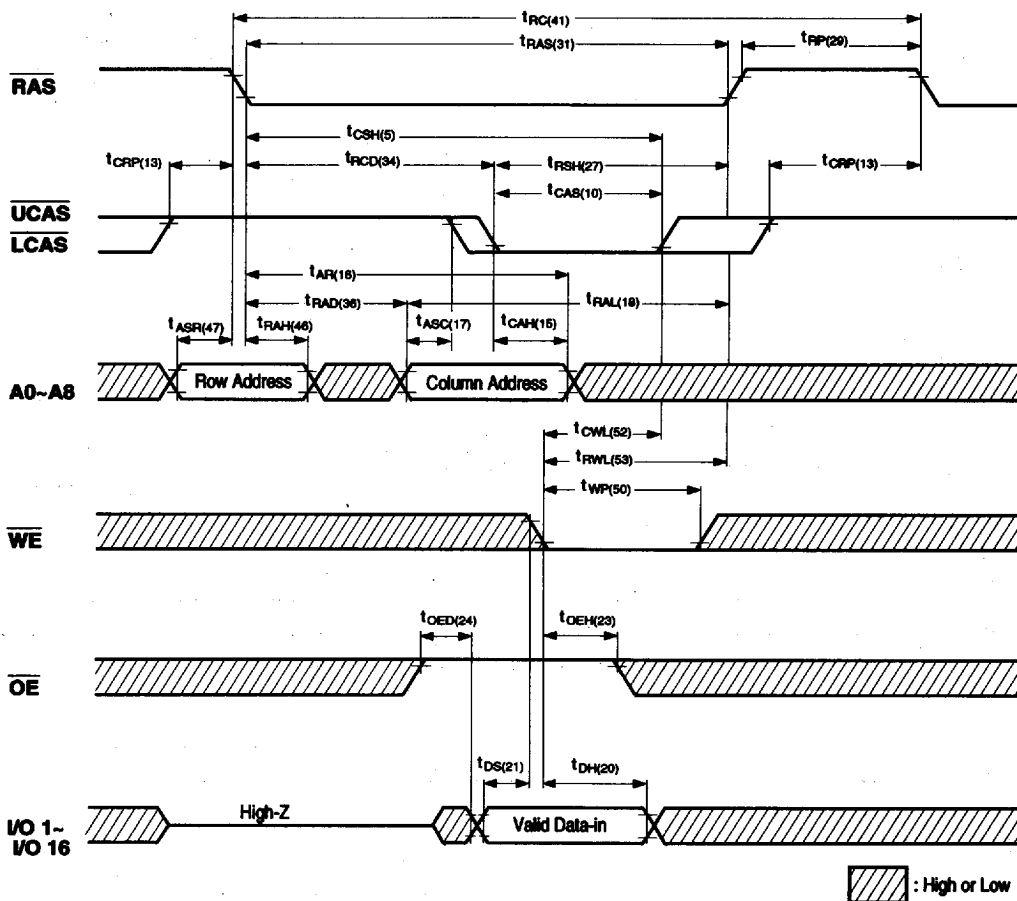
420

BYTE WRITE CYCLE (EARLY WRITE)



9005650 0001235 802

WORD WRITE CYCLE ($\overline{\text{OE}}$ -CONTROLLED WRITE)

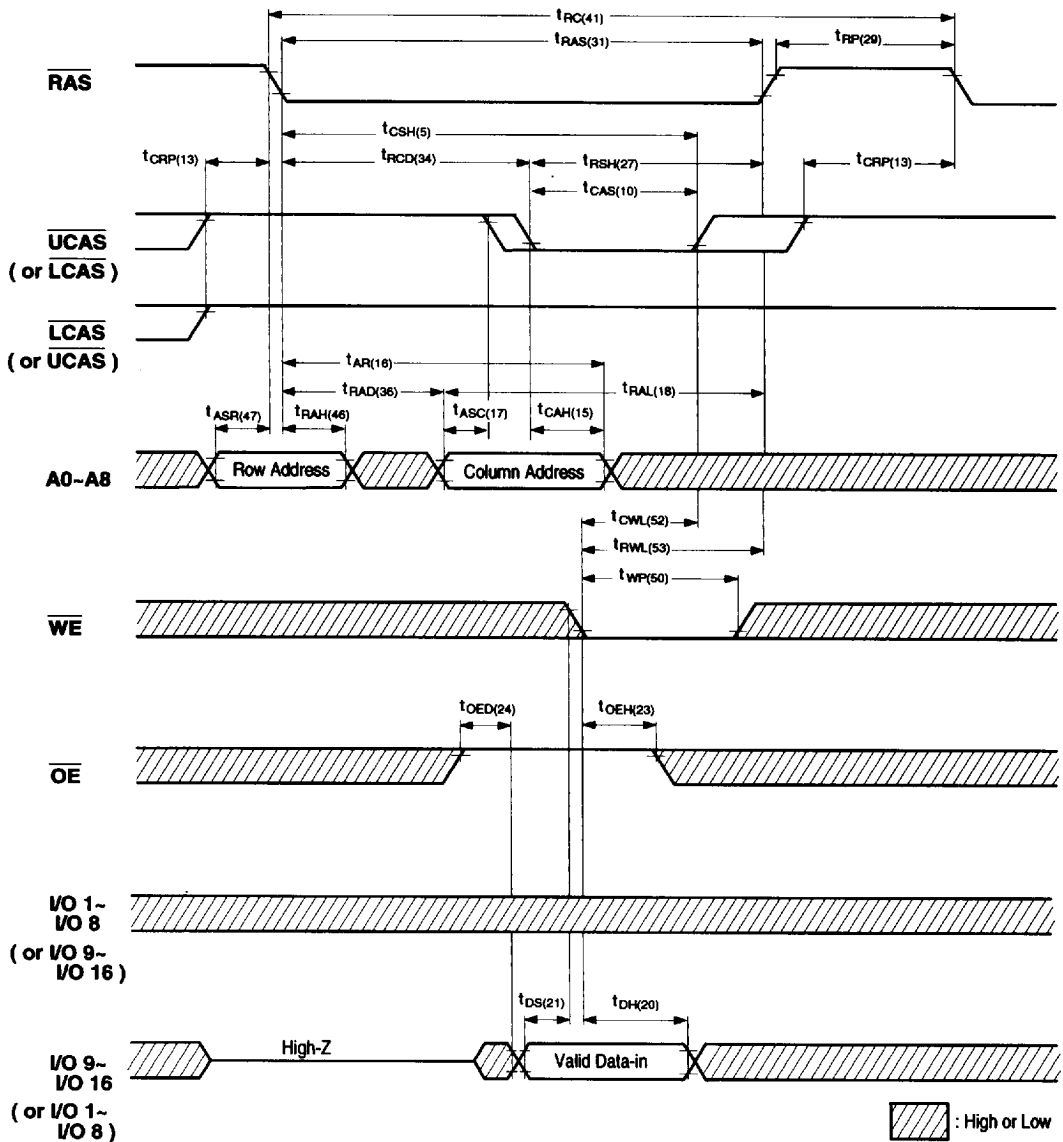


9005650 0001236 749

NPNX

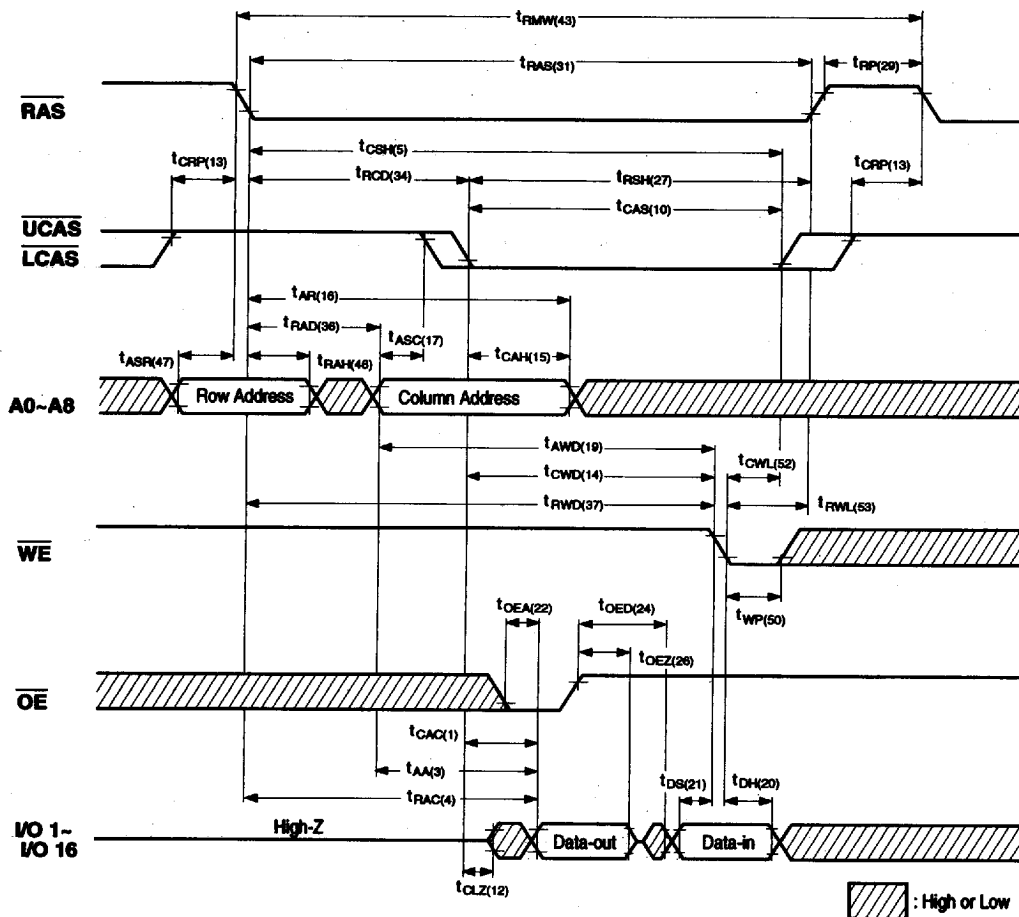
422

BYTE WRITE CYCLE ($\overline{OE}$ -CONTROLLED WRITE)



9005650 0001237 685

WORD READ-MODIFY-WRITE CYCLE

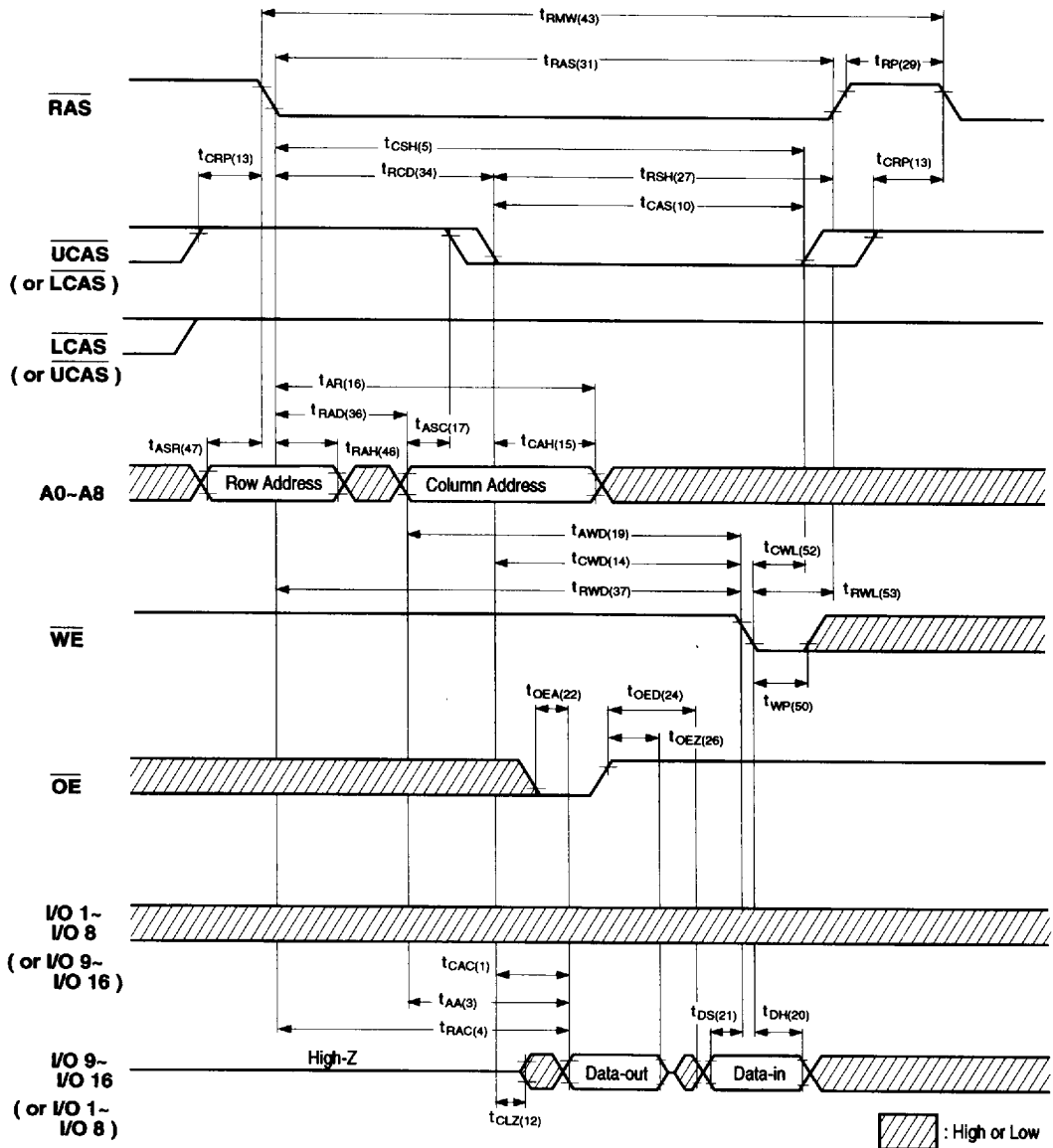


9005650 0001238 511

NPNX

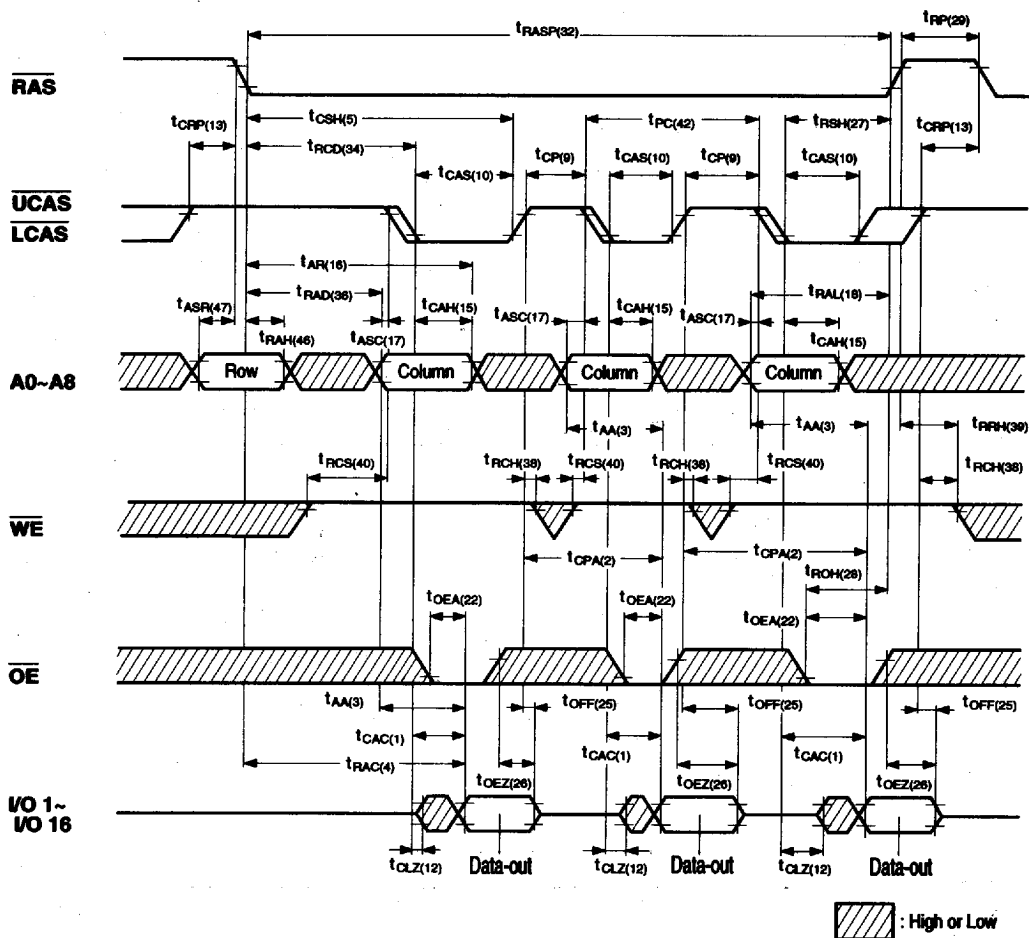
424

BYTE READ-MODIFY-WRITE CYCLE



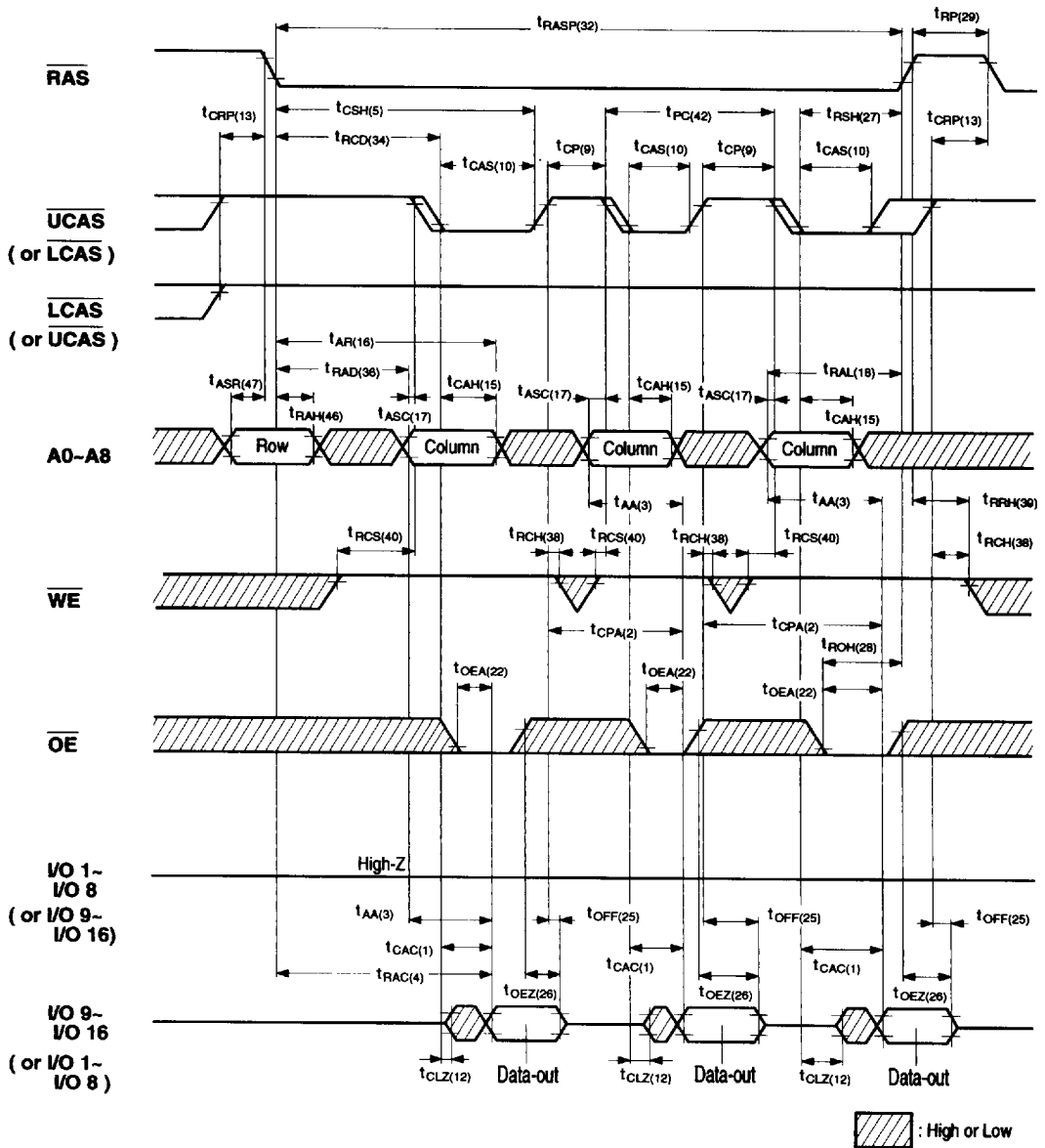
9005650 0001239 458

FAST PAGE MODE WORD READ CYCLE



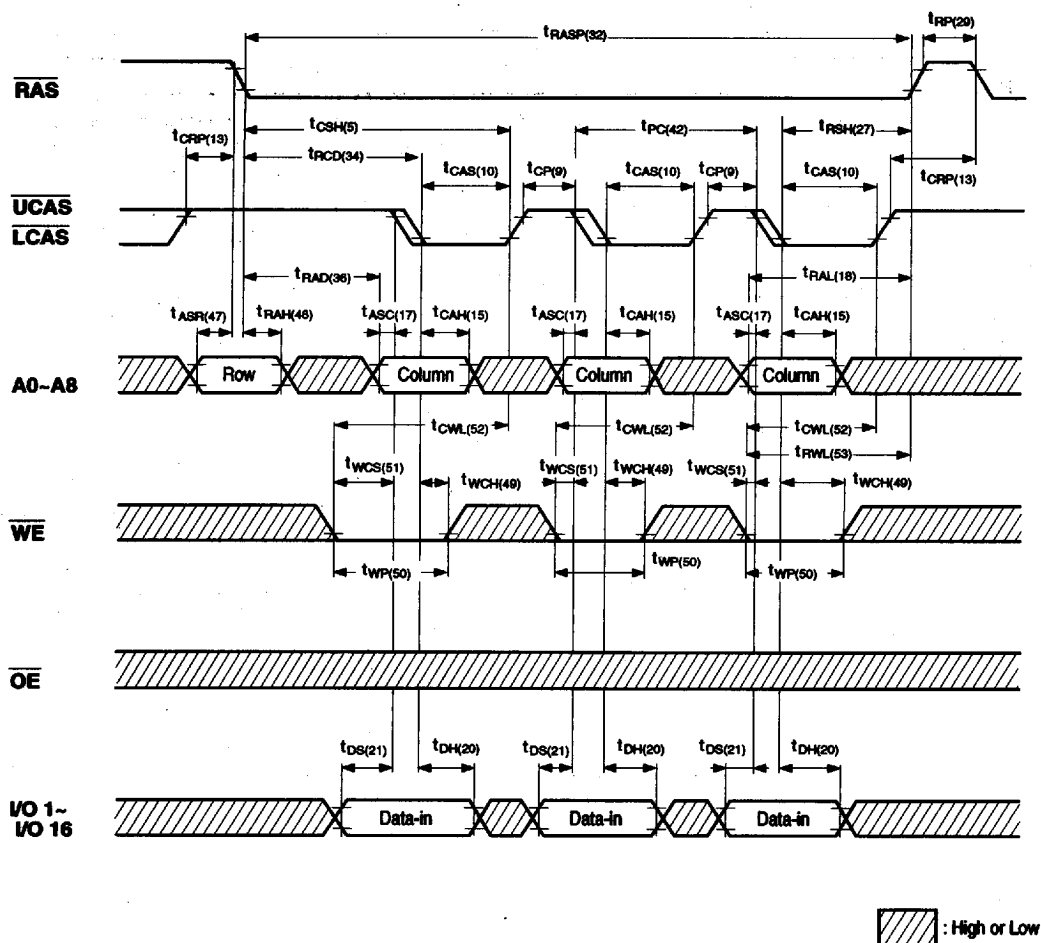
9005650 0001240 17T

FAST PAGE MODE BYTE READ CYCLE



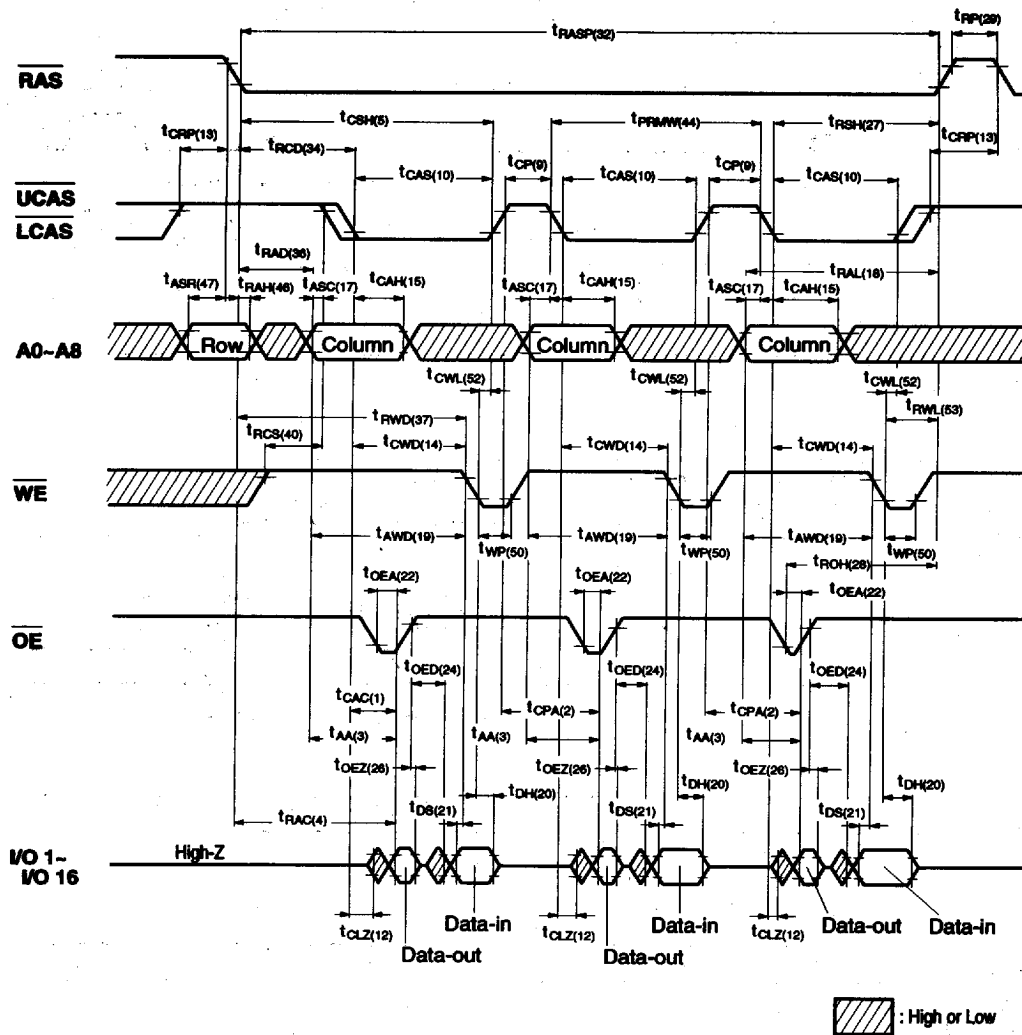
9005650 0001241 006

FAST PAGE MODE EARLY WORD WRITE CYCLE



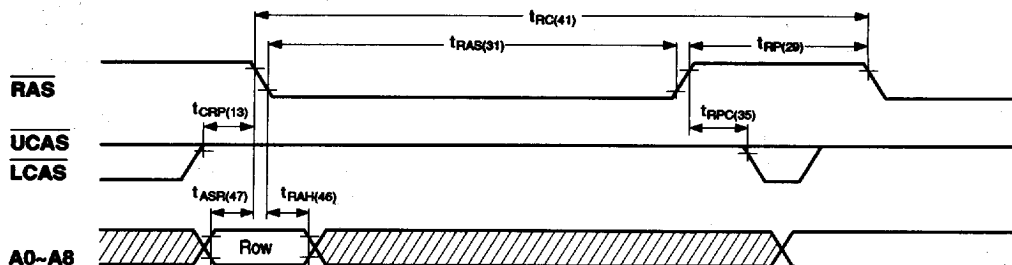
9005650 0001242 T42

FAST PAGE MODE WORD READ-MODIFY-WRITE CYCLE



9005650 0001244 815

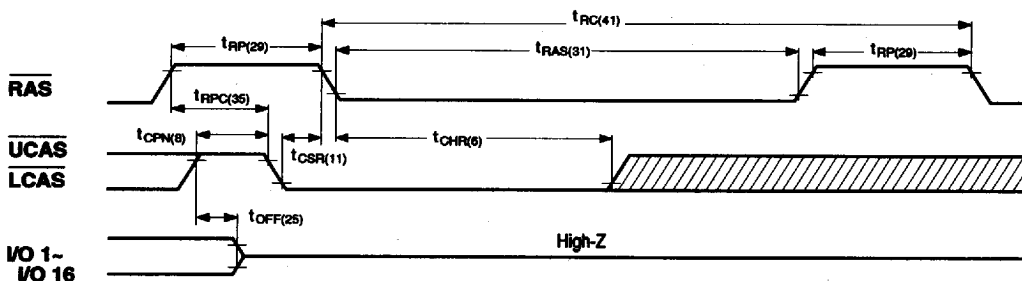
RAS ONLY REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

 : High or Low

CAS BEFORE RAS REFRESH CYCLE

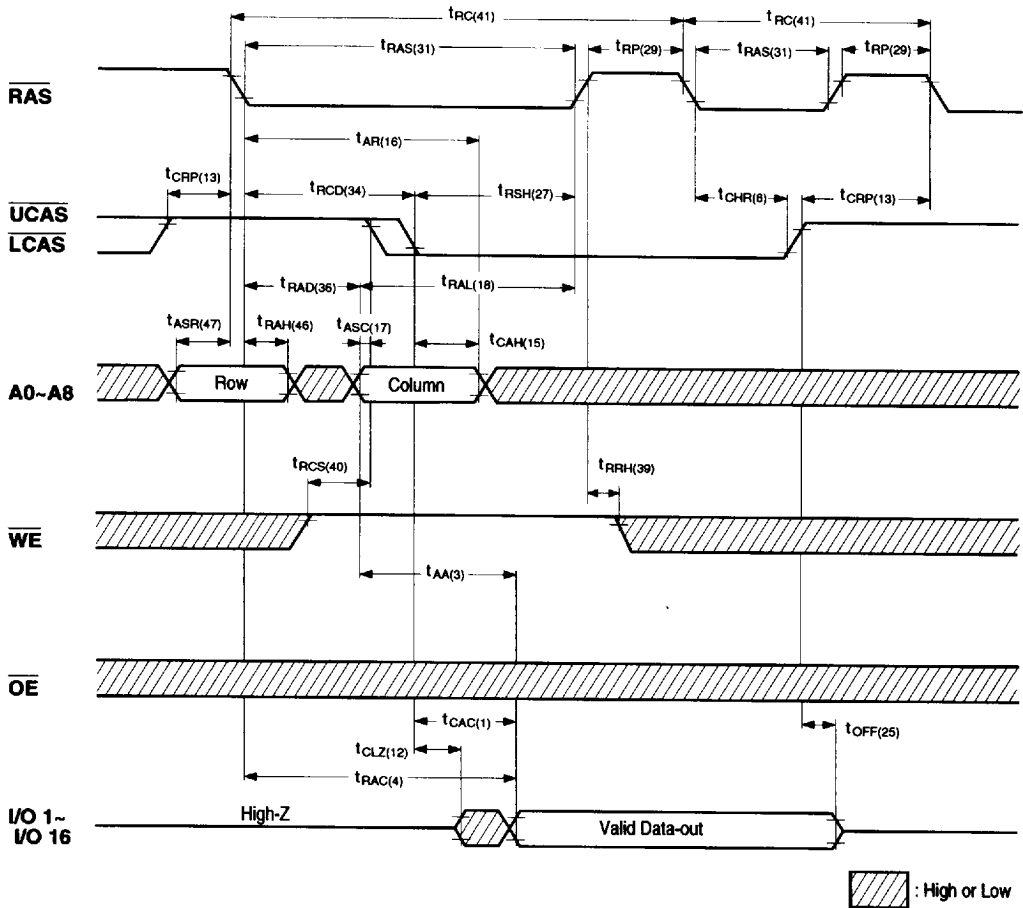


Note: $\overline{WE}$, $\overline{OE}$, A0~A8 = Don't care.

 : High or Low

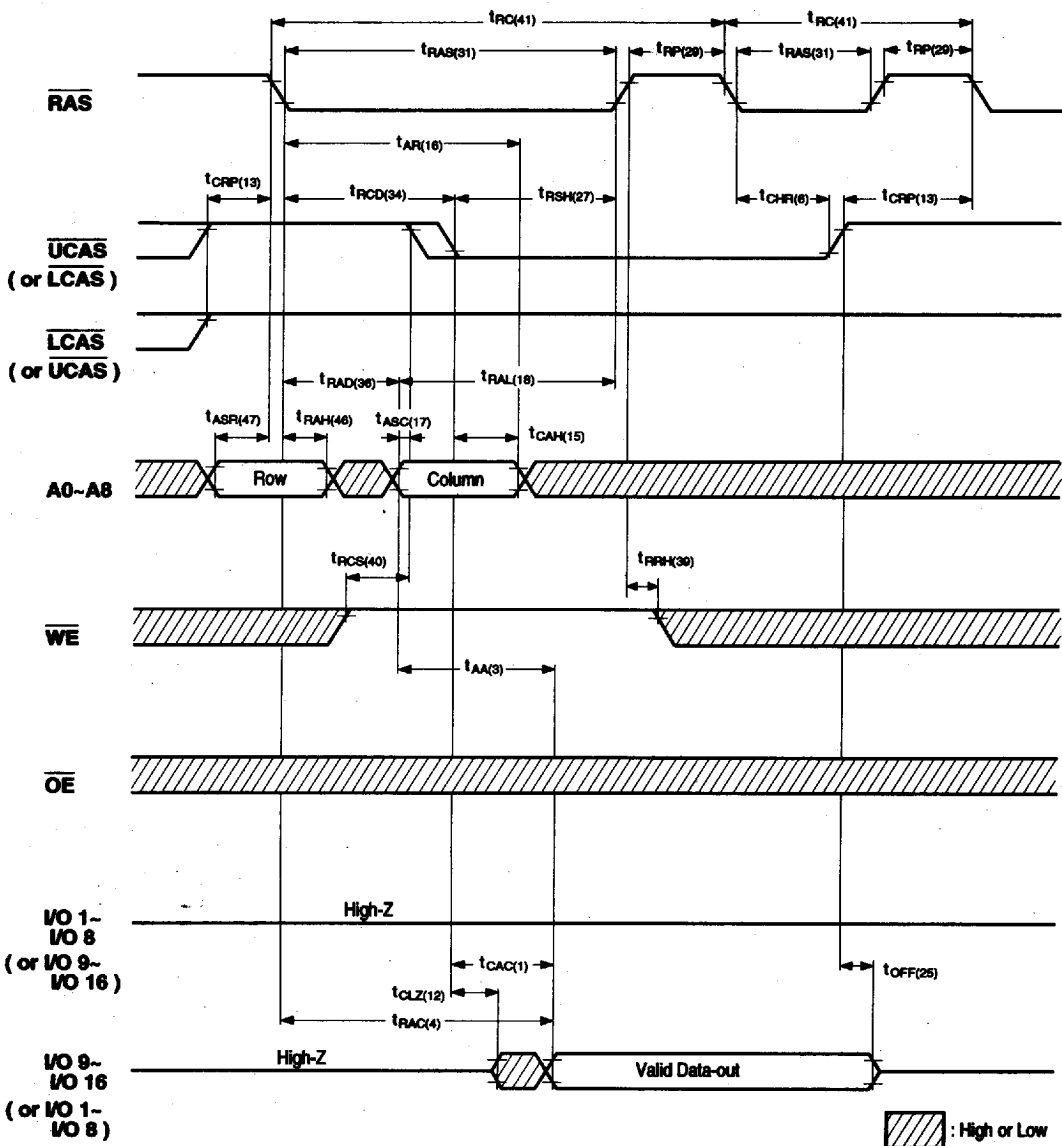
9005650 0001246 698

HIDDEN REFRESH CYCLE (WORD READ)



9005650 0001247 524

HIDDEN REFRESH CYCLE (BYTE READ)

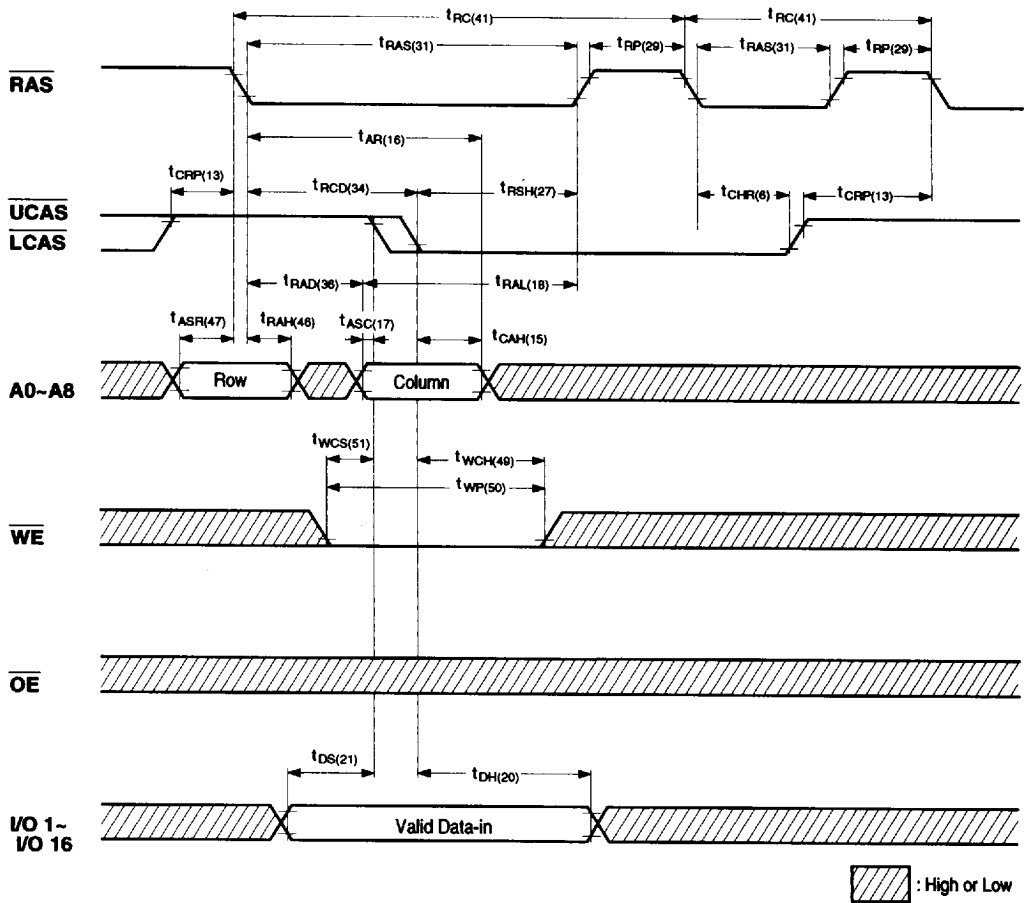


9005650 0001248 460

NPNX

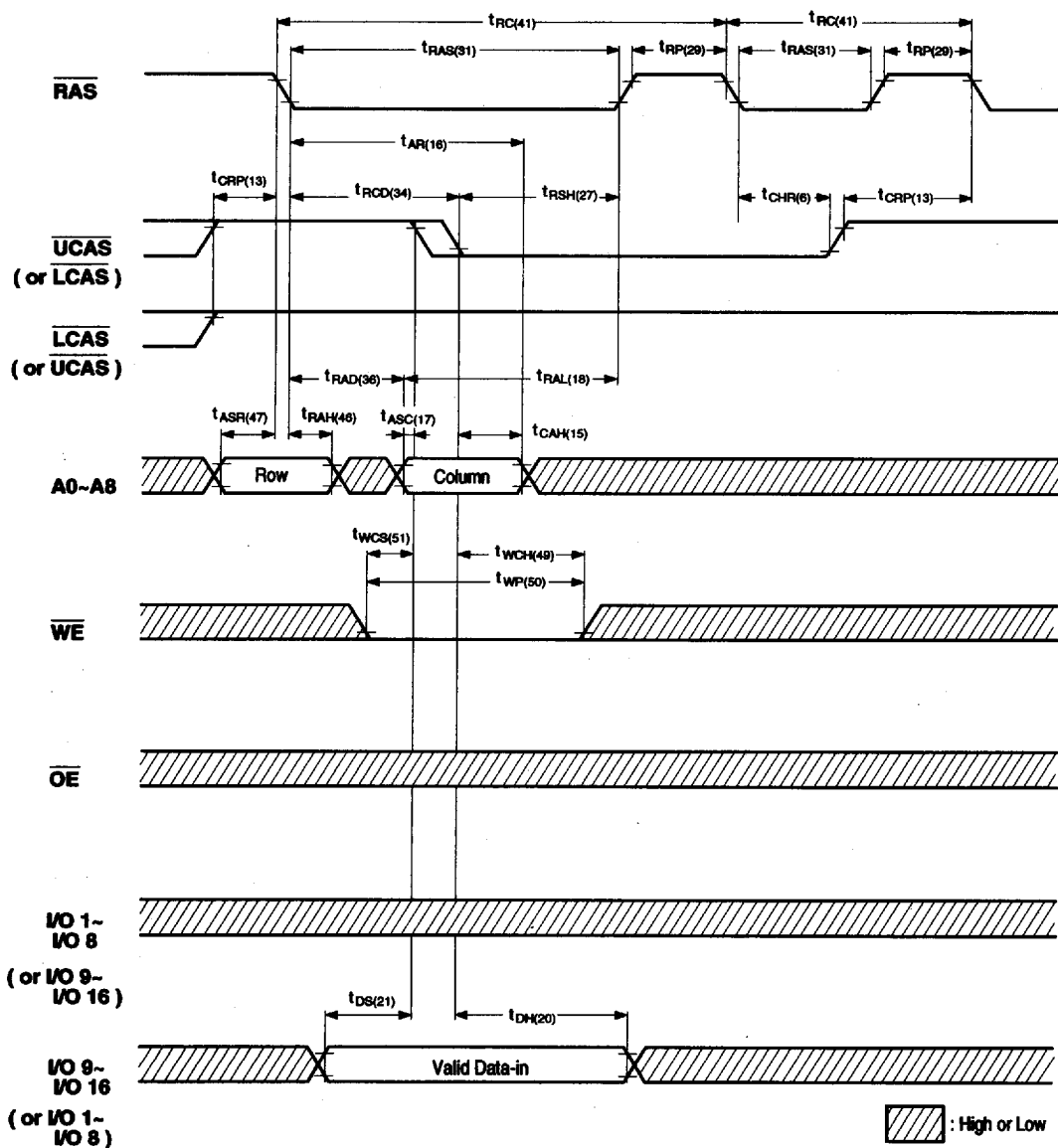
434

HIDDEN REFRESH CYCLE (EARLY WORD WRITE)



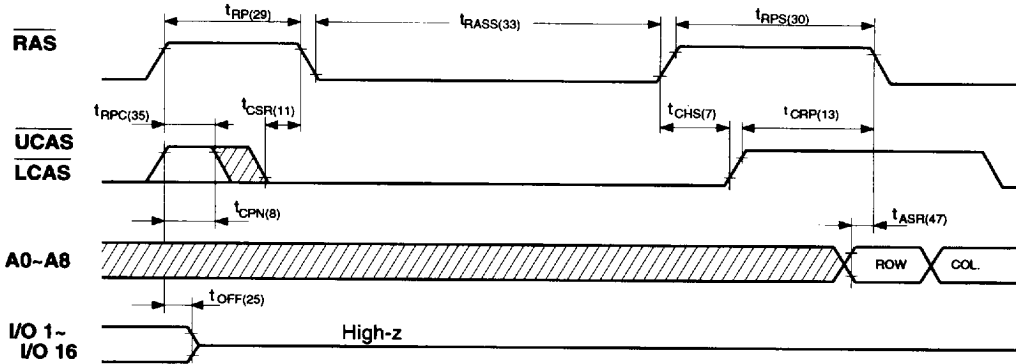
9005650 0001249 3T7

HIDDEN REFRESH CYCLE (EARLY BYTE WRITE)



9005650 0001250 019

SELF REFRESH MODE



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

 : High or Low

■ The NN514260L/AL version has a Self Refresh Mode.

a. Entering the Self Refresh Mode:

The NN514260L/AL Self Refresh Mode is entered by using $\overline{CAS}$ before $\overline{RAS}$ cycle and holding $\overline{RAS}$ and $\overline{CAS}$ signal "low" longer than 300 μ s.

b. Continuing the Self Refresh Mode:

The Self Refresh Mode is continued by holding $\overline{RAS}$ "low" after entering the Self Refresh Mode.

It does not depend on $\overline{CAS}$ being "high" or "low" after entering the Self Refresh Mode to continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:

The NN514260L/AL exits the Self Refresh Mode when the $\overline{RAS}$ signal is brought "high".

9005650 0001251 T55

ORDERING INFORMATION

NN514260XX(X) - XX

				<u>SPEED</u>	45 : 45ns
					50 : 50ns
					60 : 60ns
					70 : 70ns
				<u>PACKAGE</u>	J : Plastic SOJ
					TT : Plastic TSOP TYPEII
				<u>VERSION</u>	BLANK : Standard Version
					L : Long Refresh Version 128ms Refresh
				<u>MODE</u>	4260 : Fast Page
					2CAS ,256K x 16 ,512refresh cycle

NN514260AXX(X) - XX

					<u>SPEED</u>	35 : 35ns
						40 : 40ns
						45 : 45ns
						50 : 50ns
						60 : 60ns
					<u>PACKAGE</u>	J : Plastic SOJ
						TT : Plastic TSOP TYPEII
					<u>VERSION</u>	BLANK : Standard Version
						L : Long Refresh Version 128ms Refresh
					<u>DESIGN CODE</u>	A : NN514260A
					<u>MODE</u>	4260 : Fast Page
						2CAS ,256K x 16 ,512refresh cycle

9005650 0001252 991