DESCRIPTION

The NN51V17405B series is a high performance CMOS Dynamic Random Access Memory organized as 4,194,304 words by 4 bits. The NN51V17405B series is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN51V17405B series features EDO (Hyper page) mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

The outputs are tri-stated by $\overline{CAS}$ which, in essence, acts as an output enable independent of $\overline{RAS}$ with very fast $\overline{CAS}$ to output access time.

Refresh is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 2,048 address combinations of A0 to A10 during a 32 ms period.

Multiplexed address inputs permit the NN51V17405B series to be packaged in a standard 26-pin plastic SOJ. 26 pin TSOP TYPE II. The package sizes provide high system bit densities. System level features include single power supply of 3.3V ±10% tolerance and direct interface with high performance TTL logic families.

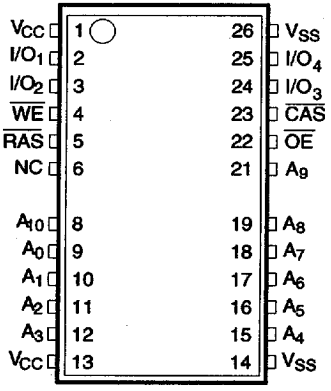
FEATURES

- 4,194,304 × 4 bit Organization
- Single 3.3V ±10% Power Supply
- Performance Ranges

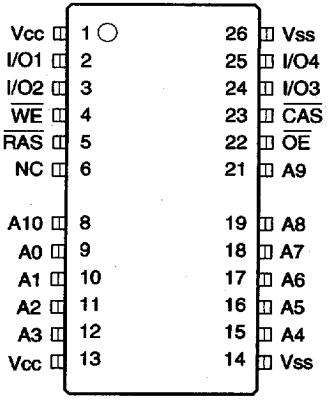
Parameter	-50	-60	-70
Max. $\overline{RAS}$ Access Time (t_{RAC})	50ns	60ns	70ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	15ns	17ns	20ns
Max. Column Address Access Time (t_{AA})	25ns	30ns	40ns
Min. Read/Write Cycle Time (t_{RC})	90ns	110ns	130ns

- EDO (Hyper Page) Mode Operation
- Low Power Operation
  Low Standby Current (CMOS level input)
  -Standard 1mA
  -L version 150μA
- 2048 Refresh Cycles
  -Standard 32ms
  -L version 128ms
- Self Refresh Mode
  (L version)
- All inputs/Outputs and Clocks
  fully TTL and CMOS compatible
- Refresh Modes
  $\overline{RAS}$ only
  $\overline{CAS}$ before $\overline{RAS}$
  Hidden Refresh
- High Reliability Package
  Plastic 26pin SOJ (P26/24SJ-2A-L)
  Plastic 26pin TSOP TYPE II (P26/24TP-2A-L)

PIN CONFIGURATION



26/24-pin SOJ (300mil)
P26/24SJ-2A-L

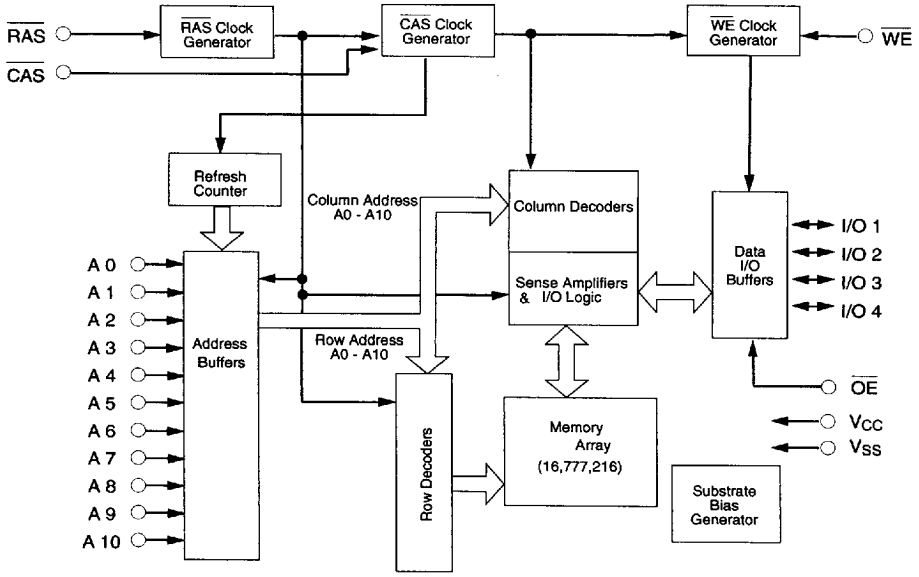


26/24-pin TSOP TYPE II (300mil)
P26/24TP-2A-L

PIN NAMES

A0~A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{OE}$	Output Enable
I/O1~I/O4	Data-in / Data-out
$\overline{WE}$	Write Enable
V_{CC}	+3.3V Supply
V_{SS}	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	Vin,Vout	−0.5 to 4.6	V
Voltage on Vcc Relative to V_{SS}	V_{CC}	−0.5 to 4.6	V
Storage Temperature (Plastic)	Tstg	−55 to +125	°C
Power Dissipation	Pd	1.0	W
Ambient Operating Temperature	Ta	0 to + 70	°C
Short Circuit Output Current	Iout	20	mA

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage, All Inputs	2.0	—	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage, All Inputs	−0.3	—	0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS} unless otherwise specified.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 3.3V ±10%)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I_{CC1}	Operating Current	-50 -60 -70		110 100 90	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$, $\overline{CAS}$, Address cycling	1, 2
I_{CC2}	Standby Current			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V)	
				2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}	
	Standby Current (L version)			150	µA	$\overline{RAS}$ = $\overline{CAS}$ ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	
I_{CC3}	Refresh Current ($\overline{RAS}$ only refresh)	-50 -60 -70		110 100 90	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}	1
I_{CC4}	EDO (Hyper) Page Mode Current	-50 -60 -70		100 90 80	mA mA mA	t_{HPC} = t_{HPC} (min.) $\overline{RAS}$ = V_{IL} $\overline{CAS}$, Address cycling	1,2
I_{CC5}	Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	-50 -60 -70		110 100 90	mA mA mA	t_{RC} = t_{RC} (min.) $\overline{RAS}$, $\overline{CAS}$ cycling	1
I_{CC6}	Refresh Current $\overline{CAS}$ before $\overline{RAS}$ refresh)			500	µA	2,048 cycles / 128ms t_{RAS} ≤ 200ns, $\overline{WE}$ ≥ (V_{CC} - 0.2V) All other inputs are stable at (V_{CC} - 0.2V) or (V_{SS} + 0.2V)	
I_{CC7}	Self Refresh Mode Current			300	µA	$\overline{RAS}$ =$\overline{CAS}$ ≤ (V_{SS} + 0.2V) All other input high levels are (V_{CC} - 0.2V) or input low levels are (V_{SS} + 0.2V)	
$\lvert I_{L1} \rvert$	Input Leakage Current (Any input pin)		-10	10	µA	0V ≤ V_{IH} ≤ 3.6V, Others = 0V	
$\lvert I_{LO} \rvert$	Output Leakage Current (For high impedance state)		-10	10	µA	$\overline{RAS}$ ≥ V_{IH}(min), $\overline{CAS}$ ≥ V_{IH}(min) 0V ≤ V_{OUT} ≤ 3.6V	
V_{OH}	Output High Voltage		2.4		V	I_{OH} = –2.0 mA	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.0 mA	

Notes: 1. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 3.3V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN1}	Address(A0 ~ A10)	—	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	—	5	pF
C_{OUT}	I/O1,I/O2,I/O3,I/O4	—	7	pF

AC ELECTRICAL CHARACTERISTICS

Test conditions : V_{IH} / V_{IL}= 2.4V / 0.8V V_{OH} / V_{OL} = 2.0V / 0.8V output loading C_L = 100pF + 1TTL

Operating conditions : (0 °C≤Ta≤70°C, V_{CC} = 3.3 V ± 10%, V_{SS} = 0 V) (NOTES 3, 4, 5)

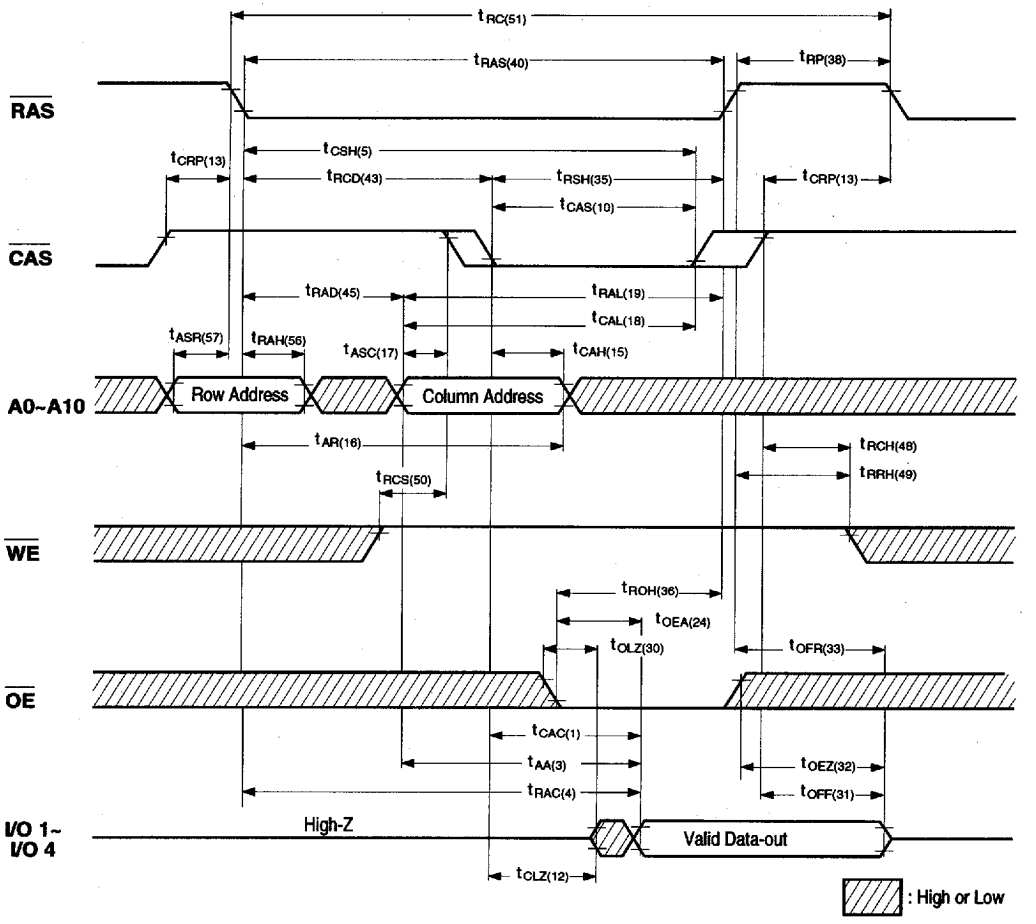
NO.	NOTES		PARAMETER	-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	17	—	20	ns	6,13
2	t_{CH2QV}	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	30	—	35	—	40	ns	13,14
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	25	—	30	—	40	ns	7,13
4	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	—	50	—	60	—	70	ns	6,7
5	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	35	—	40	—	45	—	ns	
6	t_{RL1CX}	t_{CHS}	$\overline{CAS}$ Hold Time (Self Refresh Mode)	-50	—	-50	—	-50	—	ns	
7	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	10	—	ns	
8	t_{CH2CL2}	t_{CPN}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	7	—	10	—	10	—	ns	
9	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	5	—	5	—	5	—	ns	14
10	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	8	100K	10	100K	15	100K	ns	
11	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	5	—	5	—	5	—	ns	
12	t_{CL1QX}	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	32	—	37	—	42	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	7	—	10	—	12	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	35	—	40	—	40	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	ns	14
18	t_{AVCH1}	t_{CAL}	Column Address to CAS Lead Time	13	—	18	—	23	—	ns	
19	t_{AVRH1}	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	—	30	—	35	—	ns	
20	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	39	—	47	—	54	—	ns	11
21	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	7	—	10	—	10	—	ns	12
22	t_{CL2QX}	t_{DHC}	Data Output Hold Time	0	—	0	—	0	—	ns	
23	t_{DVCL2} t_{DVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	ns	12
24	t_{OL1QV}	t_{OEA}	$\overline{OE}$ Access Time	—	15	—	17	—	20	ns	
25	t_{WL1OL2}	t_{OEH}	$\overline{OE}$ Command Hold Time	13	—	15	—	20	—	ns	
26	t_{GH2GL2}	t_{OPZ}	$\overline{OE}$ Pulse Width for Output Disable When $\overline{CAS}$ High	7	—	7	—	7	—	ns	
27	t_{GL1CH1}	t_{OCS}	$\overline{OE}$ Setup Time to $\overline{CAS}$ High	7	—	7	—	7	—	ns	
28	t_{GL1RH1}	t_{ORS}	$\overline{OE}$ Setup Time to $\overline{RAS}$ High	7	—	7	—	7	—	ns	
29	t_{CH2QV}	t_{OED}	$\overline{OE}$ to Data Delay Time	15	—	15	—	20	—	ns	
30	t_{GL2QX}	t_{OLZ}	$\overline{OE}$ to Output in low-Z	0	—	0	—	0	—	ns	
31	t_{CH2QZ}	t_{OFF}	Output Buffer Turn-off Delay Time	0	13	0	15	0	20	ns	10,17
32	t_{OH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{OE}$	0	13	0	15	0	20	ns	
33	t_{RHQZ}	t_{OFR}	Output Buffer Turn-off Delay Time Referenced to $\overline{RAS}$	0	13	0	15	0	20	ns	16
34	t_{WL2QZ}	t_{WEZ}	Output Buffer Turn-off Delay Time Referenced to $\overline{WE}$	0	13	0	15	0	20	ns	

NO.	SYMBOL		PARAMETER	-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
35	t_{CL1RH1}	t_{RSH}	$\overline{RAS}$ Hold Time	13	—	15	—	18	—	ns	
36	t_{OL1RH1}	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10	—	10	—	10	—	ns	
37	t_{CH2RH1}	t_{RHCP}	$\overline{RAS}$ Hold Time Referenced $\overline{CAS}$ Precharge	30	—	35	—	40	—	ns	
38	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	25	—	30	—	40	—	ns	
39	t_{RH2RL2}	t_{RPS}	$\overline{RAS}$ Precharge Time (Self Refresh Mode)	90	—	110	—	130	—		
40	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	50	100K	60	100K	70	100K	ns	
41	t_{RL1RH1}	t_{RASS}	$\overline{RAS}$ Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	µs	
42	t_{RL1RH1}	t_{RASP}	$\overline{RAS}$ Pulse Width (EDO (Hyper Page) Mode)	50	100K	60	100K	70	100K	ns	
43	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	13	35	13	45	13	50	ns	6
44	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	—	5	—	5	—	ns	
45	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	11	25	11	30	11	35	ns	7
46	t_{RL2QX}	t_{RLZ}	$\overline{RAS}$ To Output in Low-Z	0	—	0	—	0	—	ns	
47	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	64	—	77	—	89	—	ns	11
48	t_{CH2WL2}	t_{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	9
49	t_{RH2WL2}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	—	0	—	0	—	ns	9
50	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	ns	
51	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	90	—	110	—	130	—	ns	
52	t_{CL2CL2}	t_{HPC}	Read or Write Cycle Time (EDO (Hyper Page) Mode)	20	—	25	—	30	—	ns	13,14
53	t_{RL2RL2}	t_{RMW}	Read-Modify-Write Cycle Time	120	—	140	—	160	—	ns	
54	t_{CL2CL2}	t_{PRMW}	Read-Modify-Write Cycle Time (EDO (Hyper Page) Mode)	55	—	65	—	75	—	ns	13,14
55	t_{REF}	t_{REF}	Refresh Period	—	32	—	32	—	32	ms	15
56	t_{RL1AX}	t_{RAH}	Row Address Hold Time	8	—	8	—	8	—	ns	
57	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	ns	
58	t_T	t_T	Transition Time (Rise and Fall)	1	50	1	50	1	50	ns	4,5
59	t_{WL1WH1}	t_{WPZ}	$\overline{WE}$ Pulse Width for Disable When $\overline{CAS}$ High	7	—	7	—	7	—	ns	
60	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10	—	10	—	15	—	ns	
61	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	10	—	10	—	15	—	ns	
62	t_{WL1CL2}	t_{WCS}	Write Command Setup Tlme	0	—	0	—	0	—	ns	11
63	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	7	—	10	—	13	—	ns	
64	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	7	—	10	—	13	—	ns	
65	t_{WL1RL2}	t_{WSR}	Write Command Setup Time (Test Mode)	10	—	10	—	10	—	ns	
66	t_{RL1WH1}	t_{WHR}	Write Command Hold Time (Test Mode)	10	—	10	—	10	—	ns	
67	t_{WH2RL2}	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$)	10	—	10	—	10	—	ns	
68	t_{RL1WH2}	t_{WRH}	$\overline{WE}$ to RAS Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	10	—	10	—	10	—	ns	

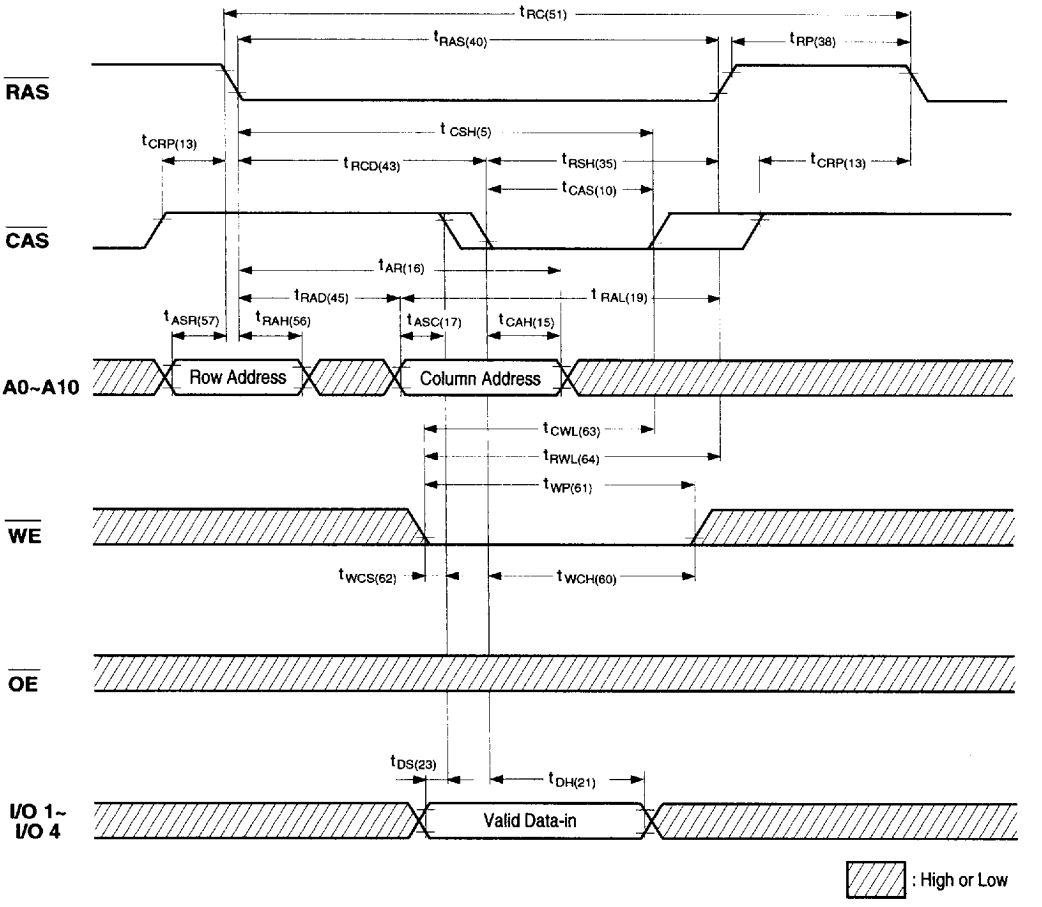
Notes:

3. Eight Initialization Cycles are required following a 200μs pause after Power Up. These Initialization Cycles may consist of any combination of the following : $\overline{RAS}$ only refresh Cycles, Read Cycles, Write Cycles. $\overline{CAS}$ before $\overline{RAS}$ refresh Cycles.
4. AC measurements assume t_T=2ns.
5. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
7. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
8. Assumes three state test load (500 ohm to 1.4V Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{OFF}(max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels. t_{OFF} only applies when $\overline{RAS}$ is high.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.) , the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
13. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{CPA}.
14. $t_{ASC} \geq t_{CP}$ to achieve t_{PC}(min.) and t_{CPA}(max.) values.
15. t_{REF}=128msec for Long Refresh version (L version).
16. t_{OFR} applies only when $\overline{CAS}$ is high.
17. Output buffers turn into Hi-Z by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$, Therefore t_{OFF} and t_{OFR} are determined by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$.

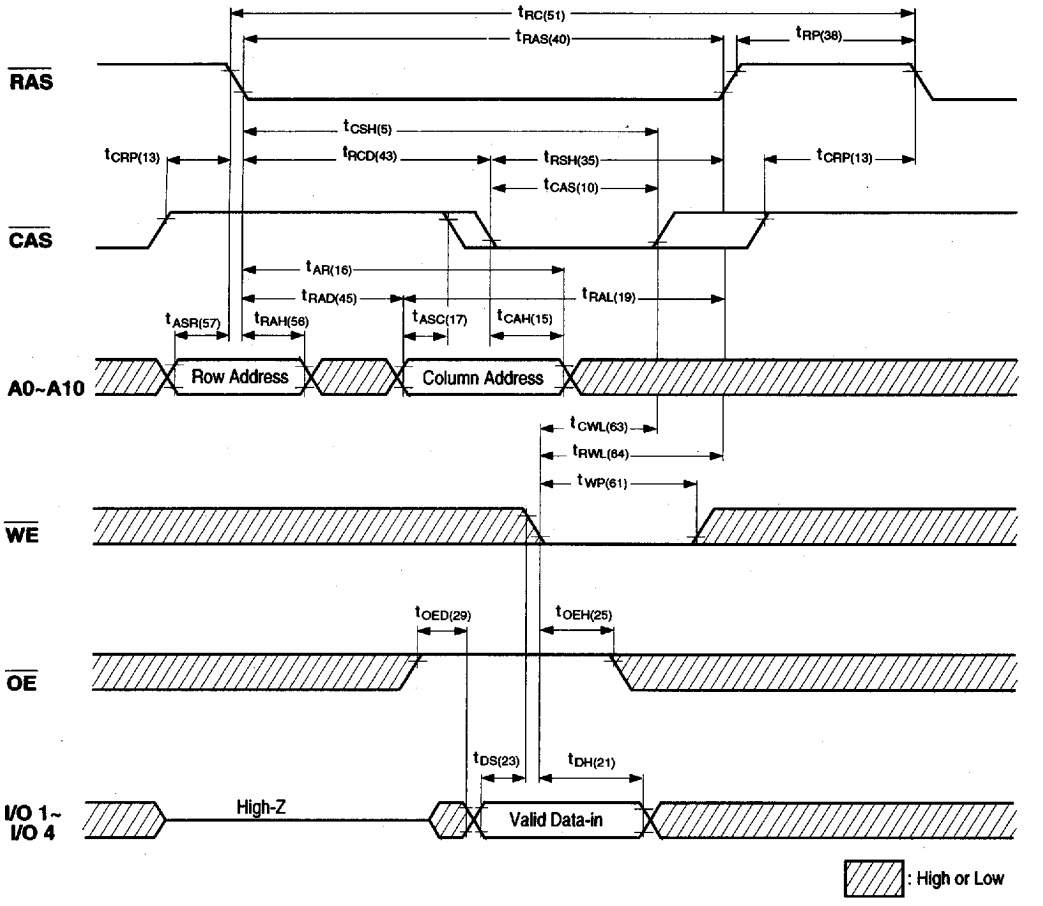
READ CYCLE



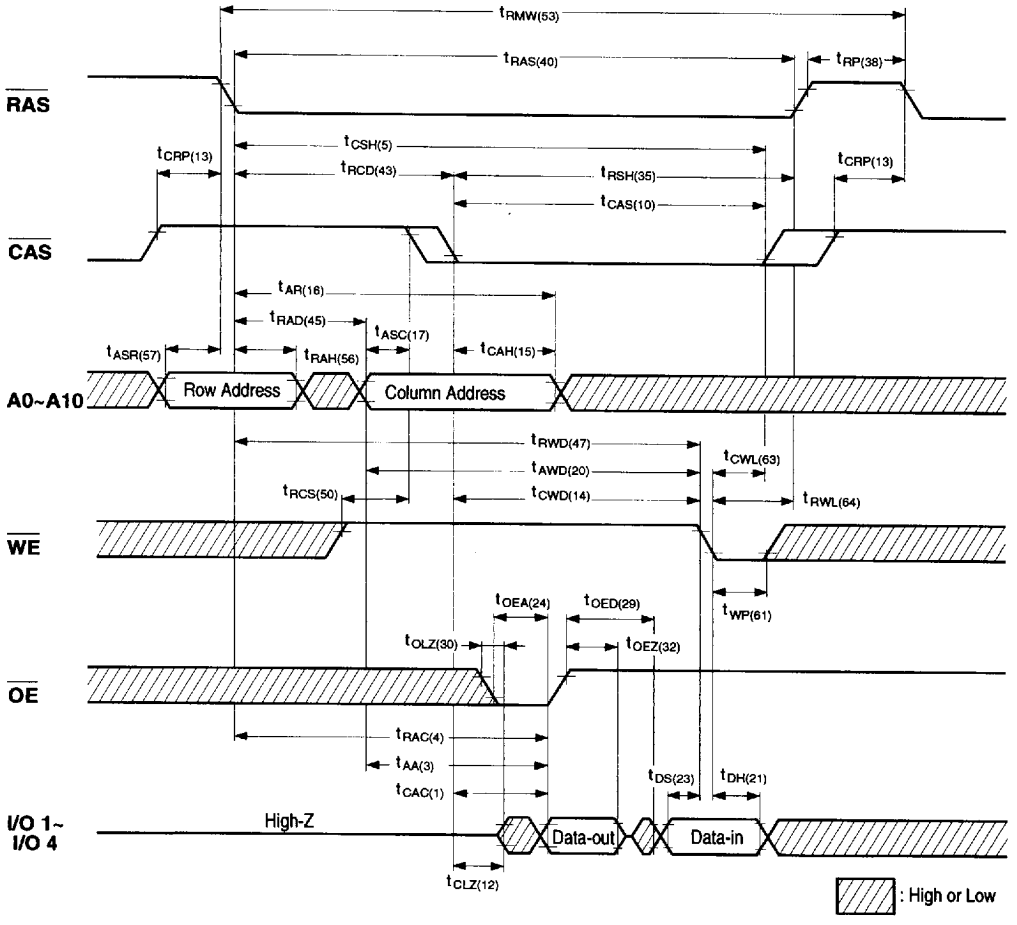
WRITE CYCLE (EARLY WRITE)



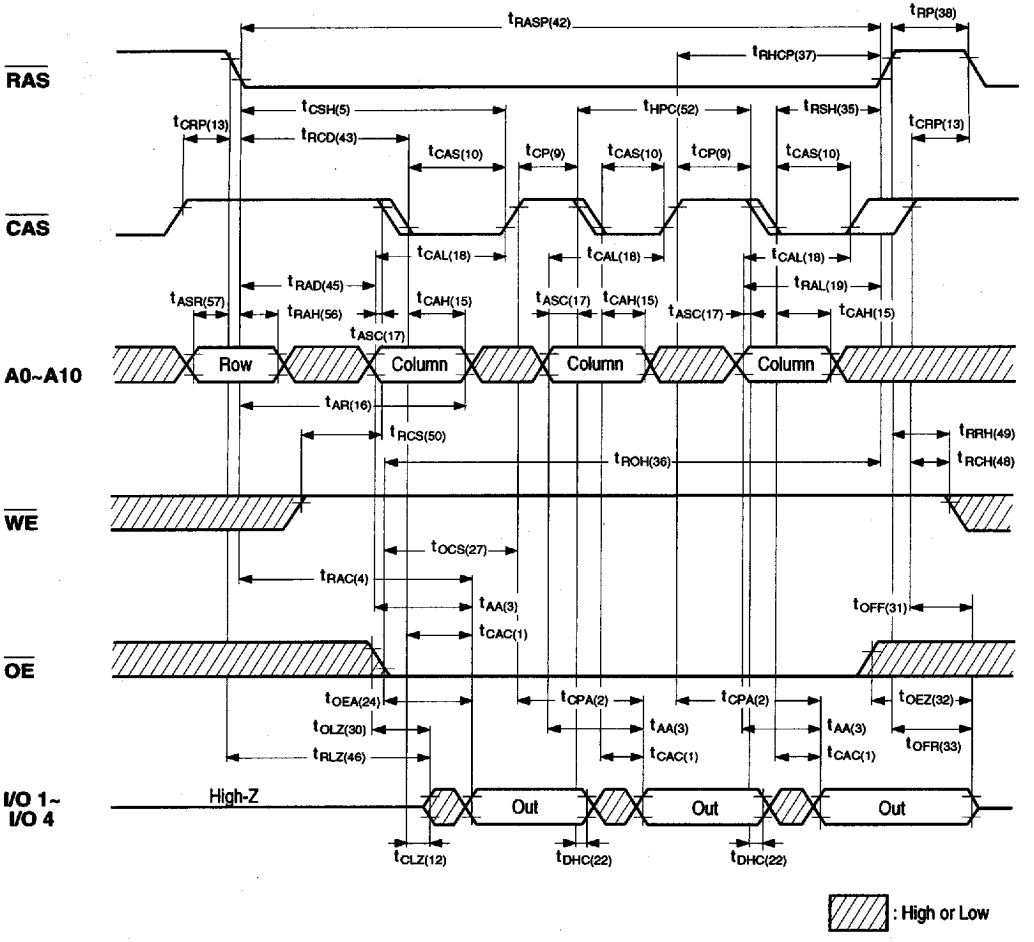
WRITE CYCLE ($\overline{OE}$-CONTROLLED WRITE)



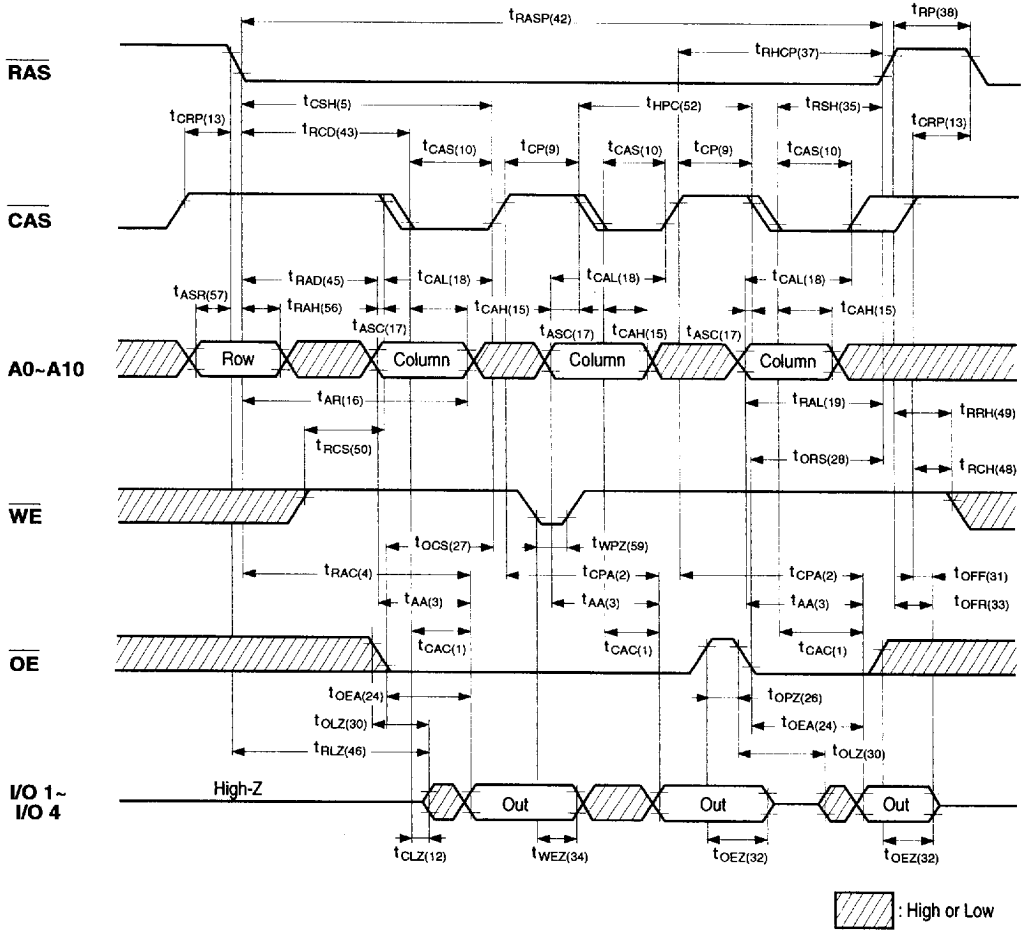
READ-MODIFY-WRITE CYCLE



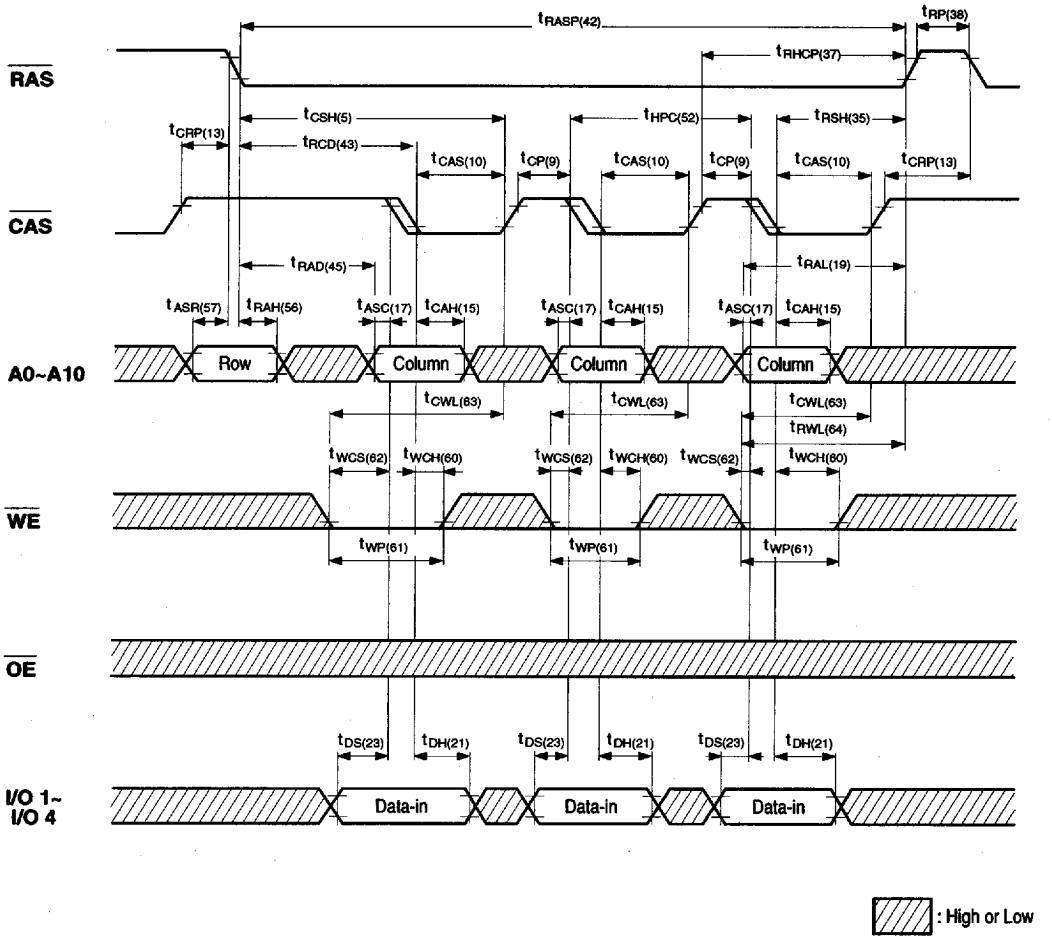
EDO (HYPER PAGE) MODE READ CYCLE



EDO (HYPER PAGE) MODE READ CYCLE ($\overline{OE}$ AND $\overline{WE}$ CONTROLLED OUTPUT)

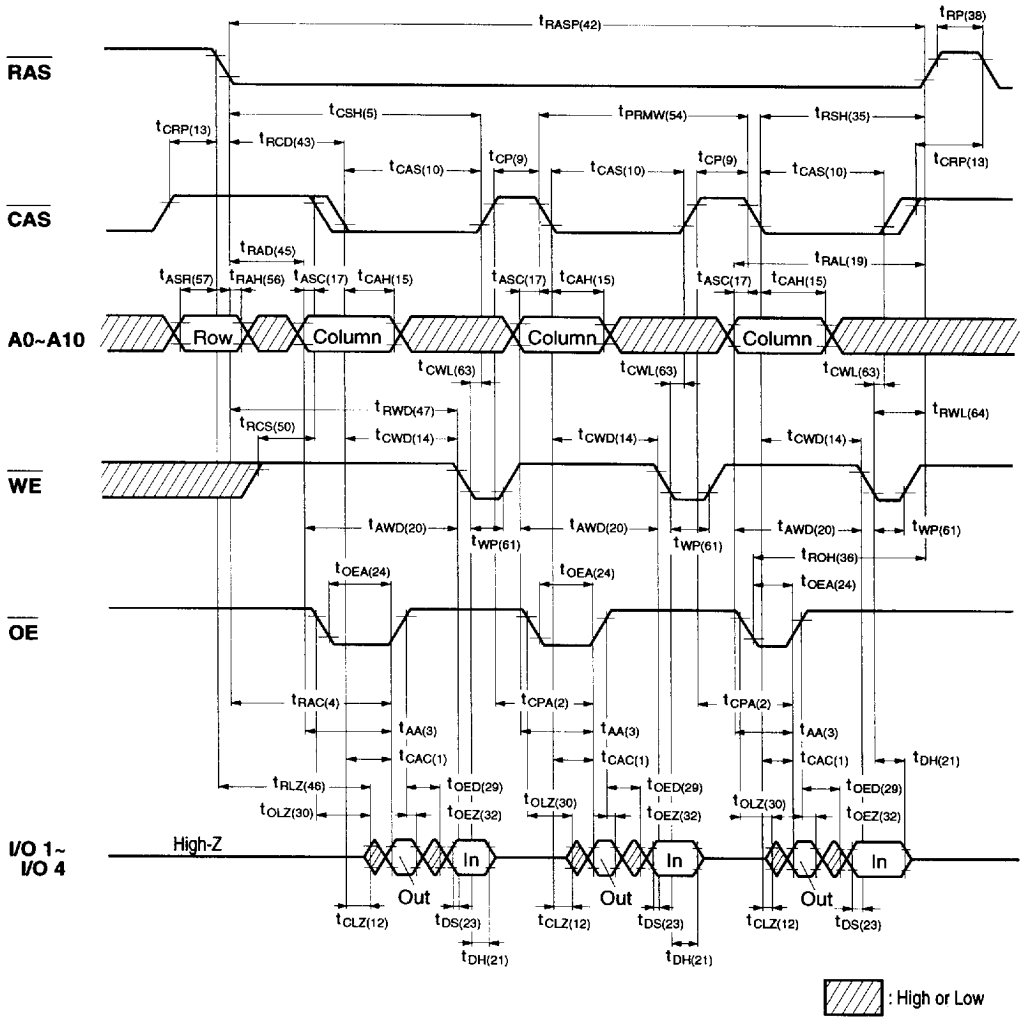


EDO (HYPER PAGE) MODE EARLY WRITE CYCLE

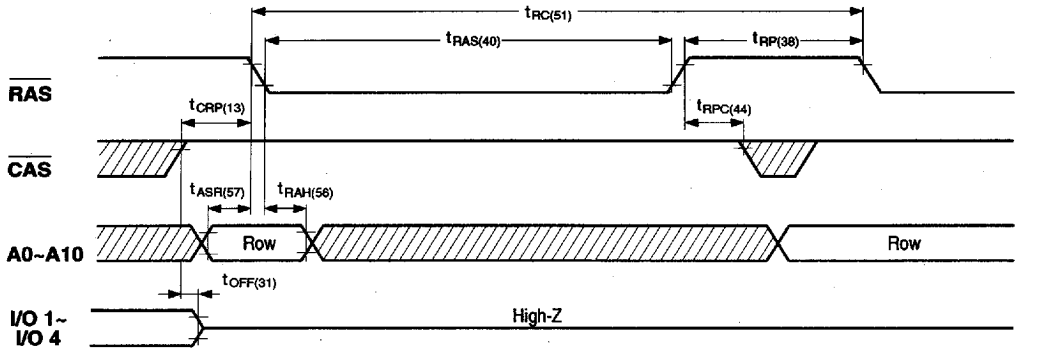


: High or Low

EDO (HYPER PAGE) MODE READ-MODIFY-WRITE CYCLE



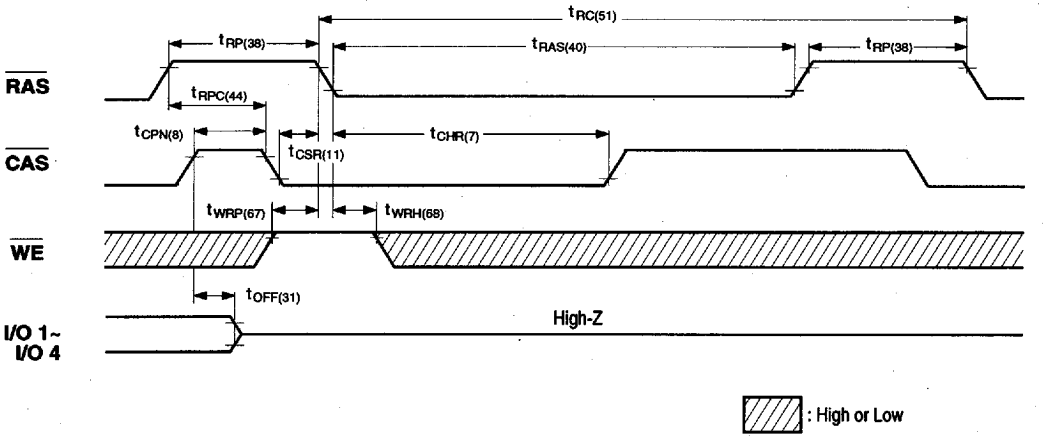
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

: High or Low

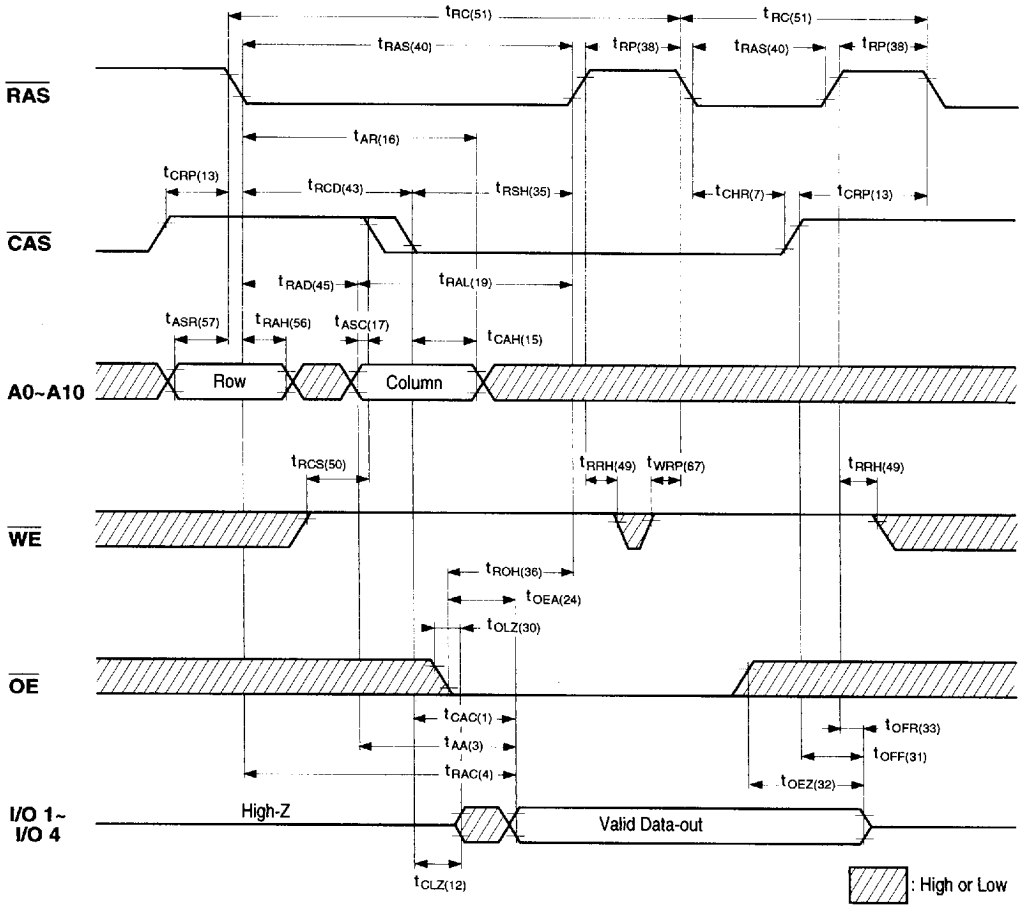
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



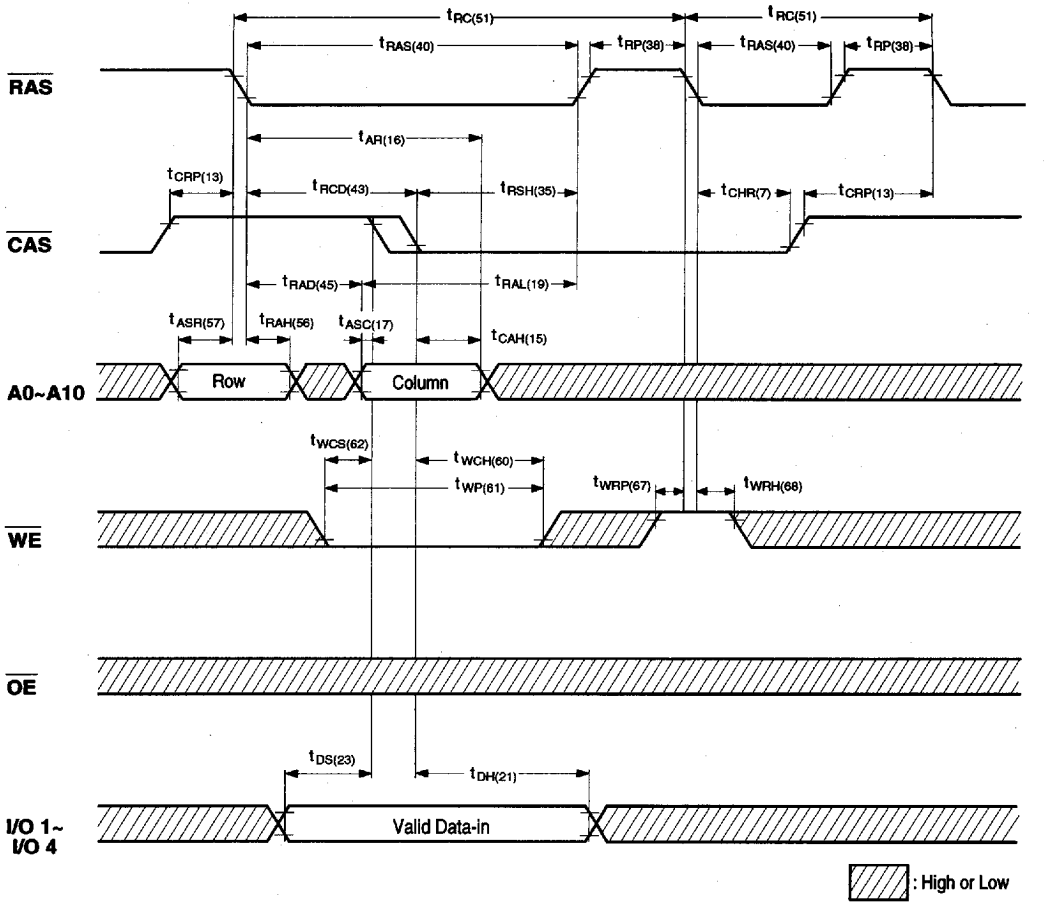
: High or Low

Note: $\overline{OE}$, A0~A10 = Don't care.
$\overline{WE}$ must be high at the falling edge of $\overline{RAS}$ in order to prevent from entering test mode.

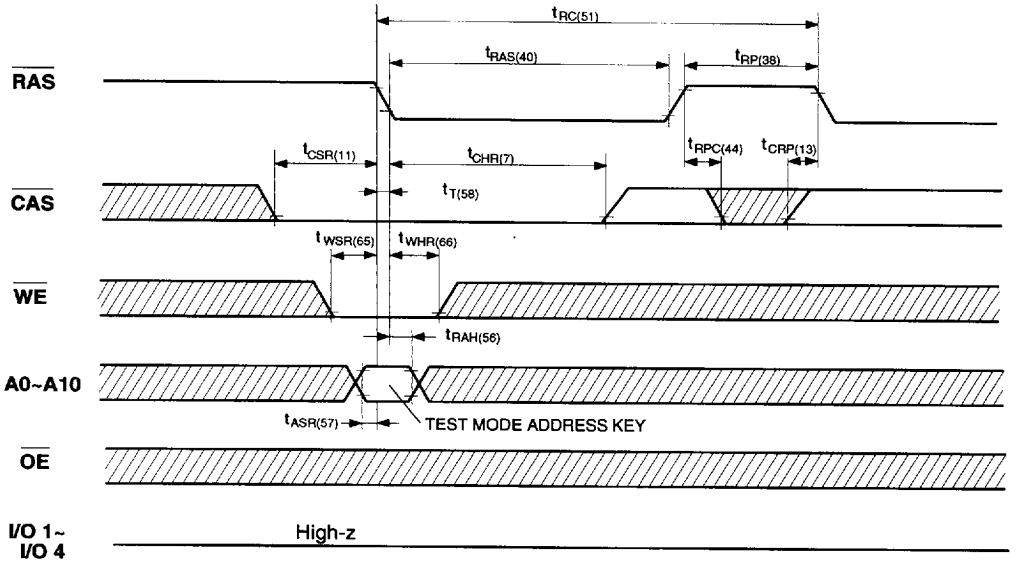
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



TEST MODE SET CYCLE ($\overline{WE}$, $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE)



Note : TEST MODE ADDRESS KEY
A5 and A6 must be "High".
A4 and A7 must be "Low".
All other address are "Don't care".

: High or Low

■ The NN51V17405B has a 16 bit parallel Test Mode Function for reducing test time. In the Test Mode, memory configuration is 1M x 16 bits and the Column address A0 and A1 address is ignored.

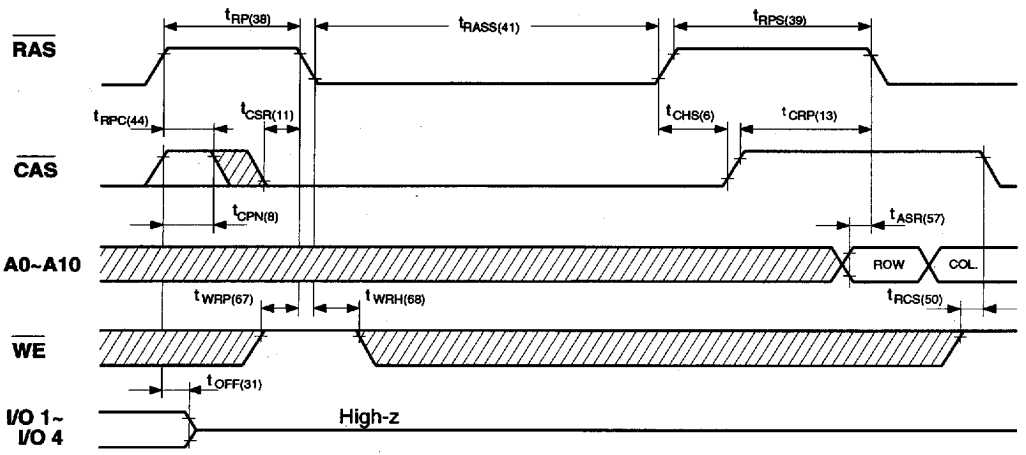
a. Entering the test mode:
The NN51V17405B test mode is entered by using the test mode set cycle ($\overline{WE}$,$\overline{CAS}$ before $\overline{RAS}$ cycle).

b. Read/Write operation in test mode:
For Write cycle, data input from each I/O (I/O1~I/O4) is written to 4 bit memory cells (total 16bits) at the same time.
During the read cycle, if the 4 bits of data are equal then a "1" is output from each I/O.
If there is a difference in the read data for a given 4 bit combination, a "0" will be output from that I/O.

c. Exiting the test mode:
The NN51V17405B will exit the test mode by either a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle width $\overline{WE}$ "high".

d. Refresh during test mode:
During test mode refresh must be executed by a normal Read cycle or a $\overline{WE}$, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

SELF REFRESH MODE



■ The NN51V17405B (L version) has a Self Refresh Mode.

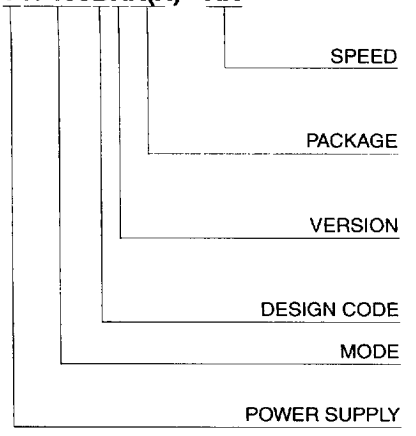
a. Entering the Self Refresh Mode:
The NN51V17405BL Self Refresh Mode is entered by using $\overline{CAS}$ before $\overline{RAS}$ cycle and holding $\overline{RAS}$ and $\overline{CAS}$ signal " low " longer than 300μs.

b. Continuing the Self Refresh Mode:
The Self Refresh Mode is continued by holding $\overline{RAS}$ " low " after entering the Self Refresh Mode.
It does not depend on being $\overline{CAS}$ " high " or " low " after entering the Self Refresh Mode for to continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:
The NN51V17405BL exits the Self Refresh Mode when the $\overline{RAS}$ signal is brought " high ".

ORDERING INFORMATION

NN51V17405BXX(X) - XX



SPEED	50	:	50ns
	60	:	60ns
	70	:	70ns
PACKAGE	J	:	Plastic SOJ
	TT	:	Plastic TSOP TYPE II
VERSION	BLANK	:	Standard Version
	L	:	Long Refresh Version 128ms Refresh
DESIGN CODE	B		
MODE	17405	:	EDO (Hyper Page) Mode 4M x 4 ,2048 Refresh Cycle
POWER SUPPLY	V	:	3.3V Version