

DESCRIPTION

The NN51V17805B series is a high performance CMOS Dynamic Random Access Memory organized as 2,097,152 words by 8 bits. The NN51V17805B series is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN51V17805B series features EDO (Hyper page) mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

Refresh is accomplished by performing $\overline{\text{RAS}}$ only refresh cycles, hidden refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, or normal read or write cycles on the 2,048 address combinations of A0 to A10 during a 32 ms period.

Multiplexed address inputs permit the NN51V17805B series to be packaged in a standard 28-pin plastic SOJ, plastic TSOP II. The package sizes provide high system bit densities. System level features include single power supply of 3.3V $\pm 10\%$ tolerance and direct interface with high performance TTL logic families.

FEATURES

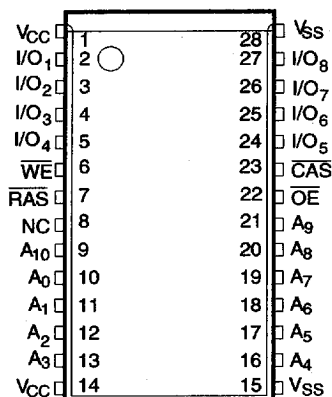
- 2,097,152 × 8 bit Organization
- Single 3.3V $\pm 10\%$ Power Supply
- Performance Ranges

Parameter	-50	-60	-70
Max. $\overline{\text{RAS}}$ Access Time (t_{RAC})	50ns	60ns	70ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	15ns	17ns	20ns
Max. Column Address Access Time (t_{AA})	25ns	30ns	40ns
Min. Read/Write Cycle Time (t_{RC})	90ns	110ns	130ns

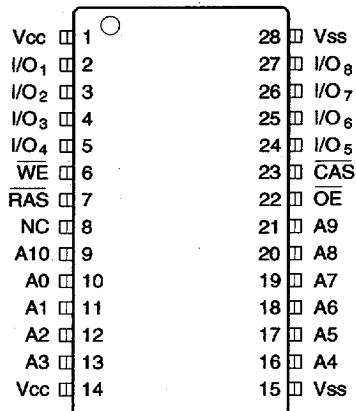
- EDO (Hyper Page) Mode Operation
- Low Power Operation
 - Low Standby Current (CMOS level input)
 - Standard 1mA
 - L version 150 μ A
- 2048 Refresh Cycles
 - Standard 32ms
 - L version 128ms
- Self Refresh Mode (L version)
- All inputs/Outputs and Clocks fully TTL and CMOS compatible
- Refresh Modes
 - $\overline{\text{RAS}}$ only
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$
 - Hidden Refresh
- High Reliability Package
 - Plastic 28pin SOJ (P28SJ-2B-L)
 - Plastic 28pin TSOP (P28TP-2B-L)

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PIN CONFIGURATION



28-pin SOJ (400mil)
P28SJ-2B-L



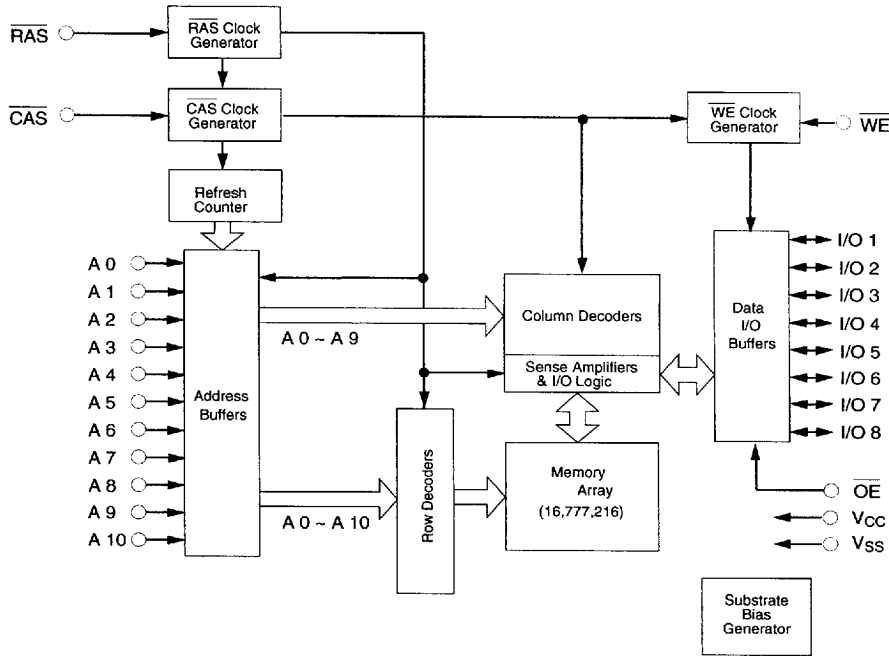
28-pin TSOP TYPE II (400mil)
P28SJ-2B-L

PIN NAMES

A0-A10	Address Inputs Row/Refresh :A0~A10 Column :A0~A9
RAS	Row Address Strobe
CAS	Column Address Strobe
OE	Output Enable
I/O1~I/O8	Data-in / Data-out
WE	Write Enable
Vcc	+3.3V Supply
Vss	Ground
NC	No Connection

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FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	-0.5 to 4.6	V
Voltage on V_{CC} Relative to V_{SS}	V_{CC}	-0.5 to 4.6	V
Storage Temperature (Plastic)	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	1.0	W
Ambient Operating Temperature	T_a	0 to +70	°C
Short Circuit Output Current	I_{out}	20	mA

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage, All Inputs	2.0	—	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage, All Inputs	-0.3	—	0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS} unless otherwise specified.

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DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 3.3V ±10%)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I _{CC1}	Operating Current	-50 -60 -70		120 110 100	mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS, Address cycling	1, 2
I _{CC2}	Standby Current			1.0	mA	RAS = CAS ≥ (V _{CC} - 0.2V)	
				2.0	mA	RAS = CAS ≥ V _{IH}	
I _{CC2}	Standby Current (L version)			150	μA	RAS = CAS ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC3}	Refresh Current (RAS only refresh)	-50 -60 -70		120 110 100	mA mA mA	t _{RC} = t _{RC} (min.) RAS cycling, CAS = V _{IH}	1
I _{CC4}	EDO (Hyper) Page Mode Current	-50 -60 -70		110 100 90	mA mA mA	t _{HPC} = t _{HPC} (min.) RAS = V _{IL} CAS, Address cycling	1,2
I _{CC5}	Refresh Current (CAS before RAS refresh)	-50 -60 -70		120 110 100	mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS cycling	1
I _{CC6}	Refresh Current CAS before RAS refresh)			500	μA	2,048 cycles / 128ms t _{RAS} ≤ 200ns, WE ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC7}	Self Refresh Mode Current			300	μA	RAS = CAS ≤ (V _{SS} + 0.2V) All other input high levels are (V _{CC} - 0.2V) or input low levels are (V _{SS} + 0.2V)	
I _{L1}	Input Leakage Current (Any input pin)		-10	10	μA	0V ≤ V _{IH} ≤ 3.6V, Others = 0V	
I _{L0}	Output Leakage Current (For high impedance state)		-10	10	μA	RAS ≥ V _{IH} (min), CAS ≥ V _{IH} (min) 0V ≤ V _{OUT} ≤ 3.6V	
V _{OH}	Output High Voltage		2.4		V	I _{OH} = -2.0 mA	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 2.0 mA	

Notes: 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.

2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 3.3V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{IN1}	Address(A0 ~ A10)	—	5	pF
C _{IN2}	RAS, CAS, WE, OE	—	5	pF
C _{OUT}	I/O1 ~ I/O8	—	7	pF

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AC ELECTRICAL CHARACTERISTICS

Test conditions : $V_{IH}/V_{IL} = 2.4V / 0.8V$ $V_{OH}/V_{OL} = 2.0V / 0.8V$ output loading $C_L = 100pF + 1TTL$
 Operating conditions : ($0^\circ C \leq T_a \leq 70^\circ C$, $V_{CC} = 3.3V \pm 10\%$, $V_{SS} = 0V$) (NOTES 3, 4, 5)

NO.	NOTES		PARAMETER	-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	17	—	20	ns	6,13
2	t_{CH2QV}	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	30	—	35	—	40	ns	13,14
3	t_{AVQV}	t_{AA}	Access Time from Column Address	—	25	—	30	—	40	ns	7,13
4	t_{RL1QV}	t_{RAC}	Access Time from RAS	—	50	—	60	—	70	ns	6,7
5	t_{RL1CH1}	t_{CSH}	CAS Hold Time	35	—	40	—	45	—	ns	
6	t_{RL1CX}	t_{CHS}	CAS Hold Time (Self Refresh Mode)	-50	—	-50	—	-50	—	ns	
7	t_{RL1CH1}	t_{CHR}	CAS Hold Time (CAS before RAS Refresh)	10	—	10	—	10	—	ns	
8	t_{CH2CL2}	t_{CPN}	CAS Precharge Time (CAS before RAS Refresh)	7	—	10	—	10	—	ns	
9	t_{CH2CL2}	t_{CP}	CAS Precharge Time	5	—	5	—	5	—	ns	14
10	t_{CL1CH1}	t_{CAS}	CAS Pulse Width	8	100K	10	100K	15	100K	ns	
11	t_{CL1RL2}	t_{CSR}	CAS Setup Time (CAS before RAS Refresh)	5	—	5	—	5	—	ns	
12	t_{CL1QX}	t_{CLZ}	CAS to Output in Low-Z	0	—	0	—	0	—	ns	8
13	t_{CH2RL2}	t_{CRP}	CAS to RAS Precharge Time	5	—	5	—	5	—	ns	
14	t_{CL1WL2}	t_{CWD}	CAS to WE Delay Time	32	—	37	—	42	—	ns	11
15	t_{CL1AX}	t_{CAH}	Column Address Hold Time	7	—	10	—	12	—	ns	
16	t_{RL1AX}	t_{AR}	Column Address Hold Time Referenced to RAS	35	—	40	—	40	—	ns	
17	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	ns	14
18	t_{AVCH1}	t_{CAL}	Column Address to CAS Lead Time	13	—	18	—	23	—	ns	
19	t_{AVRH1}	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	—	30	—	35	—	ns	
20	t_{AVWL2}	t_{AWD}	Column Address to WE Delay Time	39	—	47	—	54	—	ns	11
21	t_{CL1DX} t_{WL1DX}	t_{DH}	Data Hold Time	7	—	10	—	10	—	ns	12
22	t_{CL2QX}	t_{DHC}	Data Output Hold Time	0	—	0	—	0	—	ns	
23	t_{DVCL2} t_{DVWL2}	t_{DS}	Data Setup Time	0	—	0	—	0	—	ns	12
24	t_{OL1QV}	t_{OEA}	OE Access Time	—	15	—	17	—	20	ns	
25	t_{WL1OL2}	t_{OEH}	OE Command Hold Time	13	—	15	—	20	—	ns	
26	t_{GH2GL2}	t_{OPZ}	OE Pulse Width for Output Disable When CAS High	7	—	7	—	7	—	ns	
27	t_{GL1CH1}	t_{OCS}	OE Setup Time to $\overline{CAS}$ High	7	—	7	—	7	—	ns	
28	t_{GL1RH1}	t_{ORS}	OE Setup Time to $\overline{RAS}$ High	7	—	7	—	7	—	ns	
29	t_{CH2QV}	t_{OED}	OE to Data Delay Time	15	—	15	—	20	—	ns	
30	t_{GL2QX}	t_{OLZ}	OE to Output in low-Z	0	—	0	—	0	—	ns	
31	t_{CH2QZ}	t_{OFF}	Output Buffer Turn-off Delay Time	0	13	0	15	0	20	ns	10,17
32	t_{OH2QX}	t_{OEZ}	Output Buffer Turn-off Delay Time Referenced to OE	0	13	0	15	0	20	ns	
33	t_{RHQZ}	t_{OFR}	Output Buffer Turn-off Delay Time Referenced to RAS	0	13	0	15	0	20	ns	16
34	t_{WL2QZ}	t_{WEZ}	Output Buffer Turn-off Delay Time Referenced to WE	0	13	0	15	0	20	ns	

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NN51V17805B series
CMOS 2M × 8bit Dynamic RAM

NO.	SYMBOL		PARAMETER	-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
35	t _{CL1RH1}	t _{RS}	RAS Hold Time	13	—	15	—	18	—	ns	
36	t _{OL1RH1}	t _{ROH}	RAS Hold Time Referenced to $\overline{OE}$	10	—	10	—	10	—	ns	
37	t _{CH2RH1}	t _{RHCP}	RAS Hold Time Referenced CAS Precharge	30	—	35	—	40	—	ns	
38	t _{RH2RL2}	t _{RP}	RAS Precharge Time	25	—	30	—	40	—	ns	
39	t _{RH2RL2}	t _{RPS}	RAS Precharge Time (Self Refresh Mode)	90	—	110	—	130	—		
40	t _{RL1RH1}	t _{RAS}	RAS Pulse Width	50	100K	60	100K	70	100K	ns	
41	t _{RL1RH1}	t _{RASS}	RAS Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	μs	
42	t _{RL1RH1}	t _{RASP}	RAS Pulse Width (EDO (Hyper Page) Mode)	50	100K	60	100K	70	100K	ns	
43	t _{RL1CL1}	t _{RCD}	RAS to $\overline{CAS}$ Delay Time	13	35	13	45	13	50	ns	6
44	t _{RH2CL2}	t _{RPC}	RAS to CAS Precharge Time	5	—	5	—	5	—	ns	
45	t _{RL1AV}	t _{RAD}	RAS to Column Address Delay Time	11	25	11	30	11	35	ns	7
46	t _{RL2QX}	t _{RLZ}	RAS To Output in Low-Z	0	—	0	—	0	—	ns	
47	t _{RL1WL1}	t _{RWD}	RAS to $\overline{WE}$ Delay Time	64	—	77	—	89	—	ns	11
48	t _{CH2WL2}	t _{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	9
49	t _{RH2WL2}	t _{RRH}	Read Command Hold Time Referenced to RAS	0	—	0	—	0	—	ns	9
50	t _{WH2CL2}	t _{RCS}	Read Command Setup Time	0	—	0	—	0	—	ns	
51	t _{RL2RL2}	t _{RC}	Random Read or Write Cycle Time	90	—	110	—	130	—	ns	
52	t _{CL2CL2}	t _{HPC}	Read or Write Cycle Time (EDO (Hyper Page) Mode)	20	—	25	—	30	—	ns	13,14
53	t _{RL2RL2}	t _{RMW}	Read-Modify-Write Cycle Time	120	—	140	—	160	—	ns	
54	t _{CL2CL2}	t _{PRMW}	Read-Modify-Write Cycle Time (EDO (Hyper Page) Mode)	55	—	65	—	75	—	ns	13,14
55	t _{REF}	t _{REF}	Refresh Period	—	32	—	32	—	32	ms	15
56	t _{RL1AX}	t _{RAH}	Row Address Hold Time	8	—	8	—	8	—	ns	
57	t _{AVRL2}	t _{ASR}	Row Address Setup Time	0	—	0	—	0	—	ns	
58	t _T	t _T	Transition Time (Rise and Fall)	1	50	1	50	1	50	ns	4,5
59	t _{WL1WH1}	t _{WPZ}	$\overline{WE}$ Pulse Width for Disable When CAS High	7	—	7	—	7	—	ns	
60	t _{CL1WH1}	t _{WCH}	Write Command Hold Time	10	—	10	—	15	—	ns	
61	t _{WL1WH1}	t _{WP}	Write Command Pulse Width	10	—	10	—	15	—	ns	
62	t _{WL1CL2}	t _{WCS}	Write Command Setup Time	0	—	0	—	0	—	ns	11
63	t _{WL1CH1}	t _{CWL}	Write Command to $\overline{CAS}$ Lead Time	7	—	10	—	13	—	ns	
64	t _{WL1RH1}	t _{RWL}	Write Command to RAS Lead Time	7	—	10	—	13	—	ns	
65	t _{WH2RL2}	t _{WRP}	$\overline{WE}$ to RAS Precharge Time	10	—	10	—	10	—	ns	
66	t _{RL1WH2}	t _{WRH}	$\overline{WE}$ to RAS Hold Time	10	—	10	—	10	—	ns	

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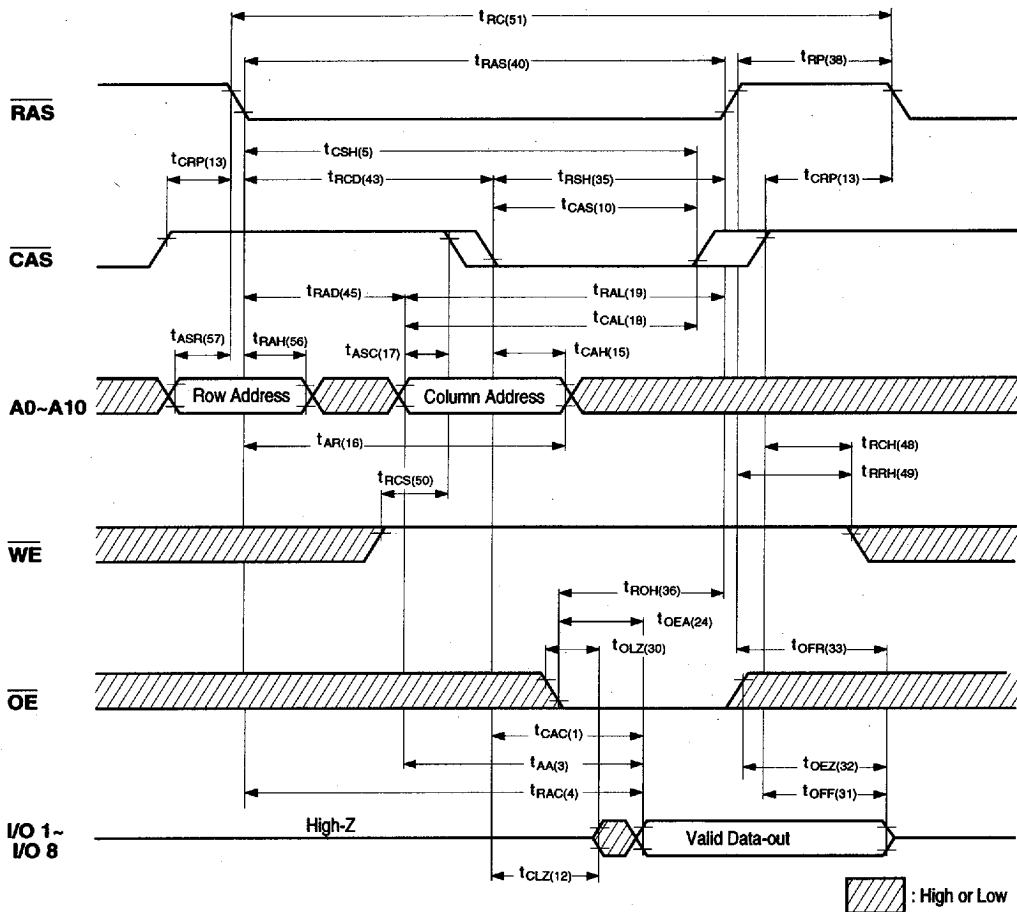
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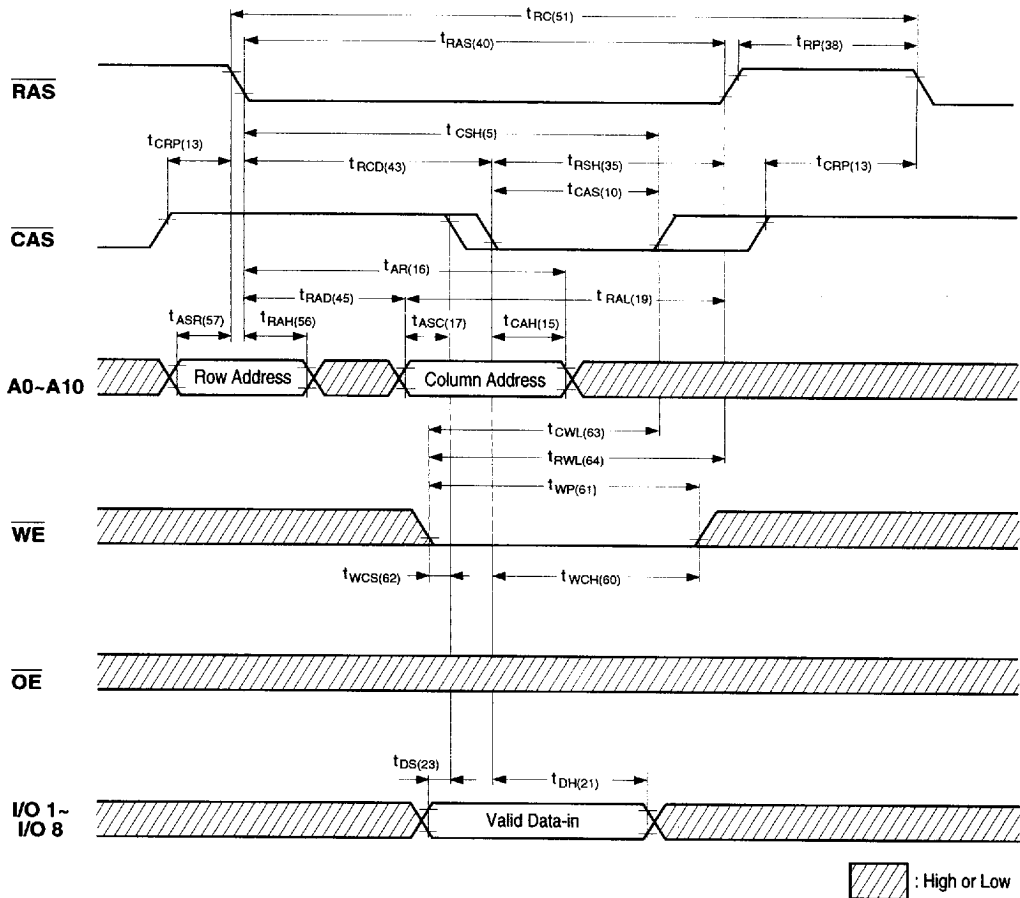
Notes:

3. Eight Initialization Cycles are required following a 200 μ s pause after Power Up. These Initialization Cycles may consist of any combination of the following : RAS only refresh Cycles, Read Cycles, Write Cycles. $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh Cycles.
4. AC measurements assume $t_f=2\text{ns}$.
5. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
6. Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
7. Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
8. Assumes three state test load (500 ohm to 1.4V Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. $t_{OFF}(\text{max.})$ defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels. t_{OFF} only applies when $\overline{\text{RAS}}$ is high.
11. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$ and $t_{AWD} \geq t_{AWD}(\text{min.})$, the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
12. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in read-modify-write cycles.
13. Access time is determined by the longer of t_{AA} , t_{CAC} , or t_{CPA} .
14. $t_{ASC} \geq t_{CP}$ to achieve $t_{PC}(\text{min.})$ and $t_{CPA}(\text{max.})$ values.
15. $t_{REF}=128\text{msec}$ for Long Refresh version (L version).
16. t_{OFF} applies only when $\overline{\text{CAS}}$ is high.
17. Output buffers turn into Hi-Z by the later rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, Therefore t_{OFF} and t_{OFF} are determined by the later rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$.

READ CYCLE

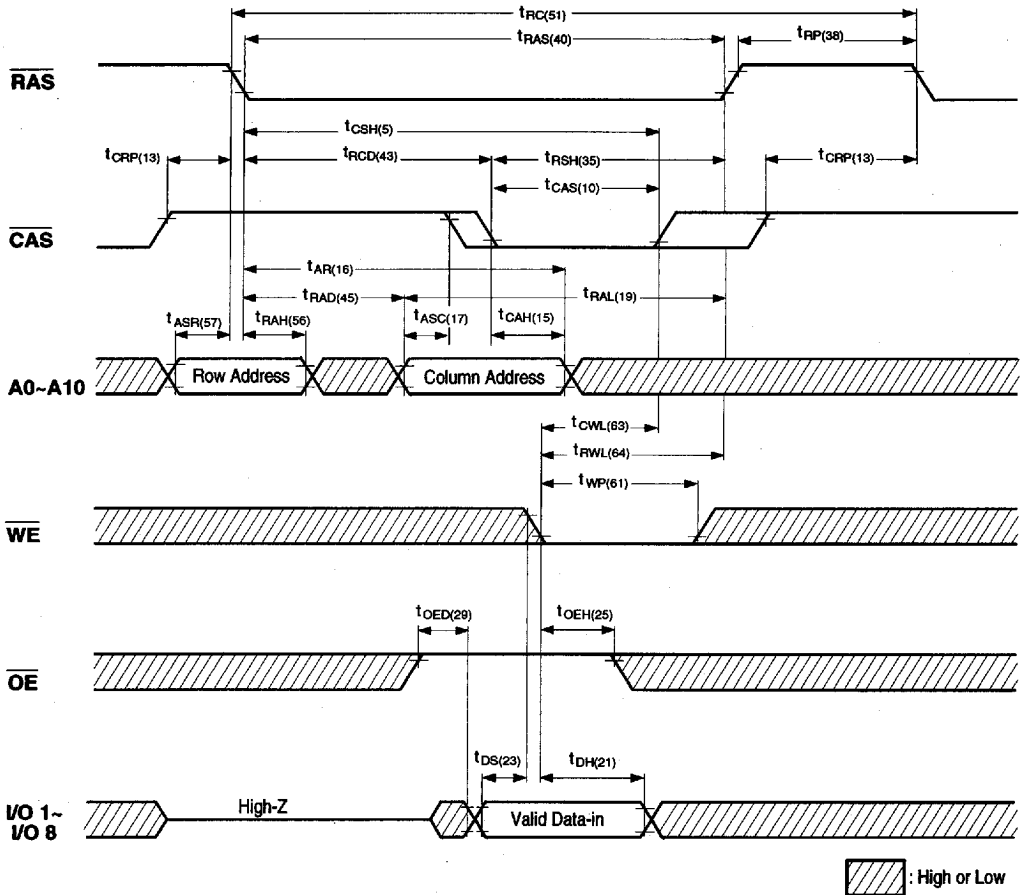


WRITE CYCLE (EARLY WRITE)



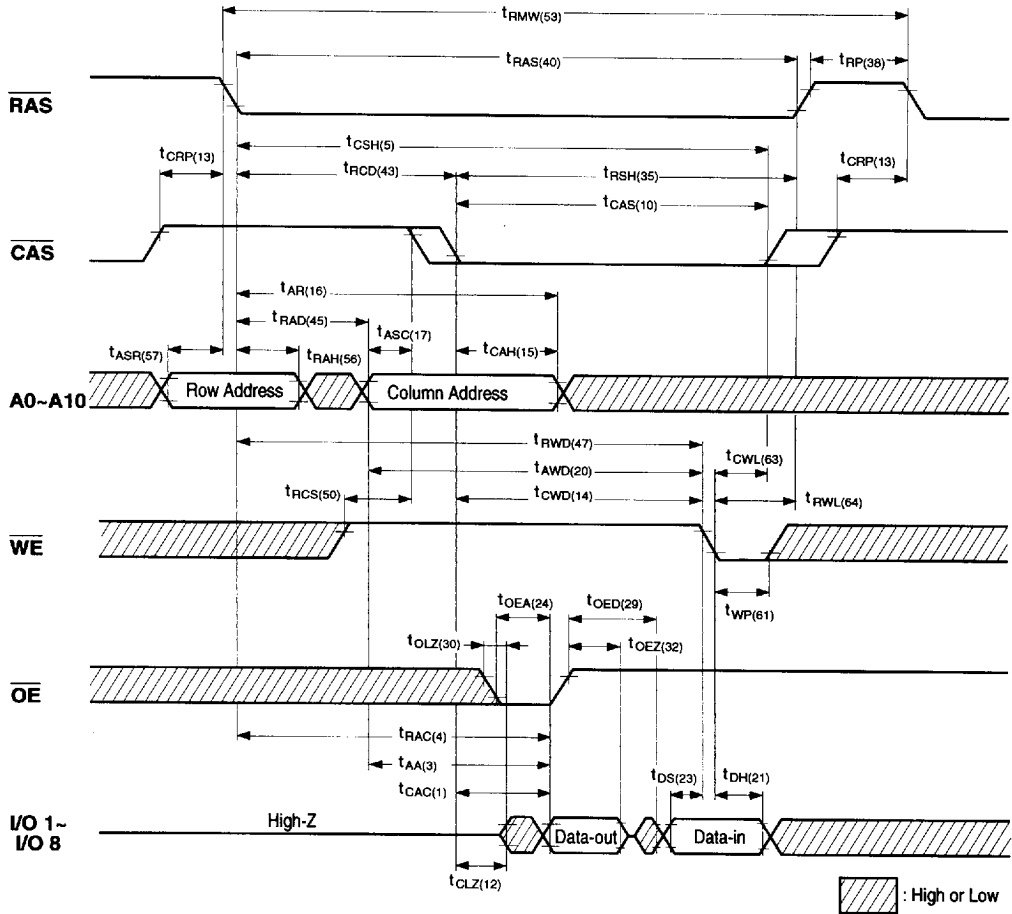
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WRITE CYCLE (OE-CONTROLLED WRITE)



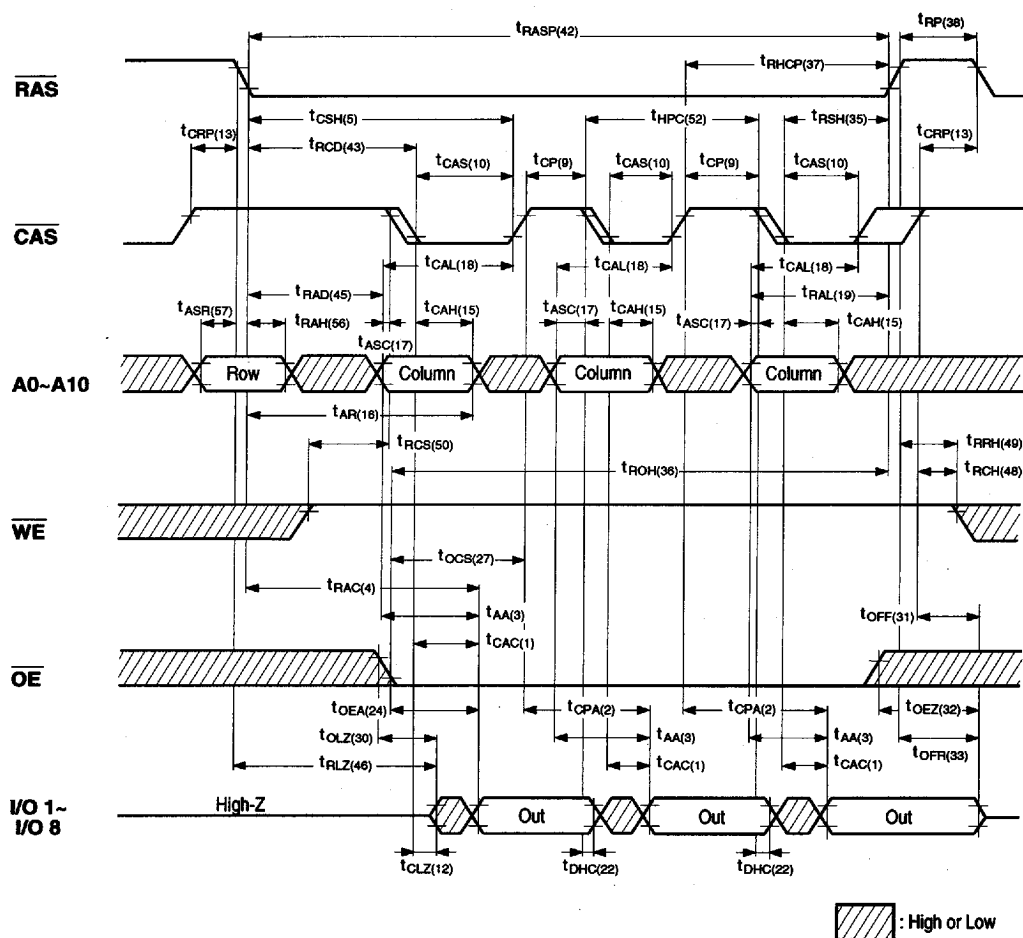
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READ-MODIFY-WRITE CYCLE

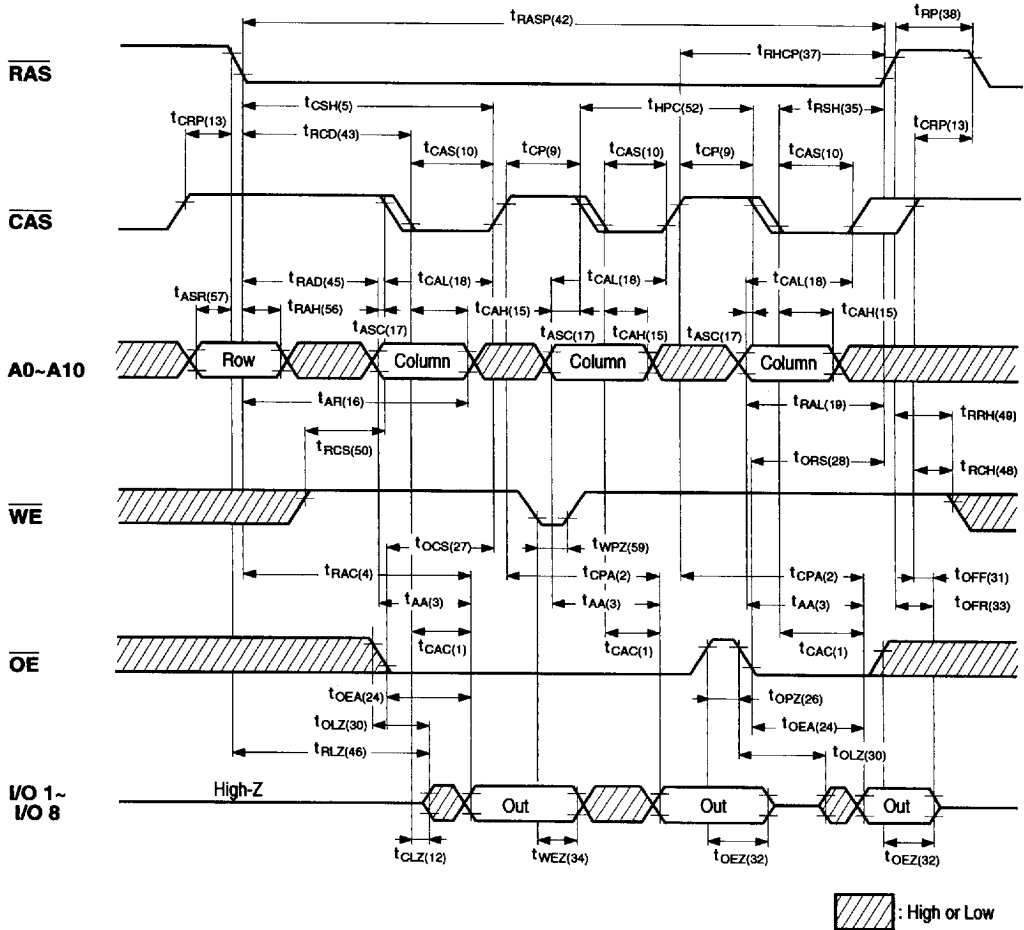


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EDO (HYPER PAGE) MODE READ CYCLE



EDO (HYPER PAGE) MODE READ CYCLE ($\overline{\text{OE}}$ AND $\overline{\text{WE}}$ CONTROLLED OUTPUT)



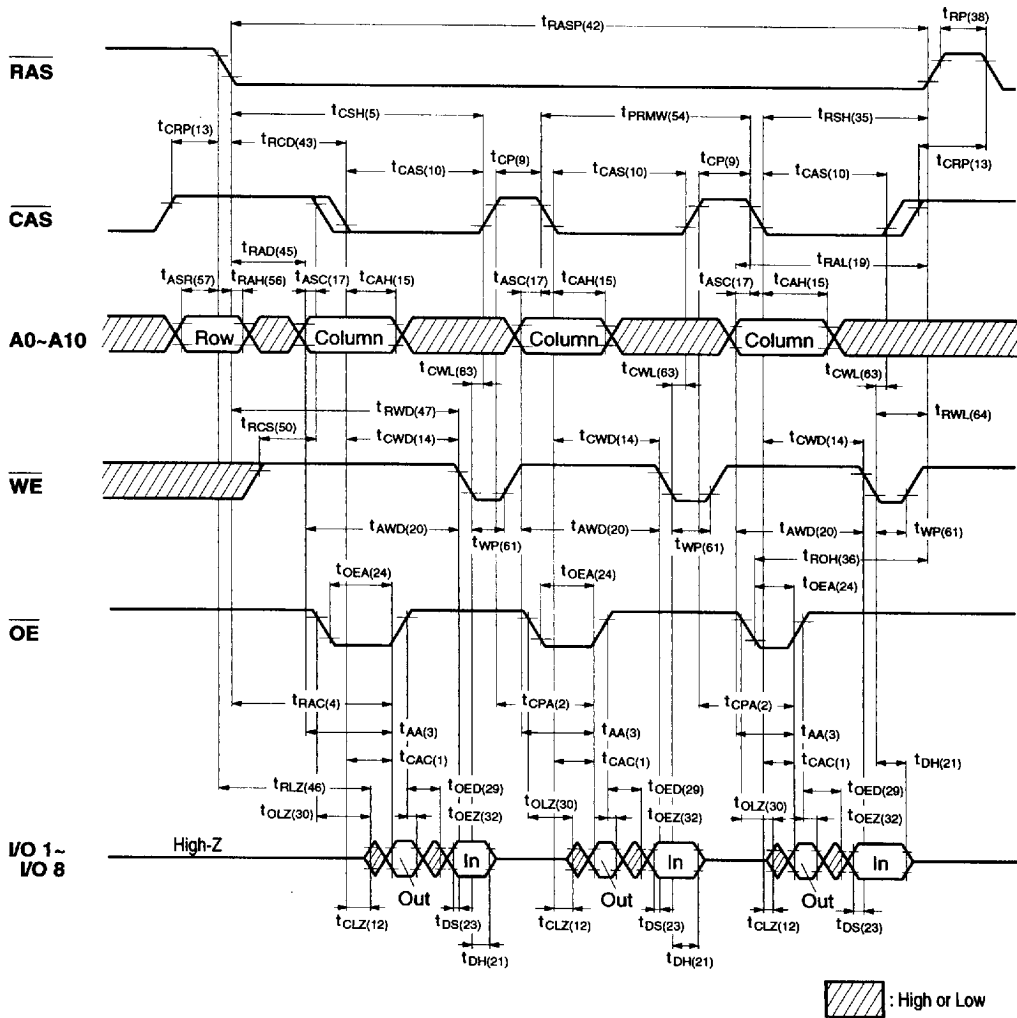
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EDO (HYPER PAGE) MODE EARLY WRITE CYCLE



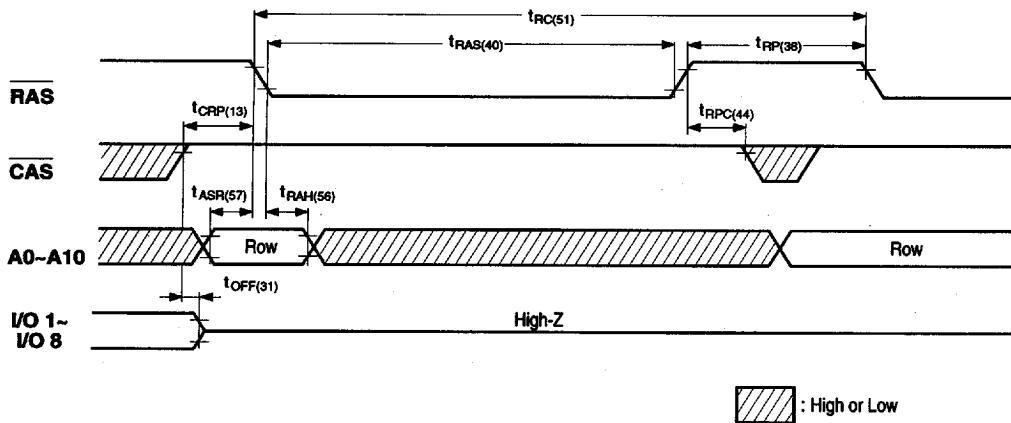
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EDO (HYPER PAGE) MODE READ-MODIFY-WRITE CYCLE



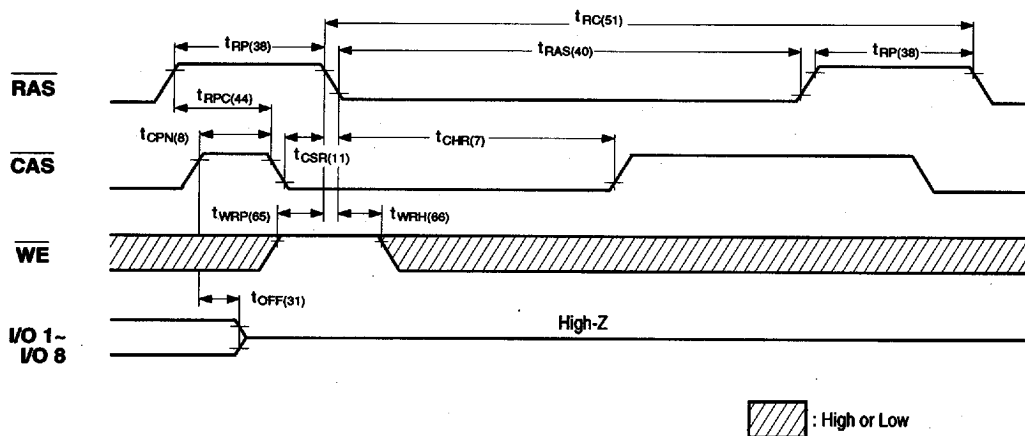
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$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



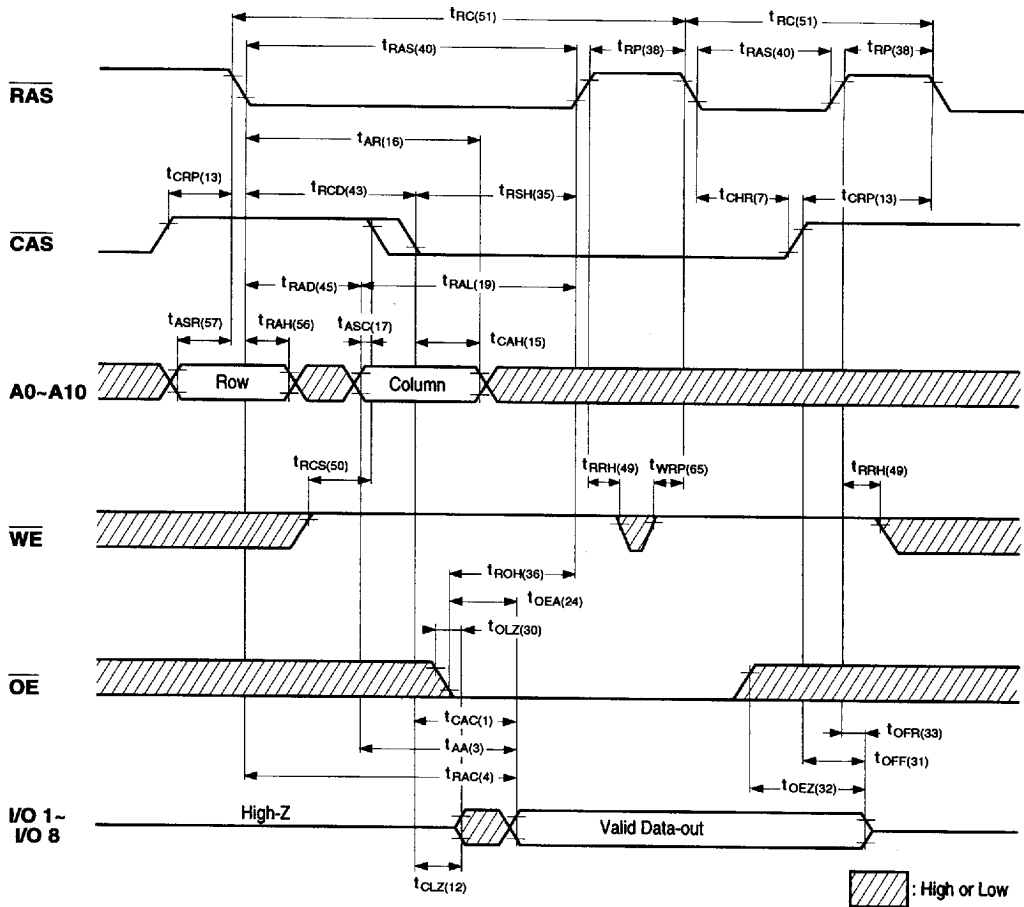
Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$ = Don't care.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



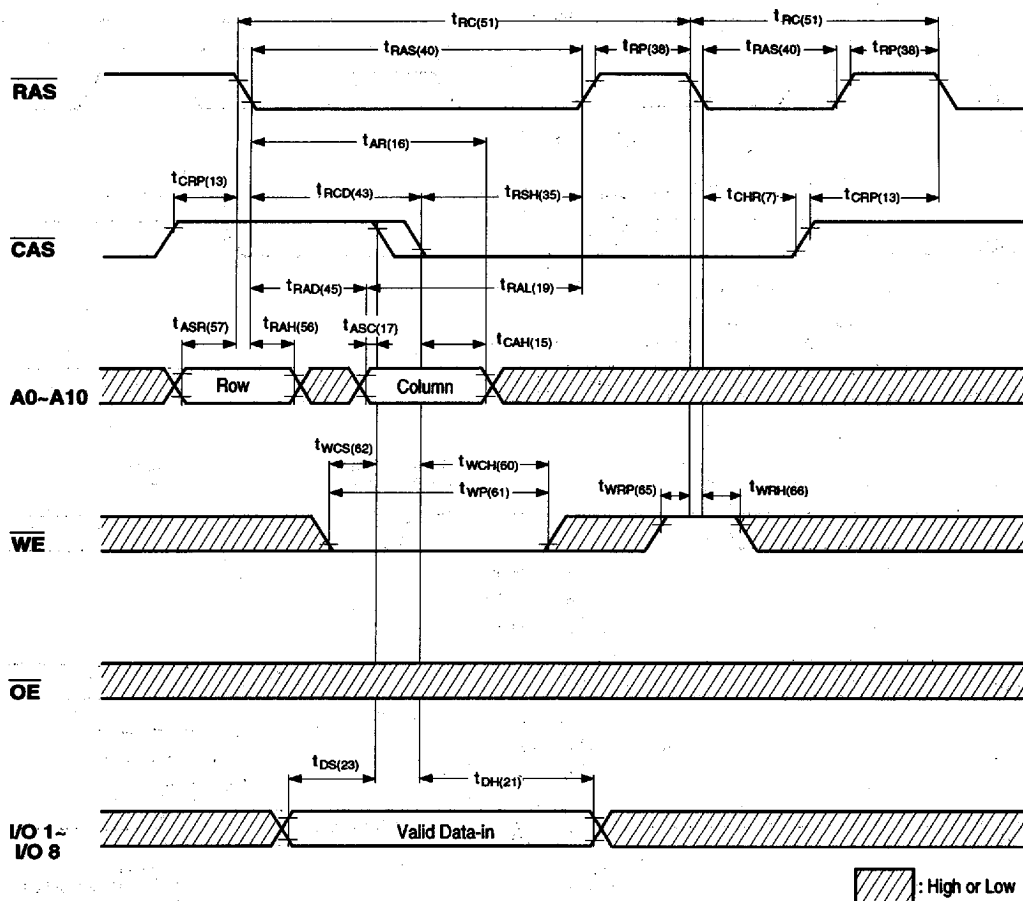
Note: $\overline{\text{OE}}$, A0~A10 = Don't care.

HIDDEN REFRESH CYCLE (READ)

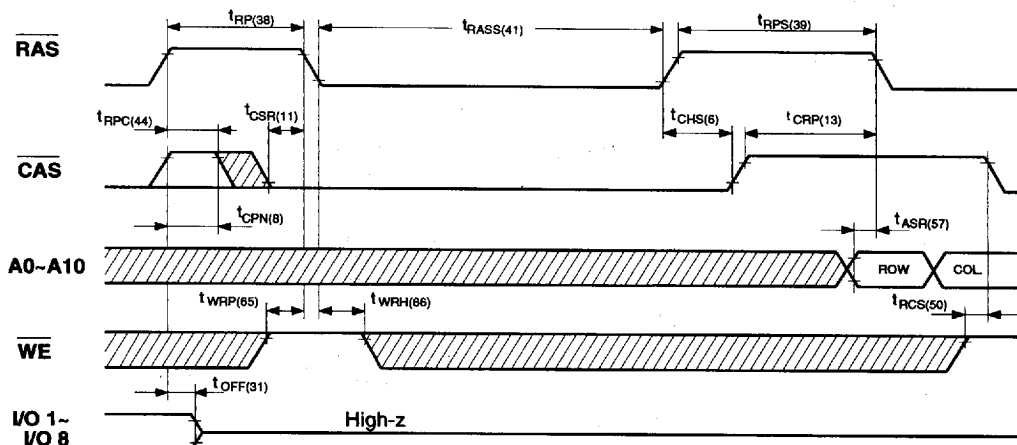


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HIDDEN REFRESH CYCLE (EARLY WRITE)



SELF REFRESH MODE



■ The NN51V17805B (L version) has a Self Refresh Mode.

a. Entering the Self Refresh Mode:

The NN51V17805BL Self Refresh Mode is entered by using $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle and holding $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signal "low" longer than 300 μ s.

b. Continuing the Self Refresh Mode:

The Self Refresh Mode is continued by holding $\overline{\text{RAS}}$ "low" after entering the Self Refresh Mode.

It does not depend on being $\overline{\text{CAS}}$ "high" or "low" after entering the Self Refresh Mode for to continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:

The NN51V17805BL exits the Self Refresh Mode when the $\overline{\text{RAS}}$ signal is brought "high".

ORDERING INFORMATION

NN51V17805BXX(X) - XX

	<u>SPEED</u>	50 : 50ns 60 : 60ns 70 : 70ns
	<u>PACKAGE</u>	J : Plastic SOJ TT : Plastic TSOP TYPE II
	<u>VERSION</u>	BLANK : Standard Version L : Long Refresh Version 128ms Refresh
	<u>DESIGN CODE</u>	B
	<u>MODE</u>	17805 : EDO (Hyper Page) Mode 2M x 8 ,2048 Refresh Cycle
	<u>POWER SUPPLY</u>	V : 3.3V Version