

DESCRIPTION

The NN51V4400B series is a high performance CMOS Dynamic Random Access Memory organized as 1,048,576 words by 4 bit. The NN51V4400B series is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN51V4400B series features a high speed page mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

The outputs are tri-stated by $\overline{\text{CAS}}$ which, in essence, acts as an output enable independent of $\overline{\text{RAS}}$ with very fast $\overline{\text{CAS}}$ to output access time.

Refresh is accomplished by performing $\overline{\text{RAS}}$ only refresh cycles, hidden refresh cycles, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles, or normal read or write cycles on the 1,024 address combinations of A0 to A9 during a 16 ms period.

Multiplexed address inputs permit The NN51V4400B series to be packaged in a standard 26-pin plastic SOJ, 26 pin TSOP TYPE II. The package sizes provide high system bit densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 3.3V $\pm 10\%$ tolerance and direct interface with high performance TTL logic families.

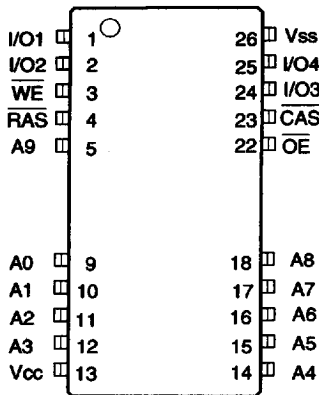
FEATURES

- 1,048,576 × 4 bit Organization
- Single 3.3V $\pm 10\%$ Power Supply
- Performance Ranges

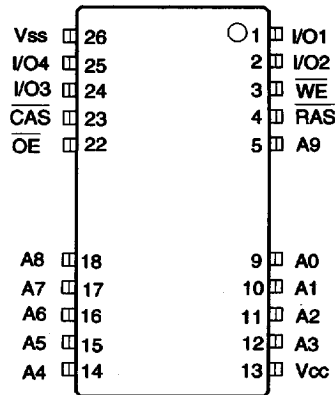
Parameter	-50	-60	-70
Max. $\overline{\text{RAS}}$ Access Time (t_{RAC})	50ns	60ns	70ns
Max. $\overline{\text{CAS}}$ Access Time (t_{CAC})	13ns	15ns	20ns
Max. Column Address Access Time (t_{AA})	27ns	30ns	35ns
Min. Read/Write Cycle Time (t_{RC})	90ns	110ns	130ns

- Fast Page Mode Operation
- Low Power Operation
 - Low Standby Current (CMOS level inputs)
 - Standard 1mA
 - L version 50 μ A
- 1,024 Refresh Cycles
 - Standard distributed across 16ms
 - L version distributed across 128ms
- Self Refresh Mode (L version)
- All inputs/Outputs and Clocks fully TTL and CMOS compatible
- Refresh Modes
 - $\overline{\text{RAS}}$ only
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$
 - Hidden Refresh
- ×8 bit Test Mode
- High Reliability Packages
 - Plastic 26pin SOJ (P26/20SJ-2A)
 - Plastic 26pin TSOP TYPE II (P26/20TP-2A/R)

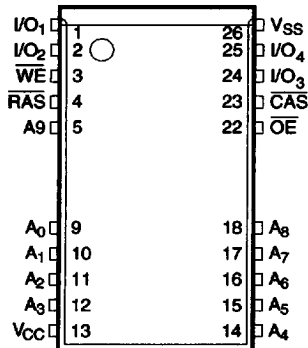
PIN CONFIGURATION (TOP VIEW)



26/20-pin TSOP TYPE (II)
 Normal Bend (300 mil)
 P26/20TP-2A



26/20-pin TSOP TYPE (II)
 Reverse Bend (300 mil)
 P26/20TP-2A-R

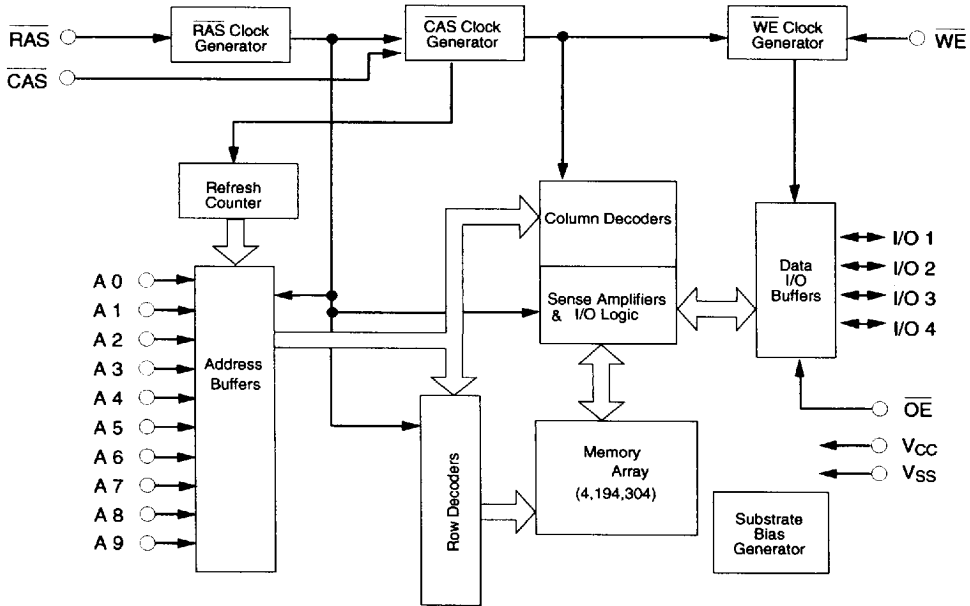


26/20-pin SOJ (300mil)
 P26/20SJ-2A

PIN NAMES

A0~A9	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
OE	Output Enable
I/O1~I/O4	Data-in / Data-out
WE	Write Enable
Vcc	+3.3V Supply
Vss	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V_{SS}	V_{in}, V_{out}	-0.5 to 4.6	V
Voltage on V_{CC} Relative to V_{SS}	V_{CC}	-0.5 to 4.6	V
Storage Temperature (Plastic)	T_{stg}	-55 to +125	°C
Power Dissipation	P_d	1.0	W
Ambient Operating Temperature	T_a	0 to +70	°C
Short Circuit Output Current	I_{out}	20	mA

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage, All Inputs	2.0	—	$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage, All Inputs	-0.3	—	0.8	V

Note: All voltage values in this data sheet are with respect to V_{SS} unless otherwise specified.

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DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V_{CC} = 3.3V ±10%)

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I _{CC1}	Operating Current	-50 -60 -70		90 80 70	mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS, Address cycling	1, 2
I _{CC2}	Standby Current			1.0 2.0	mA mA	RAS = CAS ≥ (V _{CC} - 0.2V) RAS = CAS ≥ V _{IH}	
	Standby Current (L version)			50	μA	RAS = CAS ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC3}	Refresh Current (RAS only refresh)	-50 -60 -70		90 80 70	mA mA mA	t _{RC} = t _{RC} (min.) RAS cycling, CAS = V _{IH}	1
I _{CC4}	Fast Page Mode Current	-50 -60 -70		60 50 40	mA mA mA	t _{PC} = t _{PC} (min.) RAS = V _{IL} CAS, Address cycling	1, 2
I _{CC5}	Refresh Current (CAS before RAS refresh)	-50 -60 -70		90 80 70	mA mA mA	t _{RC} = t _{RC} (min.) RAS, CAS cycling	1
I _{CC6}	Refresh Current (CAS before RAS refresh)			150	μA	1024 cycles / 128ms t _{RAS} ≤ 200ns, WE ≥ (V _{CC} - 0.2V) All other inputs are stable at (V _{CC} - 0.2V) or (V _{SS} + 0.2V)	
I _{CC7}	Self Refresh Mode Current			200	μA	RAS = CAS ≤ (V _{SS} + 0.2V) All other input high levels are (V _{CC} - 0.2V) or input low levels are (V _{SS} + 0.2V)	
I _{L1}	Input Leakage Current (Any input pin)		-10	10	μA	0V ≤ V _{IH} ≤ 3.3V, Others = 0V	
I _{L0}	Output Leakage Current (For high impedance state)		-10	10	μA	RAS ≥ V _{IH} (min.), CAS ≥ V _{IH} (min.) 0V ≤ V _{OUT} ≤ 3.6V	
V _{OH}	Output High Voltage		2.4		V	I _{OH} = -2.0 mA	
V _{OL}	Output Low Voltage			0.4	V	I _{OL} = 2.0 mA	

Notes: 1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rate.

2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the outputs open.

CAPACITANCE (0°C ≤ Ta ≤ 70°C, V_{CC} = 3.3V ±10%, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{IN1}	Address(A0 ~ A9)	—	5	pF
C _{IN2}	RAS, CAS, WE, OE	—	5	pF
C _{OUT}	I/O1, I/O2, I/O3, I/O4	—	7	pF

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A.C. OPERATING CONDITIONS (0 °C ≤ Ta ≤ 70 °C, V_{CC} = 3.3 V ± 10%, V_{SS} = 0 V) (NOTES 3, 4, 5)

NO.	NOTES		PARAMETER	-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t _{CL1QV}	t _{CAC}	Access Time from CAS	—	13	—	15	—	20	ns	6,13
2	t _{CH2QV}	t _{CPA}	Access Time from CAS Precharge	—	32	—	35	—	40	ns	13,14
3	t _{AVQV}	t _{AA}	Access Time from Column Address	—	27	—	30	—	35	ns	7,13
4	t _{RL1QV}	t _{RAC}	Access Time from RAS	—	50	—	60	—	70	ns	6,7
5	t _{RL1CH1}	t _{CSH}	CAS Hold Time	50	—	60	—	70	—	ns	
6	t _{RL1CH1}	t _{CHR}	CAS Hold Time (CAS before RAS Refresh)	10	—	10	—	10	—	ns	
7	t _{RL1CX}	t _{CHS}	CAS Precharge Time (Self Refresh Mode)	-50	—	-50	—	-50	—	ns	
8	t _{CH2CL2}	t _{CPN}	CAS Precharge Time (CAS before RAS Refresh)	10	—	10	—	10	—	ns	
9	t _{CH2CL2}	t _{CP}	CAS Precharge Time (Fast Page Mode)	5	—	5	—	5	—	ns	14
10	t _{CL1CH1}	t _{CAS}	CAS Pulse Width	13	100K	15	100K	20	100K	ns	
11	t _{CL1RL2}	t _{CSR}	CAS Setup Time (CAS before RAS Refresh)	5	—	5	—	5	—	ns	
12	t _{CL1QX}	t _{CLZ}	CAS to Output in Low-Z	0	—	0	—	0	—	ns	8
13	t _{CH2RL2}	t _{CRP}	CAS to RAS Precharge Time	5	—	5	—	5	—	ns	
14	t _{CL1WL2}	t _{CWD}	CAS to WE Delay Time	35	—	35	—	50	—	ns	11
15	t _{CL1AX}	t _{CAH}	Column Address Hold Time	10	—	15	—	15	—	ns	
16	t _{RL1AX}	t _{AR}	Column Address Hold Time Referenced to RAS	35	—	40	—	40	—	ns	
17	t _{AVCL2}	t _{ASC}	Column Address Setup Time	0	—	0	—	0	—	ns	14
18	t _{AVRH1}	t _{RAL}	Column Address to RAS Lead Time	24	—	30	—	35	—	ns	
19	t _{AVWL2}	t _{AWD}	Column Address to WE Delay Time	50	—	50	—	65	—	ns	11
20	t _{CL1DX} t _{WL1DX}	t _{DH}	Data Hold Time	10	—	10	—	15	—	ns	12
21	t _{DVCL2} t _{DVWL2}	t _{DS}	Data Setup Time	0	—	0	—	0	—	ns	12
22	t _{OL1QV}	t _{OEa}	OE Access Time	—	13	—	15	—	20	ns	
23	t _{WL1OL2}	t _{OEh}	OE Command Hold Time	13	—	15	—	20	—	ns	
24	t _{CH2QV}	t _{OED}	OE to Data Delay Time	8	—	10	—	10	—	ns	
25	t _{CH2QZ}	t _{OFF}	Output Buffer Turn-off Delay Time	0	13	0	15	0	20	ns	10
26	t _{OH2QX}	t _{OEZ}	Output Buffer Turn-off Delay Time Referenced to OE	0	10	0	15	0	15	ns	
27	t _{CL1RH1}	t _{RSH}	RAS Hold Time	13	—	15	—	20	—	ns	
28	t _{OL1RH1}	t _{ROH}	RAS Hold Time Referenced to OE	8	—	10	—	10	—	ns	
29	t _{RH2RL2}	t _{RP}	RAS Precharge Time	25	—	30	—	40	—	ns	
30	t _{RH2RL2}	t _{RPS}	RAS Precharge Time (Self Refresh Mode)	90	—	110	—	130	—	ns	
31	t _{RL1RH1}	t _{RAS}	RAS Pulse Width	50	100K	60	100K	70	100K	ns	
32	t _{RL1RH1}	t _{RASP}	RAS Pulse Width (Fast Page Mode)	50	100K	60	100K	70	100K	ns	
33	t _{RL1RH1}	t _{RASS}	RAS Pulse Width (Self Refresh Mode)	300	—	300	—	300	—	μs	
34	t _{RL1CL1}	t _{RCD}	RAS to CAS Delay Time	13	35	13	45	13	50	ns	6
35	t _{RH2CL2}	t _{RPC}	RAS to CAS Precharge Time	10	—	10	—	10	—	ns	
36	t _{RL1AV}	t _{RAD}	RAS to Column Address Delay Time	11	23	11	30	11	35	ns	7
37	t _{RL1WL2}	t _{RWD}	RAS to WE Delay Time	68	—	80	—	100	—	ns	11
38	t _{CH2WL2}	t _{RCH}	Read Command Hold Time	0	—	0	—	0	—	ns	9

NN51V4400B series
CMOS 1M × 4bit Dynamic RAM

NO.	SYMBOL		PARAMETER	-60		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
39	t_{RH2WL2}	t_{RRH}	Read Command Hold Time Referenced to RAS	5	—	5	—	5	—	ns	9
40	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	ns	
41	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	90	—	110	—	130	—	ns	
42	t_{CL2CL2}	t_{PC}	Read or Write Cycle Time (Fast Page Mode)	33	—	40	—	45	—	ns	13,14
43	t_{RL2RL2}	t_{RMW}	Read-Modify-Write Cycle Time	125	—	135	—	165	—	ns	
44	t_{CL2CL2}	t_{PRMW}	Read-Modify-Write Cycle Time (Fast Page Mode)	57	—	66	—	100	—	ns	13,14
45	t_{REF}	t_{REF}	Refresh Period	—	16	—	16	—	16	ms	15
46	t_{RL1AX}	t_{RAH}	Row Address Hold Time	8	—	8	—	8	—	ns	
47	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	ns	
48	t_T	t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	4,5
49	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	8	—	10	—	15	—	ns	
50	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	8	—	10	—	15	—	ns	
51	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0	—	0	—	0	—	ns	11
52	t_{WL1CH1}	t_{CWL}	Write Command to CAS Lead Time	13	—	15	—	20	—	ns	
53	t_{WL1RH1}	t_{RWL}	Write Command to RAS Lead Time	13	—	15	—	20	—	ns	
54	t_{WL1RL2}	t_{WSR}	Write Command Setup Time (Test Mode)	10	—	10	—	10	—	ns	
55	t_{RL1WH1}	t_{WHR}	Write Command Hold Time (Test Mode)	10	—	10	—	10	—	ns	
56	t_{WH2RL2}	t_{WRP}	WE to RAS Precharge Time (CAS before RAS)	10	—	10	—	10	—	ns	
57	t_{RL1WH2}	t_{WRH}	WE to RAS Hold Time (CAS before RAS)	10	—	10	—	10	—	ns	

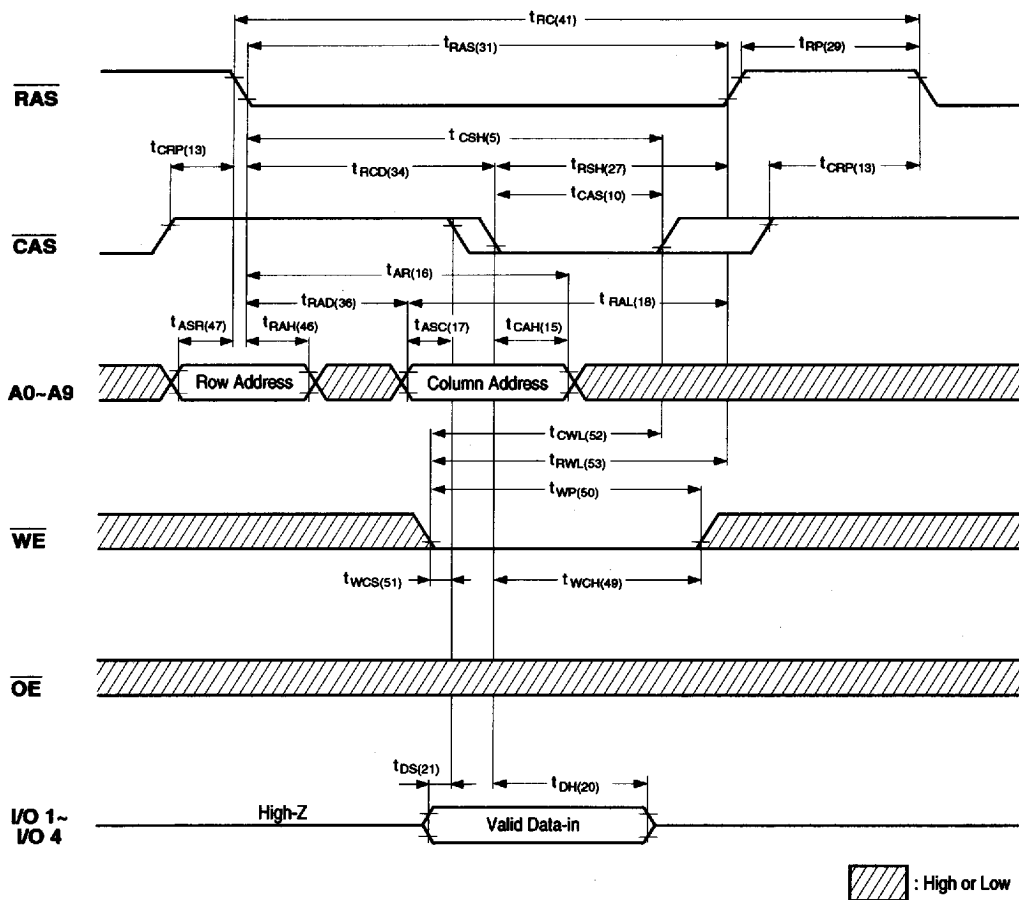
Notes:

- Eight Initialization Cycles are required following a 200 μ s pause after Power Up. These Initialization Cycles may consist of any combination of the following : RAS only refresh Cycles, Read Cycles, Write Cycles, CAS before RAS refresh Cycles.
- AC measurements assume $t_T=3$ ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$ and with a load equivalent to TTL loads and 50pF.
- $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
- Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
- Assumes three state test load (500 ohm to 1.4V Thevenin equivalent).
- Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- $t_{OFF}(\text{max.})$ defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
- t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$ and $t_{AWD} \geq t_{AWD}(\text{min.})$, the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
- These parameters are referenced to CAS leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
- Access time is determined by the longer of t_{AA} , t_{CAC} , or t_{CPA} .
- $t_{ASC} \geq t_{CP}$ to achieve $t_{PC}(\text{min.})$ and $t_{CPA}(\text{max.})$ values.
- $t_{REF}=128$ msec for Long Refresh version (L version).

NPNX

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WRITE CYCLE (EARLY WRITE)

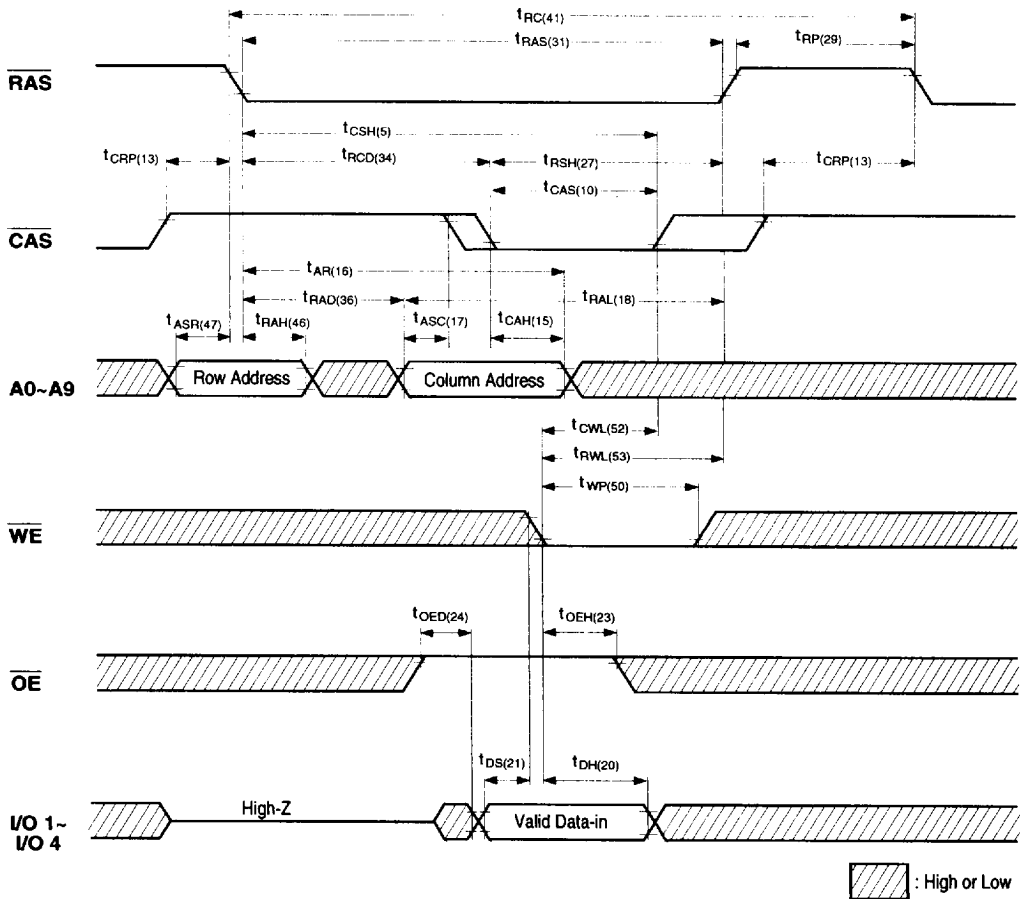


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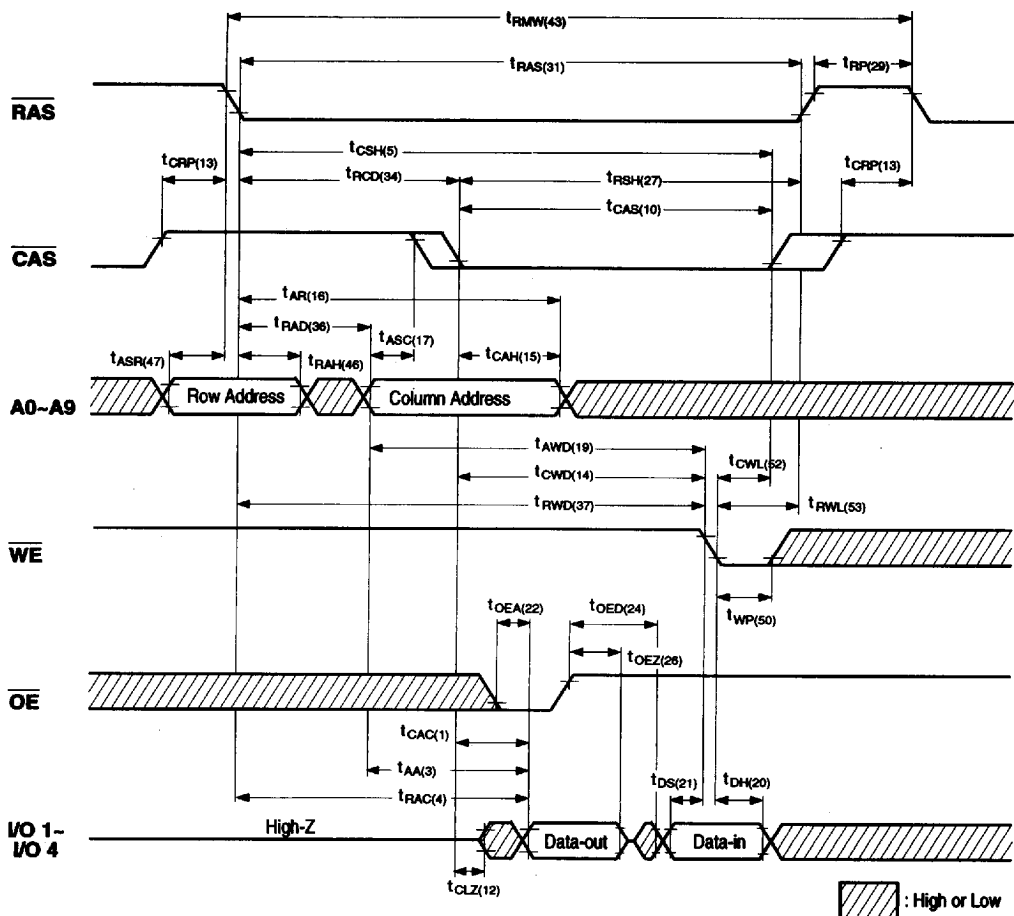
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WRITE CYCLE ($\overline{\text{OE}}$ -CONTROLLED WRITE)



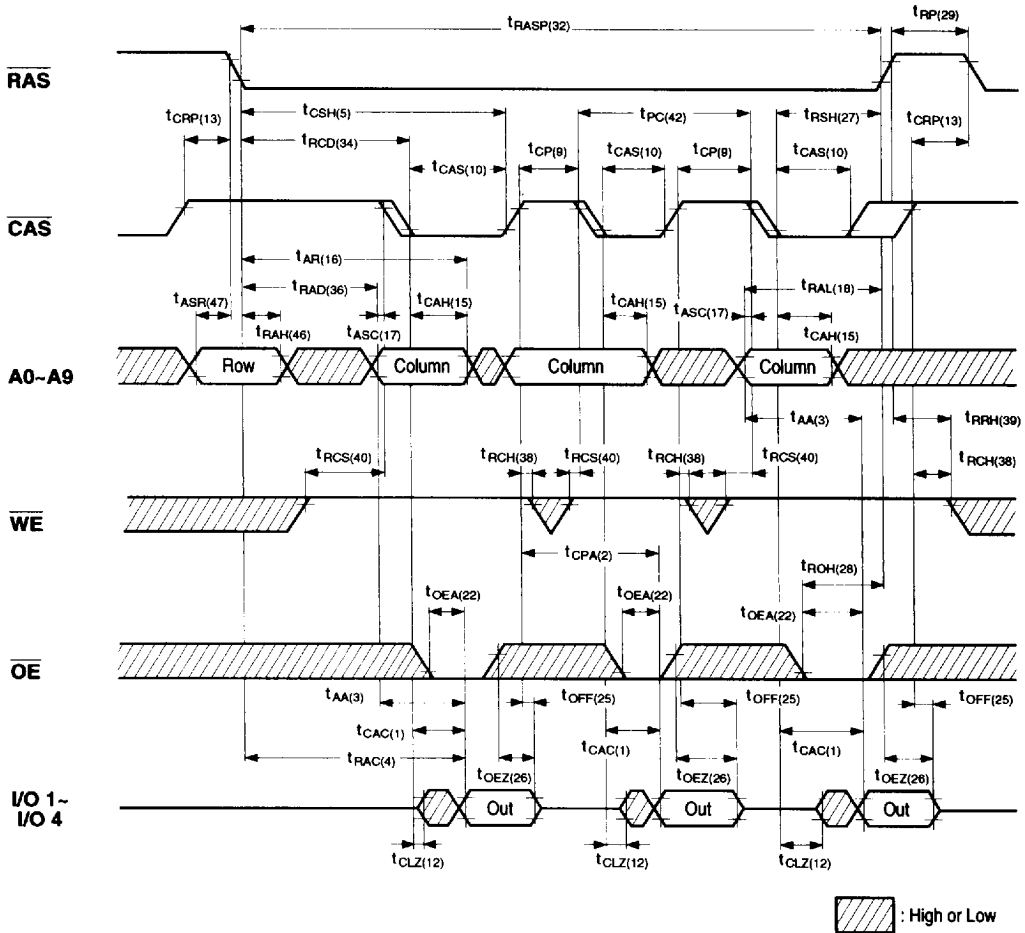
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READ-MODIFY-WRITE CYCLE



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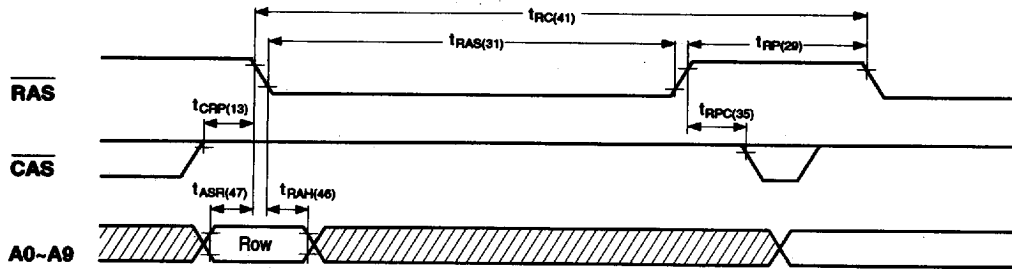
FAST PAGE MODE READ CYCLE



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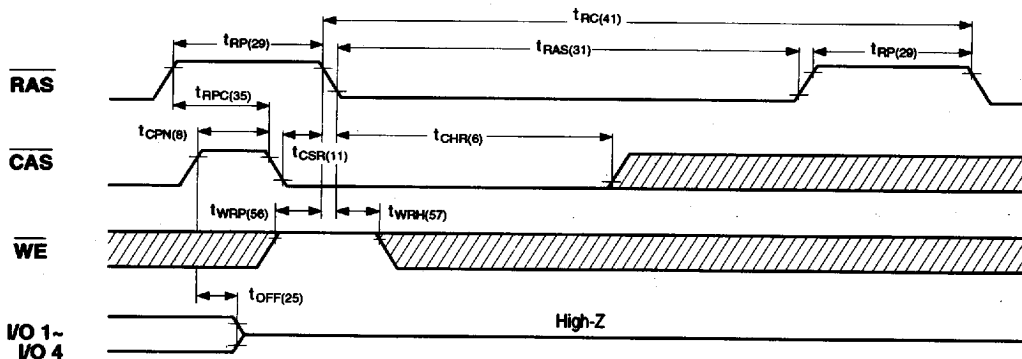
RAS ONLY REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$ = Don't care.

 : High or Low

CAS BEFORE RAS REFRESH CYCLE

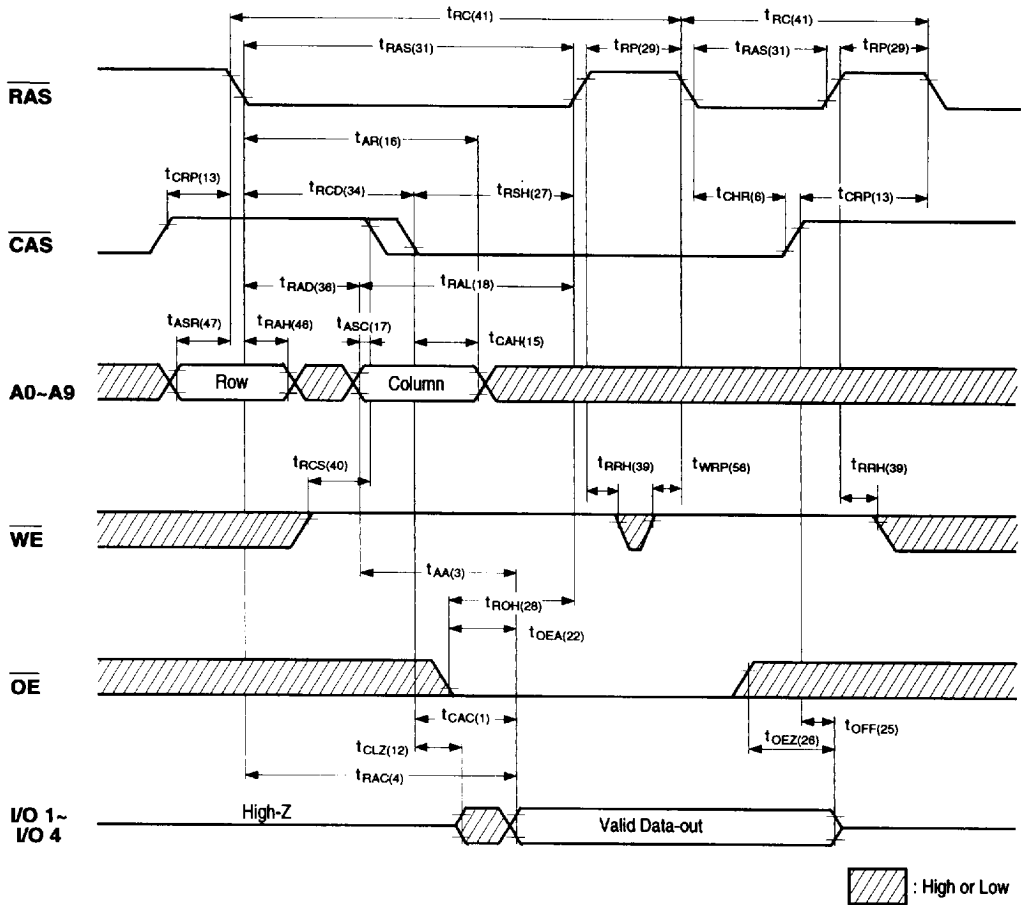


 : High or Low

Note: $\overline{OE}$, A0~A9 = Don't care.

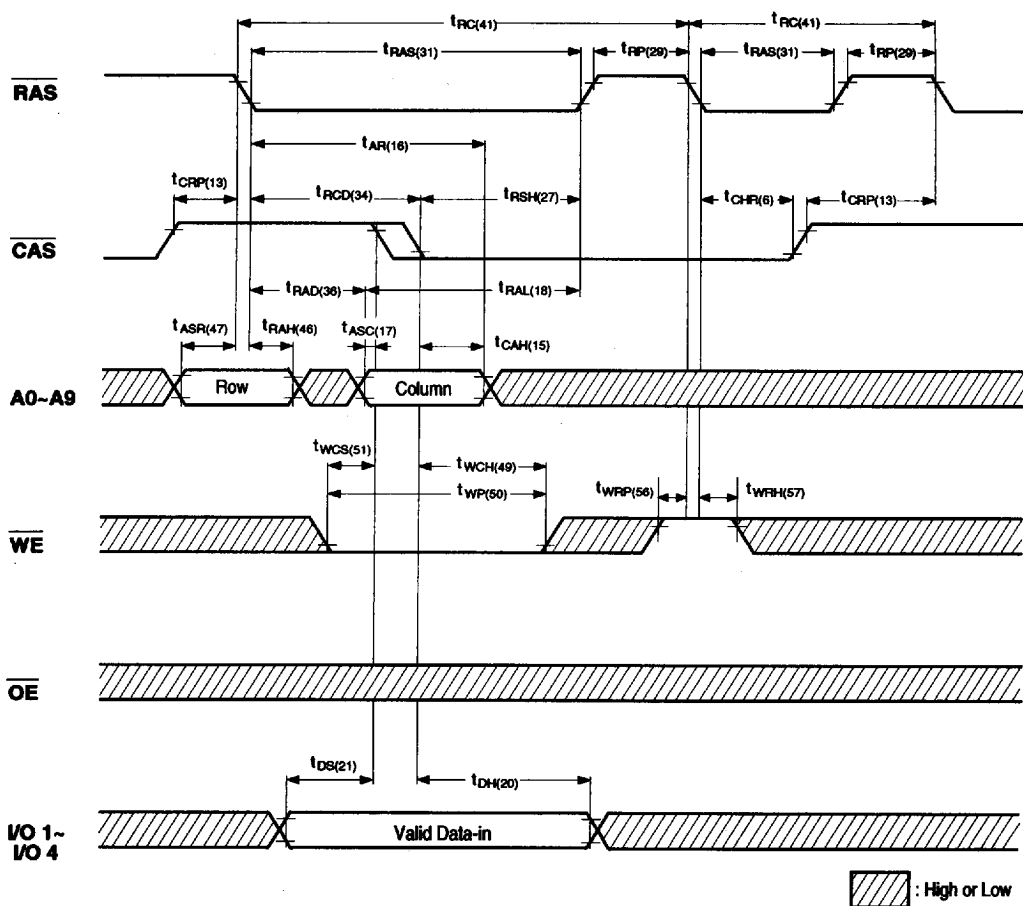
WE must be high at the falling edge of RAS in order to prevent from entering test mode.

HIDDEN REFRESH CYCLE (READ)



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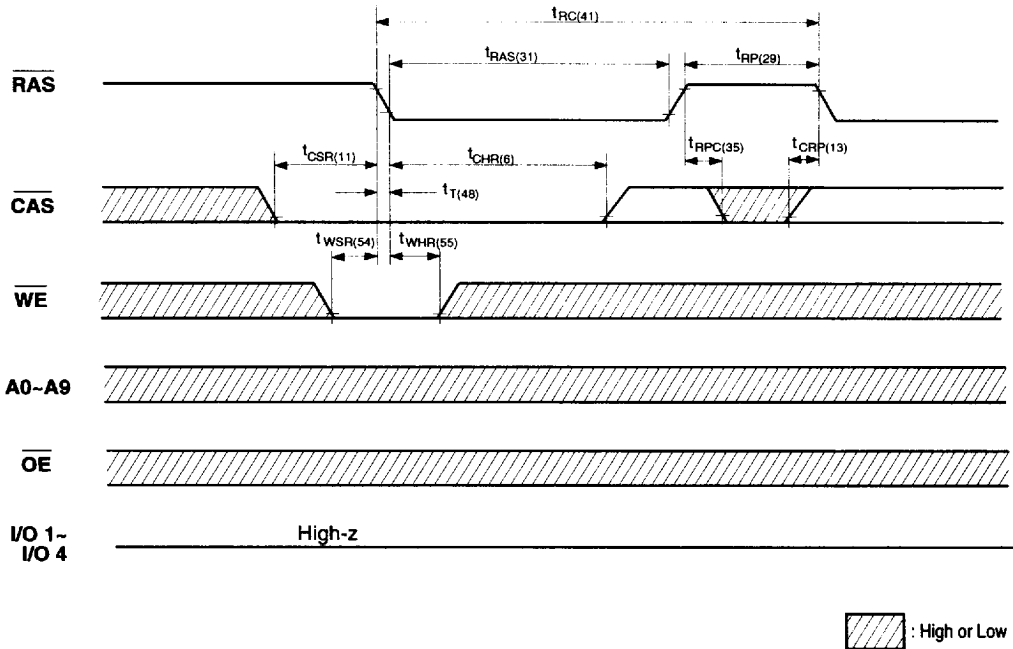
HIDDEN REFRESH CYCLE (EARLY WRITE)



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NPNX

TEST MODE SET CYCLE ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE)



■ The NN51V4400B has an 8 bit parallel Test Mode Function for reducing test time. In the Test Mode, memory configuration is 512K x 8 bits and the column address A0 is ignored.

a. Entering the test mode:

The NN51V4400B test mode is entered by using the test mode set cycle ($\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle).

b. Read/Write operation in test mode:

For Write cycle, data input from each I/O (I/O1~I/O4) is written to 2 bit memory cells (total 8bits) at the same time. During the read cycle, if the 2 bits of data are equal, then a "1" is output from each I/O. If there is a difference in the read data for a given 2 bit pair, a "0" will be output from that I/O.

c. Exiting the test mode:

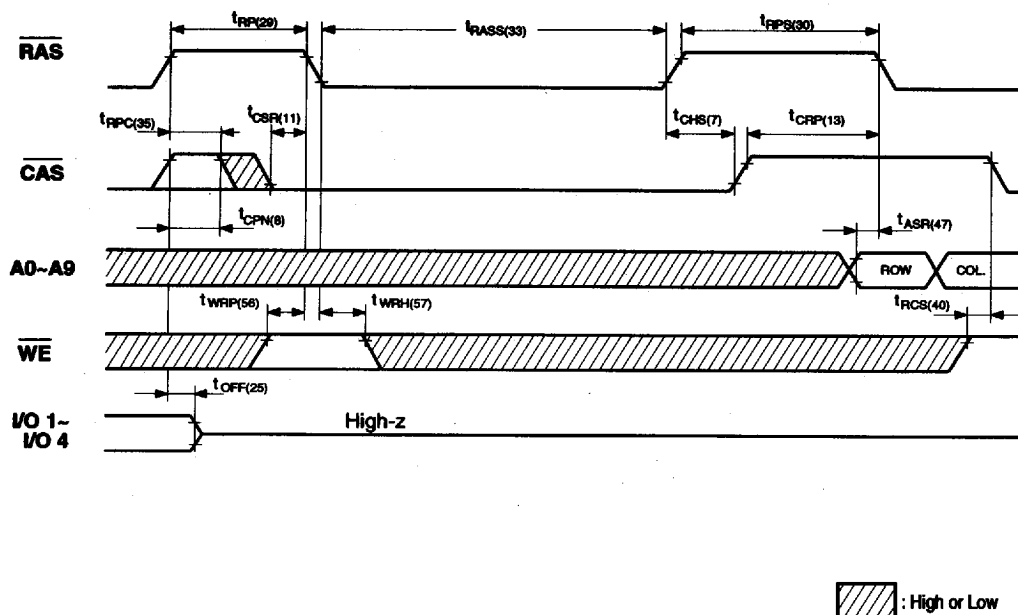
The NN51V4400B will exit the test mode by either a $\overline{\text{RAS}}$ only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle with WE "high".

d. Refresh during test mode:

During test mode refresh must be executed by a normal Read cycle or a $\overline{\text{WE}}$, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

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SELF REFRESH MODE



■ The NN51V4400BL version has a Self Refresh Mode.

a. Entering the Self Refresh Mode:

The NN51V4400BL Self Refresh Mode is entered by using $\overline{CAS}$ before $\overline{RAS}$ cycle with $\overline{WE}$ "high" and holding $\overline{RAS}$ and $\overline{CAS}$ signal "low" longer than 300 μ s.

b. Continuing the Self Refresh Mode:

The Self Refresh Mode is continued by holding $\overline{RAS}$ "low" after entering the Self Refresh Mode.

It does not depend on $\overline{CAS}$ being "high" or "low" after entering the Self Refresh Mode for to continue the Self Refresh Mode.

c. Exiting the Self Refresh Mode:

The NN51V4400BL exits the Self Refresh Mode when the $\overline{RAS}$ signal is brought "high".

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ORDERING INFORMATION

NN51V4400BXX(X) - XX

<u>SPEED</u>	50 : 50ns 60 : 60ns 70 : 70ns
<u>PACKAGE</u>	J : Plastic SOJ TT : Plastic TSOP TYPE II (Normal Bend) RR : Plastic TSOP TYPE II (Reverse Bend)
<u>VERSION</u>	BLANK : Standard Version L : Long Refresh Version 128ms Refresh
<u>DESIGN CODE</u>	B : NN51V4400B series
<u>MODE</u>	4400 : Fast Page 1M x 4
<u>POWER SUPPLY</u>	V : 3.3V Version

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