NATEL

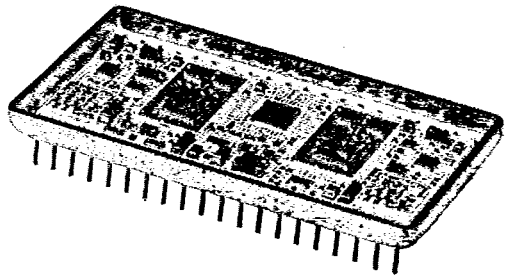
H2SD1626
H2RD1626

2–Speed, Single Hybrid 22–Bit, 0.0004° Accuracy, 5 V-dc Only Synchro(Resolver)-to-Digital Converters Programmable Speed Ratio, µP Compatible

T-71-35-03

Features

- ✓ **0.0004° Accuracy (1.5 Arc-Seconds)** (64:1, and 72:1 speed ratios)
- ✓ **Single 40-Pin TDIP Hybrid**
- ✓ **22-Bit Resolution (0.0001°)**
- ✓ **Programmable Speed Ratio** (8, 9, 16, 18, 32, 36, 64, 72:1)
- • **True Single Supply . . . 5 Volts Only** (prevents ground loop problems)
- ✓ **100 mW Power Dissipation**
- • **Analog Velocity Output** (use as tachometer)
- ✓ **Independent Tracking converters** (selectable fine, coarse, 2-speed outputs)
- • **Reference Synthesizers**
- • **BIT Output (Built-In Test)**
- • **Hi-rel MIL-STD-883B Processing**



ACTUAL SIZE

Applications

Two-speed Synchro/Resolver systems
High-accuracy motion-control systems
Fire-control systems
Avionics systems
Antenna monitoring
Servo systems
Industrial control systems
Simulation
Robotics
Machine tool control systems

Description

The **H2SD1626(H2RD1626)** is the world's first 2–speed hybrid tracking Synchro(Resolver)-to-Digital Converter. It contains two independent Type II servo loop tracking converters in a single 40-pin TDIP along with an advanced, programmable 2–speed combiner. The speed-ratio is pin-programmable by the user for eight (8) standard binary and non-binary ratios. It offers the industry's most advanced features, including operation from a single +5 V-dc only power supply. The **1626** consumes only 100 mW of power, resulting in cool running operation and putting less strain on the users power supply. The bottom line is higher component and system MTBF. Additional standard superior features include Built-In-Test, an anti 180° false lock-up circuit, reference synthesizer, analog velocity output and microprocessor compatibility. The **1626** also offers a high frequency option for higher tracking speed and wider bandwidth.

An anti 180° false lock-up circuit in each converter assures that the **1626** does not get locked into an angle of 180° from the true angle when a step function of 180° is applied.

Transferring data from the 1626 is eased through the use of a transparent latch with three-state outputs configured as a 16-bit word (MSB's) and a 6-bit word (LSB's) available over common 16-bit output lines.

The heart of the **1626** is a custom LSI circuit which functions as a programmable 2–speed combiner and microprocessor interface. This advanced LSI is driven from two independent Type II tracking converters . . . one for the "coarse" input, and one for the "fine" input. Each converter has its own internal reference synthesizer for improved dynamic accuracy by reducing the effects of "speed voltages" at high rotational speeds. The accuracy of the conversion is maintained with signal-to-reference phase shifts of up to ±45°. . . which can easily occur when using 2–speed, multi-pole synchros and resolvers.

Output select control inputs (SEL 0 and SEL 1) are available on the **1626** which can be used to select the desired type of output data. The output data modes are: 2–speed MSB's, 2–speed LSB's, fine-channel angle, course-channel angle. When the 2–speed LSB's are selected, other data is also available on the 16-bit output including BIT and ambiguity error between coarse and fine conversions.

The **1626** is completely self contained with each internal converter having an independent high-accuracy differential signal conditioner for the resolver input and a resistive scott-tee for the synchro input, providing common mode rejection in excess of 70 dB.

Theory of Operation

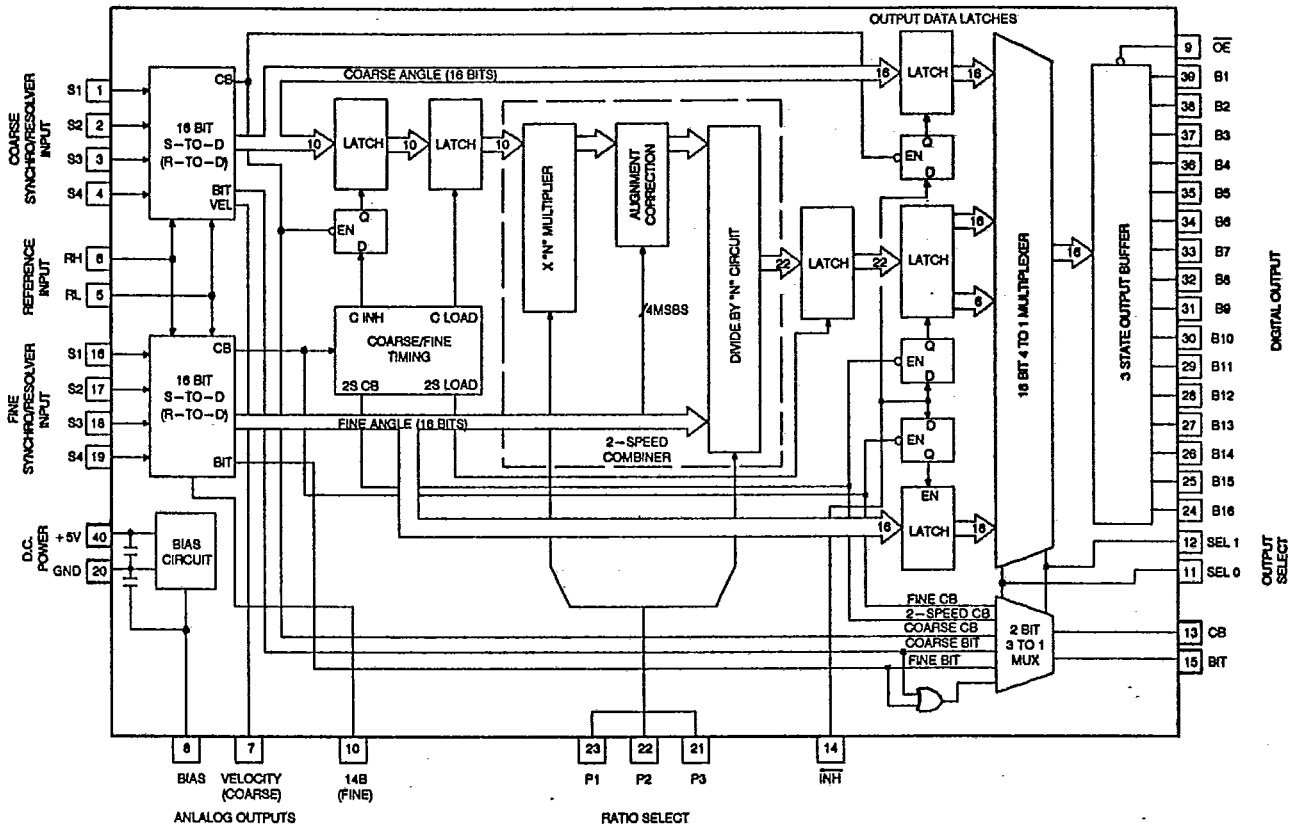


FIGURE 1 1626 Block Diagram

The operation of the **Model 1626** is illustrated in the functional block diagram of Figure 1. The circuit can be divided into the following functional blocks:

1) Coarse 16 bit S(R)-to-D Converter

2) Fine 16 bit S(R)-to-D Converter

3) 2-Speed Combiner

4) Data hold Latches and Timing Circuit

5) Output Multiplexer/Data Selector

6) Bias Circuit

Both "fine" and "coarse" S(R)-to-D converters are continuous tracking, exhibiting zero error for a constant velocity input. Each converter uses a solid-state, balanced differential input which accepts either 3-wire synchro, or 4-wire resolver formats (depending on input option). The digital angle output continuously tracks the analog angle input, regardless the state of the inhibit input (pin 14). An internal converter busy "CB" pulse is produced for each 1 LSB change of angle. Each converter utilizes a "Reference Synthesizer" to correct for signal to reference phase shift of up to ±45°. A built-in-test circuit monitors the status of each fine and coarse converter. The "Fine" converter can be pin-programmed for 14 bit operation, for faster tracking. An analog voltage output is available which is proportional to the velocity of the coarse angle input. For a more detailed description on how each converter operates, please consult Natel Data Sheet on **Model HSD1046(HRD1046).**

The "2-Speed Combiner" circuit is pin programmable for different optional coarse/fine speed ratios "N", where the Fine input rotates "N" revolutions for every single revolution of Coarse input. Ratio "N" can be set to binary ratios of 1x8,1x16,1x32,1x64 or non-binary ratios of 1x9,1x18,1x36 or 1x72. The 10 MSB's of coarse data are multiplied by "N" to obtain coarse data rescaled to a binary multiple of the fine speed digital word. The 4 MSB's of fine speed data are compared with the corresponding bits of rescaled coarse data. If the two do not match, the coarse data is modified to align it with the information contained in the fine data. The corrected coarse data together with 16 bits of fine data represent true angle (times "N"), free of any ambiguity or misalignment error. This data is divided by "N" to obtain a 22-bit digital word whose MSB is 180° and represents the angular position of the coarse shaft of the two-speed system.

The "Output Latches" and "Coarse/Fine Timing" perform the following functions:

- Provides a "glitch-free" digital angle output, regardless of the digital skew times between coarse and fine digital words.
- The digital output bits (B1-B16) change synchronously with each other (no ripple effect).
- Allows the digital output to be "frozen" via the Inhibit ($\overline{INH}$) input control, while the Coarse and Fine converters continuously track the input angle.
- Provides a "2-Speed" Converter Busy (CB) output pulse (corresponding to a 2-speed data increment or decrement transition).

Theory of Operation (continued)

The "Coarse/Fine Timing" circuit also controls the various latch enables in a particular sequence which is repeated for every LSB change of Fine angle data. Since the "fine" angle input of "two speed" systems changes at a greater rate than the "coarse" angle input, the fine converter "CB" is used to initiate a timing sequence. The following sequence of events occurs upon the rising edge of a fine "CB" pulse:

- Coarse angle data is held stable ("C INH")
- Coarse angle data is loaded into the two-speed combiner ("C LOAD")
- A 2-Speed converter busy pulse is generated ("2S CB")
- 22 bit, 2-speed angle data is loaded into an output latch ("2S LOAD")

The total elapsed time of the timing sequence is approximately one micro-second. This timing activity is transparent to external digital I/O activity. Output latches are used on the Coarse, Fine and Two-Speed angle data to provide a means of holding the digital output steady during data transfer, while allowing the converter to continuously track the input angle. Converter busy pulses are available to indicate when corresponding Coarse, Fine or Two-Speed angle data are incrementing (or decrementing) by 1 LSB. The "Two-Speed" digital output resolution will vary depending on the ratio selected (P1,P2,P3) and the fine converter resolution selected (14 or 16 bit) using "14B" input. Each converter busy (CB) is used to gate the $\overline{\text{INH}}$ (inhibit) input to prevent output latch activity during an "internal" angle change transition.

The P1, P2, or P3 programming input will accept a new programmed value only after a fine angle CB pulse is generated.

The "16-bit 4-to-1 Multiplexer" selects the desired angle data, Coarse, Fine, or 2-Speed (using SEL 0 and SEL 1) to be output at the 16-bit bus (B1-B16). The MSB is "B1" (180°) and the LSB is "B16" (.0055°). The "Two-Speed" data is split into two available bytes, (B1-B16) "MSB's" and (B17-B22) "LSBs". Bits B17 through B22 are available at output pins B1 thru B6 respectively, along with other data, such as built-in-test signals (see page 5, table 2) when the lower 2-speed byte is selected. Converter Busy (CB) and Built-In-Test (BIT) digital outputs correspond to the currently selected output data.

All digital inputs ($\overline{\text{OE}}$,P1,P2,P3,$\overline{\text{INH}}$,SEL 0,SEL 1 and 14B) are CMOS type inputs with "TTL" input voltage thresholds (.8 - 2.4 V-dc). Internal "pull-ups" to the +5 V-dc supply (100ua max.) are used on all digital inputs to prevent ambiguous operation when an input is left "floating".

The "Bias Circuit" develops an "internal analog gnd" (bias) of approximately 2.15 V-dc, when the power supply level is at +5 V-dc. The analog "coarse" velocity output is with respect to this "bias" output voltage. Internal power supply decoupling is used on both the +5V and bias voltage pins. The velocity output is an internal analog signal which represents the output angle "rate of change." The "coarse" channel velocity is provided due to its scale factor which does not change with 16- or 14-bit mode. This velocity output can be used in place of a mechanical tachometer in many servo systems, to improve loop response and dynamics.

True Single-Supply 5 V-dc Operation

One of the most outstanding features of the **Model 1626** is the single +5 V-dc power supply requirement. This feature simultaneously eliminates unwanted "ground loop" problems, and results in lower power consumption and correspondingly higher MTBF.

Without the single supply operation, systems that use separate analog and digital grounds for ±15 V-dc and +5 V-dc power, as many systems do, would be faced with potential ground loop problems. The result is usually excess noise on either the analog or digital supplies, which limits the effectiveness of single-point grounding schemes. These ground loops would be present with a converter that used both ±15 V-dc and digital +5 V-dc power because the analog (±15 V-dc) and digital (+5 V-dc) power supplies are referenced to different grounds while multiple supply converters have only a single internal ground. The **1606** takes the agony out of these difficult systems problems by operating entirely within the digital power and ground rails of your system.

All internal circuitry is designed to operate with power supply voltage of as low as 4.5 V-dc. This is made possible by using high signal-to-noise ratio amplifiers and a unique design approach incorporated into a custom LSI chip. No performance specification is sacrificed due to the single 5 V-dc operation.

Operating with a 5 V-dc supply, the converter typically requires only 20 mA of current. This low power operation results in a typical junction-to-ambient (no heat sink) temperature rise of only 4°C!

Built-In-Test (BIT)

A BIT signal (pin 15) provides an over-velocity or fault indication output signal. The error voltage of each converter is monitored continuously, and when the coarse or fine tracking error exceeds approximately 1° (over-velocity or failure), a logic "1" signal is generated to indicate invalid data. Under normal operation the BIT output is at logic "0". Possible conditions that will cause the BIT output to show fault indication are:

- Power-turn-on – BIT output will return to logic "0" when the converter synchronizes to correct coarse and fine input angle ±1°.
- Step-input – instantaneous coarse/fine input changes greater than ±1° until the converter synchronizes
- Over velocity condition
- Excessive shaft angle modulation
- Reference voltage disconnected
- Loss of signal – all signal lines are disconnected
- Converter malfunction – any converter failure which prevents synchronization to the input angle

Note that the BIT output has ≥50% duty cycle logic "1" when reference lines and/or signal lines are disconnected. The cycle frequency is synchronous with the carrier frequency when either the signal or reference (but not both) is missing. When both signal and reference lines are disconnected, the cycle frequency is ≥2 Hz. The BIT signal is a logic "or" function of the BIT on both the internal "fine" and "coarse" converters when "2-speed" data output is selected.

Reference Synthesizer

To maintain the highest accuracy under both static and dynamic conditions, the **1626** utilizes a "reference synthesizer" (one per channel) to correct for a phase difference between the signal and reference inputs of up to ±45°.

Conventional tracking Synchro (Resolver)-to-Digital converters use a phase-sensitive demodulator to detect the phase and amplitude of the error voltage, sin (θ − ϕ). One of the functions of the demodulator is to reject quadrature components in the error signal (e). A phase-sensitive demodulator rejects any quadrature signal (signal 90° out of phase) only if the synchro input and its reference are exactly in phase. Zero degree phase shift between reference and signal inputs is not practical in most applications using Synchro (Resolver)-to-Digital converters. Quadrature signal voltage can result from any of the following:

- dynamic synchro(resolver) "speed voltages," a quadrature signal that is proportional to the shaft rotational speed
- synchro(resolver) "null voltages"
- capacitive coupling between synchro lines
- differential phase shift in synchro/resolver lines

This quadrature voltage will cause angular error as a variable offset if there is a phase difference between input signals and reference. For example for a 60-Hz synchro with a 5° phase shift rotating at 2 rps (720°/sec), the dynamic error due to speed voltage would be 0.17° or 10 arc-minutes!

Natel's **Model 1626** greatly reduces the effects of this error by creating a synthetic reference. The sine and cosine voltages from the signal conditioner are combined to obtain an in-phase internal reference. Together with the external reference voltage (to determine phase) this improved reference is used for demodulating the error voltage.

No 180° False Lock-up

An additional feature of the **Model 1626** eliminates "false 180° digital output readings," during instantaneous 180° input step changes. "180° false lock-up" can occur in most Synchro-to-Digital converters whenever the synchro(resolver) input angle is "electronically switched" or stepped from one angle to another by 180°. This occurrence is most common in applications where the input is being supplied by a Digital-to-Synchro converter and the MSB (180° BIT) is turned "ON" or "OFF". This feature is especially important in two-speed systems, which have traditionally been plagued by false lock-up problems in the past. This has been a problem because of the lower accuracy and resolution of coarse-axis converters and due to the multiple lock-up points possible with the fine-axis converters. The coarse-axis converter typically has been more susceptible to lock-up due to its inherently lower resolution and accuracy. The fine-axis converter on the other hand, while being high resolution and high accuracy, will exhibit many potential lock-up angles depending on the programmed speed ratio. For example, in a 1:72 ratio system, 180° steps on the fine-axis channel occur at 180/72 intervals, or every 2.5 degrees!

With the **Model 1626**, these frustrating system-level problems are completely eliminated. In addition, the user no longer is faced with the burden of having to determine which angles are suitable for test software and which angles have lock-up potential.

Natel's **Model 1626** gets around this problem by continuously monitoring sin θ and cos θ signals and comparing the phase relationship with the digital output angle and reference input (RH, RL). When a 180° input step is applied, the internal BIT-detect circuit is activated, which forces an error in the converter loop to move the digital output angle to the correct reading. As soon as the digital output is properly phased with the shaft angle input, this "intentional error" is removed from the converter loop.

Two-Speed Synchro Conversion

Two-speed synchro systems are utilized in applications where it is necessary to achieve outstanding accuracy, stability, and repeatability. These systems are capable of achieving from one to two orders of magnitude better performance in angular accuracy than single-speed systems. There are two primary types of synchros used in two-speed systems; two speed/multi-pole, and two speed/gear-train. Two-speed multi-pole are the most common for new designs.

A multi-pole synchro(resolver) is similar to a gear-train 2-speed resolver except that the "gear" ratio is done internally using multiple windings.

The basic approach when using a 2-speed synchro system is to utilize a "coarse" and a "fine" resolver coupled to a common shaft (figure 2). For each revolution of the shaft, the synchro output of the coarse synchro changes by 360 electrical degrees. For each revolution of the coarse shaft, the output of the fine synchro changes by N X 360° for a 1:N speed ratio system. Through this approach, the electrical errors in both the fine synchro windings and the S-to-D converter are reduced by a factor of N.

If N = 16, for example, a 4 arc-minute accuracy resolver at a 16:1 ratio to the coarse shaft would exhibit an effective accuracy of 4/16 = 0.25 arc-minutes. Both coarse and fine synchro outputs and converters are needed to accurately keep track of the correct angle throughout the full 360° of rotation.

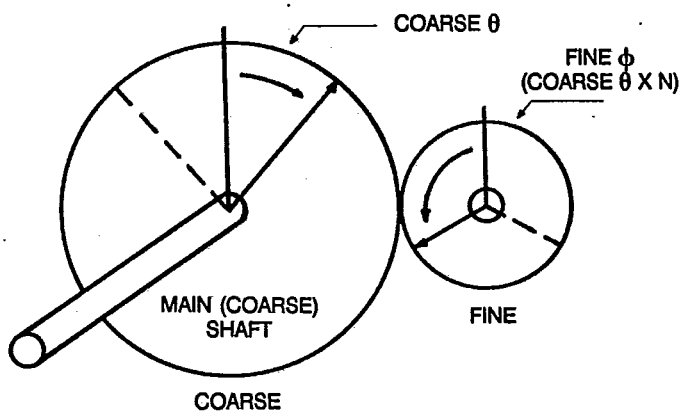


FIGURE 2 Pictorial Diagram of 2-Speed Synchro Operation

The **Model 1626** accurately converts both fine and coarse input angles from the 2-speed synchro (resolver) by continuously converting (independently) each input to digital words representing the equivalent "coarse" and "fine" synchro inputs. This dual conversion method is the most advanced and accurate technique available, resulting in not only versatile operation, but also resulting in fast settling time and a stable, unambiguous output.

Coarse, Fine, 2-Speed Output Select

A versatile feature employed in the **Model 1626** is the ability to select "coarse", "fine", "two-speed", and other data available at the digital output. Some of the possible applications of this feature are:

- Test "Coarse" and "Fine" synchro (resolver) channels independently (for fault isolation)
- Remotely determine Coarse-to-Fine synchro (resolver) shaft alignment
- Monitor "Coarse" and/or "Fine" Built-In-Test signals, via the same digital output data bus.
- Select "Coarse" angle output when slewing at high rates of shaft angle . . . then return to "Two-Speed" angle output when slewing at normal angle slew rates.

The output selected is determined by digital control inputs "SEL 0" and "SEL 1". Both inputs are TTL threshold, CMOS type inputs, with internal pull-ups (100KΩ typical) to the +5Vdc supply. The converter busy (CB) and Built-In-Test (BIT) outputs represent the correspondingly selected fine, coarse or 2-speed data accordingly. The following truth table applies:

TABLE 1
OUTPUT SELECT TRUTH TABLE

CONTROL		OUTPUT SELECTED		
SEL 1	SEL 0	Data Out (B1-B16)	Busy (CB)	Built-In-Test (BIT)
0	0	Fine	Fine CB	Fine BIT
0	1	Coarse	Coarse CB	Coarse BIT
1	0	2-Speed (LSB's)	2-Speed CB	OR'd Coarse and Fine BIT
1	1	2-Speed (MSB's)	2-Speed CB	OR'd Coarse and Fine BIT

16-Bit Output Signals

Table 1 above defines the meaning of digital outputs for the four possible states of the SEL 0 and SEL 1. When "2-Speed LSB's" data out is selected (SEL 0 = 0 and SEL 1 = 1), additional data is available on the same 16-bit byte, as shown in the table below:

TABLE 2
2-SPEED LSB DIGITAL OUTPUT SIGNALS

OUTPUT BIT	DESCRIPTION (SEL 0 = 0, SEL 1 = 1)
B1	2-Speed (Bit 17)
B2	2-Speed (Bit 18)
B3	2-Speed (Bit 19)
B4	2-Speed (Bit 20)
B5	2-Speed (Bit 21)
B6	2-Speed (Bit 22)
B7	(Logic "0")
B8	(Logic "0")
B9	2-Speed Built-In-Test (OR'd coarse and fine)
B10	Coarse Built-In-Test
B11	Fine Built-In-Test
B12	(Coarse-Fine) Alignment Error "Polarity"
B13	(Coarse-Fine) Alignment Error "180° Fine"
B14	(Coarse-Fine) Alignment Error " 90° Fine"
B15	(Coarse-Fine) Alignment Error " 45° Fine"
B16	(Coarse-Fine) Alignment Error "22.5° Fine"

The built-in-test signals are "active high" (fault = logic "1"). The (coarse-fine) alignment error bits with "polarity" indicate shaft alignment between coarse and fine synchros (resolvers). If "polarity" = 1, the alignment error is negative, i.e., the fine angle is greater than the coarse angle. See table 4 (page 13) for more information.

Programmable Speed Ratio

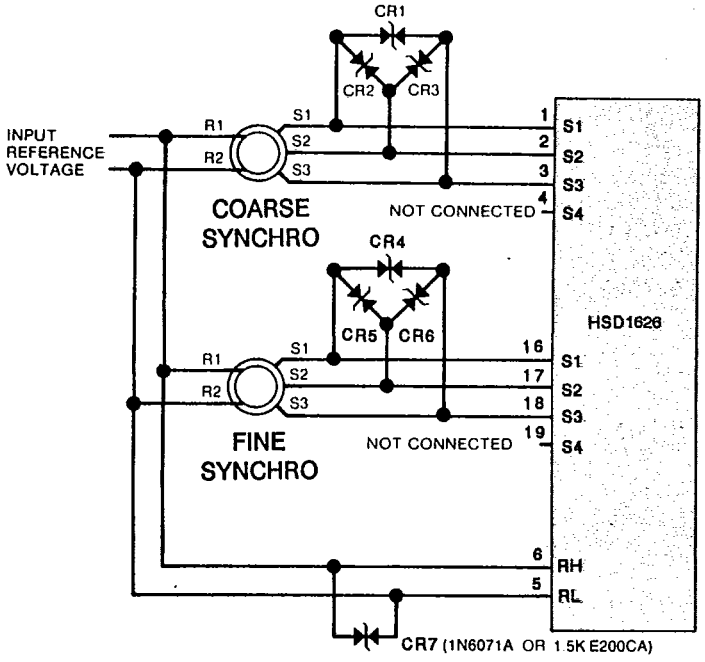
Model 1626 is pin programmable to accept up to eight different coarse-fine speed ratios (x8, x9, x16, x18, x32, x36, x64, x72). This feature allows a single device to work in a variety of applications. The three program pins (P1, P2, P3) are TTL threshold, CMOS type inputs with internal pull-up resistors (100K typical) to the +5Vdc supply. The truth table (table 3) shows the effective "2-Speed" angular output resolution as a function of the selected ratio and "fine" converter resolution select. If the ratio is binary (8, 16, 32, or 64), then some bits will not be active, depending on resolution. For example, if resolution is 17 bits, then B18 – B22 will be at logic "0." If ratio is non-binary all 22 bits will be active.

TABLE 3
2-SPEED DIGITAL OUTPUT RESOLUTION

FINE SELECT RESOLUTION	14B	RATIO SELECT P3	P2	P1	FINE RATIO MULTIPLIER	2-SPEED ANGULAR RESOLUTION
16 BIT	0	0	0	0	X8	2.5 arc-sec (19 bits)
16 BIT	0	0	0	1	X16	1.2 arc-sec (20 bits)
16 BIT	0	0	1	0	X32	0.6 arc-sec (21 bits)
16 BIT	0	0	1	1	X64	0.3 arc-sec (22 bits)
16 BIT	0	1	0	0	X9	2.2 arc-sec (19 bits)
16 BIT	0	1	0	1	X18	1.1 arc-sec (20 bits)
16 BIT	0	1	1	0	X36	0.5 arc-sec (21 bits)
16 BIT	0	1	1	1	X72	0.3 arc-sec (22 bits)
14 BIT	1	0	0	0	X8	9.9 arc-sec (17 bits)
14 BIT	1	0	0	1	X16	4.9 arc-sec (18 bits)
14 BIT	1	0	1	0	X32	2.5 arc-sec (19 bits)
14 BIT	1	0	1	1	X64	1.2 arc-sec (20 bits)
14 BIT	1	1	0	0	X9	8.8 arc-sec (17 bits)
14 BIT	1	1	0	1	X18	4.4 arc-sec (18 bits)
14 BIT	1	1	1	0	X36	2.2 arc-sec (19 bits)
14 BIT	1	1	1	1	X72	1.1 arc-sec (20 bits)

Synchro/Resolver Connections and Phasing

V_{L-L} INPUT	CR1-CR6
11.8 V-rms	1N6049A OR 1.5KE27CA
90 V-rms	1N6070A OR 1.5KE200CA



$$E_{S3-S1} = V_{max} \sin\theta$$
$$E_{S2-S3} = V_{max} \sin(\theta + 120°)$$
$$E_{S1-S2} = V_{max} \sin(\theta + 240°)$$

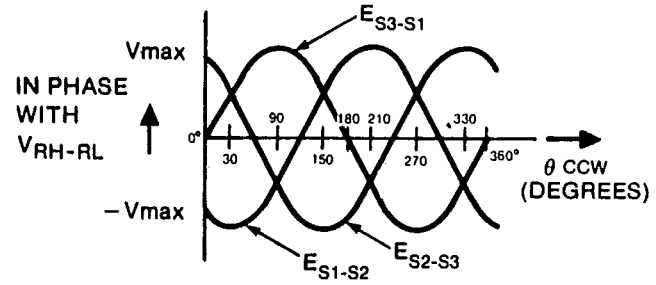
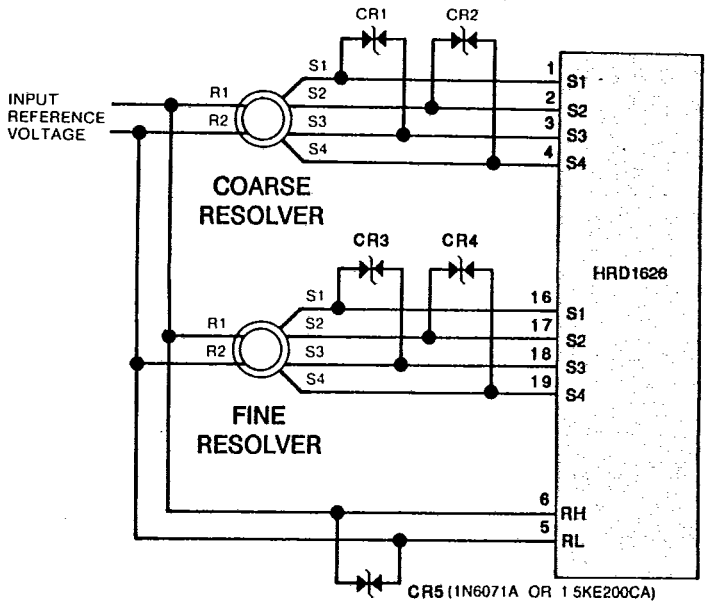


FIGURE 3 Synchro Inputs

V_{L-L} INPUT	CR1-CR4
11.8 V-rms	1N6049A OR 1.5KE27CA
26 V-rms	1N6057A OR 1.5KE56CA
90 V-rms	1N6070A OR 1.5KE200CA



$$E_{S3-S1} = V_{max} \sin\theta$$
$$E_{S2-S4} = V_{max} \cos\theta$$

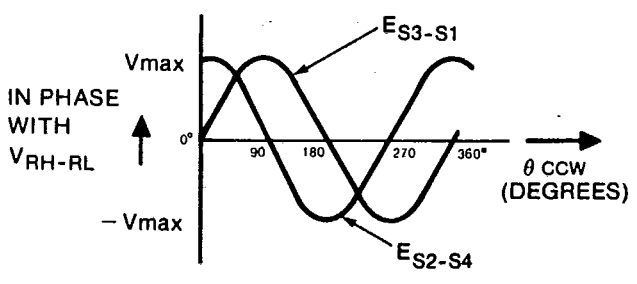


FIGURE 4 Resolver Inputs

The connections for synchro and resolver inputs are shown in Figure 3 and Figure 4. The input signal conditioners use differential amplifiers and matched precision resistors to provide a high common-mode rejection ratio. This eliminates the need for external transformers for most applications. The input signal conditioner performs two functions. For both synchro and resolver format inputs it serves as a precision attenuator reducing the amplitude of high level ac input signals to levels which can be processed by the converter. For a synchro input, this network transforms three wire synchro information into resolver format (sin θ and cos θ).

Both signal and reference inputs are true differential inputs and use precision thin film resistors for signal attenuation.

If input voltages exceed the absolute maximum ratings, the thin-film resistors may be destroyed. To prevent this from happening, it is recommended that transient voltage suppressors be installed on both signal and reference lines. Synchros and resolvers are highly inductive and can generate or couple transients many times greater than their normal signal voltages and can easily exceed the absolute maximum ratings. This situation is particularly likely to occur in cases where the excitation or source voltage for the synchro (resolver) is switched on or off. Transients can also occur by other equipment being turned on or off. Figures 3 and 4 show recommended methods of connecting synchro and resolver inputs. Transient voltage suppressors given in the tables (or equivalent) must be used to assure input protection.

Pin Designations

V_L — Power Supply Voltage
Logic Voltage
5 V-dc ±10%

GND — Power Supply Ground
Digital Ground

B1-B22 — Parallel Output Data Bits –
B1 is MSB = 180 degrees
B16 = 0.0055 degrees
B22 = 0.00009 degrees

S1-S4 (Coarse) — Coarse Input Analog Signals
S4 is NC for synchro input option

S1-S4 (Fine) — Fine Input Analog Signals
S4 is NC for synchro input option

RH, RL — Reference Voltage Input
(Common to both coarse and fine channels)

$\dot{\theta}$ — Velocity Output –
dc analog voltage proportional to rotational speed of the system shaft angle (output is referenced to BIAS voltage)

V — Bias Voltage Output –
Internal "analog gnd" (2.15Vdc typical)
Serves as reference gnd for $\dot{\theta}$ "velocity output"

$\overline{INH}$ — Inhibit Function –
A logic "0" freezes the digital angular output. Both coarse and fine converters keep tracking the analog coarse and fine inputs. For continuous operation, this pin may be left unconnected. (internal 100K ohm typical pull-up to V_L)

CB — Converter Busy –
A 700ns pulse which occurs during updating of the internal data output latches. Output data transitions occur during the middle of the busy pulse. A positive pulse occurs whenever the converter changes by 1 LSB. CB pulses are not inhibited by the application of $\overline{INH}$ or $\overline{OE}$.

BIT — Built-In-Test –
A logic "1" indicates that the output is not tracking the "coarse" and/or "fine" synchro (resolver) analog angle inputs.

$\overline{OE}$ — Output Enable –
"3-State" output enable control for digital output bits (B1-B16). When $\overline{OE}$ is set to logic "0," outputs are enabled (low impedance state). When $\overline{OE}$ is set to logic "1" (or left floating), outputs are disabled (high impedance state).

S1 (Coarse)	1	40	V_L
S2 (Coarse)	2	39	B1 [B17]
S3 (Coarse)	3	38	B2 [B18]
S4 (Coarse)	4	37	B3 [B19]
RL	5	36	B4 [B20]
RH	6	35	B5 [B21]
$\dot{\theta}$	7	34	B6 [B22]
V	8	33	B7
$\overline{OE}$	9	32	B8
14B	10	31	B9
SEL 0	11	30	B10
SEL 1	12	29	B11
CB	13	28	B12
$\overline{INH}$	14	27	B13
BIT	15	26	B14
S1 (Fine)	16	25	B15
S2 (Fine)	17	24	B16
S3 (Fine)	18	23	P1
S4 (Fine)	19	22	P2
GND	20	21	P3

FIGURE 5 H2SD/H2RD1626 Pin Assignments

NOTE: If $\overline{OE}$ is left floating, an internal 100K ohm typical pull-up to V_L (logic "1") will disable the data output bits.

14B — Fine Converter Output Resolution Control –
Selects 14 or 16-bit "fine" converter resolution.
Use 16-Bit (14B = logic "0") for best resolution.
Use 14-Bit (14B = logic "1") for fastest tracking.

NOTE: If 14B is left floating, an internal active pull-up (15µA typical) to V_L will set the fine resolution to 14 bits.

SEL 0, SEL 1 — Output Data Select Controls –
Selects desired data at B1 through B16 to represent "coarse", "fine", "2-Speed MSB", or "2-Speed LSB" angle information, as well as built-in-test and coarse-fine alignment information. See page 5 (table 1) for the Output Select truth table.

P1,P2,P3 — Ratio Select Pins –
Digital inputs select desired fine/coarse angle speed ratio. See page 5 (table 3) for the ratio select truth table.

Absolute Maximum Ratings

Synchro(Resolver) Signal Inputs	Twice Normal Voltage
Reference Input	200 V-rms
Supply Voltage (V_L)	+6.5 V-dc
Digital Inputs	−0.3 V-dc to V_L
Storage Temperature	−65°C to +135°C

When installing or removing the converter from printed circuit boards or sockets, it is recommended that the power supplies and input signals be turned off. Decoupling capacitors are recommended on the power supply V_L. A 1 µF tantalum capacitor in parallel with 0.01 µF ceramic capacitor should be mounted as close to the supply pin (40) as possible.

Specifications

PARAMETER	VALUE	REMARKS	TEST LEVEL
Digital Output Resolution			Note 2
Coarse Converter	16 Bits (0.33 arc-minutes)		
Fine Converter	16 Bits (0.33 arc-minutes)	14B = Logic "0"	
	14 Bits (1.32 arc-minutes)	14B = Logic "1"	
2-Speed Combined Output			
X8	19 Bits (2.5 arc-seconds)	14B = Logic "0" (Fine = 16 bits)	
X16	20 Bits (1.2 arc-seconds)	14B = Logic "0" (Fine = 16 bits)	
X32	21 Bits (0.6 arc-seconds)	14B = Logic "0" (Fine = 16 bits)	
X64	22 Bits (0.3 arc-seconds)	14B = Logic "0" (Fine = 16 bits)	
X9	19 Bits (2.2 arc-seconds)	14B = Logic "0" (Fine = 16 bits)	
X18	20 Bits (1.1 arc-seconds)	14B = Logic "0" (Fine = 16 bits)	
X36	21 Bits (0.5 arc-seconds)	14B = Logic "0" (Fine = 16 bits)	
X72	22 Bits (0.3 arc-seconds)	14B = Logic "0" (Fine = 16 bits)	
X8	17 Bits (9.9 arc-seconds)	14B = Logic "1" (Fine = 14 bits)	
X16	18 Bits (4.9 arc-seconds)	14B = Logic "1" (Fine = 14 bits)	
X32	19 Bits (2.5 arc-seconds)	14B = Logic "1" (Fine = 14 bits)	
X64	20 Bits (1.2 arc-seconds)	14B = Logic "1" (Fine = 14 bits)	
X9	17 Bits (8.8 arc-seconds)	14B = Logic "1" (Fine = 14 bits)	
X18	18 Bits (4.4 arc-seconds)	14B = Logic "1" (Fine = 14 bits)	
X36	19 Bits (2.2 arc-seconds)	14B = Logic "1" (Fine = 14 bits)	
X72	20 Bits (1.1 arc-seconds)	14B = Logic "1" (Fine = 14 bits)	
Angular Accuracy		sec = arc-seconds, min = arc-minutes	Note 1

	Option S	Option H	Option V	
Coarse Converter	6.0 min	6.0 min	6.0 min	Accuracy applies over the full operating temperature range, ±10% frequency variation and includes hysteresis.
Fine Converter (16-Bit)	5.2 min	2.6 min	1.3 min	14B = Logic "0" (Fine = 16 bits)
Fine Converter (14-Bit)	6.5 min	4.0 min	2.6 min	14B = Logic "1" (Fine = 14 bits)
2-Speed Combined Output				
8:1 ratio	40.0 sec	20.0 sec	10.0 sec	14B = Logic "0" (Fine = 16 bits)
16:1 ratio	20.0 sec	10.0 sec	5.0 sec	14B = Logic "0" (Fine = 16 bits)
32:1 ratio	10.0 sec	5.0 sec	2.5 sec	14B = Logic "0" (Fine = 16 bits)
64:1 ratio	5.0 sec	2.5 sec	1.4 sec	14B = Logic "0" (Fine = 16 bits)
9:1 ratio	36.0 sec	18.0 sec	9.0 sec	14B = Logic "0" (Fine = 16 bits)
18:1 ratio	18.0 sec	9.0 sec	4.7 sec	14B = Logic "0" (Fine = 16 bits)
36:1 ratio	9.0 sec	4.7 sec	2.5 sec	14B = Logic "0" (Fine = 16 bits)
72:1 ratio	4.7 sec	2.5 sec	1.4 sec	14B = Logic "0" (Fine = 16 bits)
8:1 ratio	50.0 sec	30.0 sec	20.0 sec	14B = Logic "1" (Fine = 14 bits)
16:1 ratio	25.0 sec	15.0 sec	10.0 sec	14B = Logic "1" (Fine = 14 bits)
32:1 ratio	12.2 sec	7.5 sec	5.0 sec	14B = Logic "1" (Fine = 14 bits)
64:1 ratio	6.1 sec	3.8 sec	2.5 sec	14B = Logic "1" (Fine = 14 bits)
9:1 ratio	44.0 sec	27.0 sec	18.0 sec	14B = Logic "1" (Fine = 14 bits)
18:1 ratio	22.0 sec	13.7 sec	9.0 sec	14B = Logic "1" (Fine = 14 bits)
36:1 ratio	11.2 sec	7.0 sec	4.7 sec	14B = Logic "1" (Fine = 14 bits)
72:1 ratio	5.8 sec	3.7 sec	2.5 sec	14B = Logic "1" (Fine = 14 bits)

Fine/Coarse Ambiguity	±135° Maximum	Fine-channel angle with respect to coarse-channel angle	Note 2
Reference Input			
Voltage	20 to 130 V-rms		Note 2
Frequency	700 to 3000 Hz (Option 8) 360 to 1000 Hz (Option 4) 47 to 1000 Hz (Option 6)	800 Hz Models 400 Hz Models 60Hz Models	Note 3
Input Impedance (minimum)	250 K Ω Single Ended 500 K Ω Differential		Note 2
Common-Mode Range	±250 V peak maximum	dc plus recurrent ac peak	Note 3

Specifications Continued

PARAMETER	VALUE	REMARKS	TEST LEVEL
Synchro/Resolver Inputs			
Input Voltages (line-to-line)	11.8 V-rms (Option 1) 26 V-rms (Option 2) 90 V-rms (Option 9)	Accuracy of the converter is maintained with ±10% variation in signal voltages	Note 1
Input Impedance (minimum)	30K Ω (60 K Ω) minimum 75K Ω (150 K Ω) minimum 250 K Ω (500 K Ω) minimum	Line-to-GND (differential), 11.8 V-rms L-L Models Line-to-GND (differential), 26V-rms L-L Models Line-to-GND (differential), 90V-rms L-L Models	Note 2
Impedance Unbalance	0.2% maximum (differential)	For all Models	Note 3
Common-Mode Range	± 25V peak ± 55V peak ±180V peak	11.8 V-rms Models 26 V-rms Models 90 V-rms Models	Note 3
Common-Mode Rejection	70 dB minimum	dc to 1000 Hz	Note 3
Harmonic Distortion	10% maximum	Without degradation in accuracy specification	Note 3
Reference Synthesizer		**Both fine and coarse channels**	
Phase-shift allowed between Input signals and Input reference	±45° guaranteed ±65° typical	Without any degradation of converter accuracy	Note 2
Digital Inputs		**CMOS transient protected**	
$\overline{OE}$	Logic "1" Logic "0"	16 output bits (B1 – B16) are in the high impedance state of 3 state output 16 output bits (B1 – B16) are enabled	Note 1
$\overline{INH}$	Logic "1" Logic "0"	Digital output follows analog input signal Output data latched in holding register (does not interrupt converter tracking loop)	Note 1
14B	Logic "1" Logic "0"	14-bit resolution (fine channel) 16-bit resolution (fine channel)	Note 1
Output Selected	**SEL 1** / **SEL 0**		Note 1
Fine digital angle	0 / 0	B1-B16 = fine channel data CB = fine channel CB BIT = fine channel BIT	
Coarse digital angle	0 / 1	B1-B16 = coarse channel data CB = coarse channel CB BIT = coarse channel BIT	
2-Speed (up to 6) LSB's	1 / 0	B1-B6 (B17-B22) = 2-speed LSB's (See Table 2) CB = 2-speed CB BIT = OR'd coarse/fine BIT	
2-Speed 16 MSB's	1 / 1	B1-B16 = 2-speed MSB's CB = 2-speed CB BIT = OR'd coarse/fine BIT	
Ratio Selected	**P3** / **P2** / **P1**	Pin-programmed (See Table 3) Change in programming recognized after next fine-converter CB pulse	Note 1
8:1	0 / 0 / 0		
16:1	0 / 0 / 1		
32:1	0 / 1 / 0		
64:1	0 / 1 / 1		
9:1	1 / 0 / 0		
18:1	1 / 0 / 1		
36:1	1 / 1 / 0		
72:1	1 / 1 / 1		
Voltage Levels Logic "0" Logic "1"	-0.3 V-dc to 0.8 V-dc 2.4 V-dc to 5.0 V-dc	For V_L = 5 V-dc	Note 2

Specifications Continued

PARAMETER	VALUE	REMARKS	TEST LEVEL
Input Currents			
$\overline{OE}$, SEL 0, SEL 1, $\overline{INH}$ P1, P2, P3	100 K Ω (typical) pull up to the power supply (V_L)	When not used, may be left unconnected	Note 3
14B	15 μA typical, 30 μA max. active pull up to the power supply (V_L)		Note 3
Digital Outputs		**CMOS Outputs**	
Data Bits (B1-B22)	Natural Binary Angle	Positive logic	
CB	Logic "0" Logic "1"	Internal converter at steady state Internal converter LSB update (700 ns typical) (See Figure 6 for timing)	Note 1
BIT	Logic "0" Logic "1"	"Selected" digital output is valid (±1 degree) Fault condition for "selected" digital out.	Note 1
Drive Capability Data Bits (B1-B22), CB , BIT	2 standard TTL minimum	For V_L = 4.5 V-dc, over full temp range	Note 3
Logic "0" sink current Logic "1" source current	3.2 mA (min) @ 0.40 V-dc -3.2 mA (min) @ 3.0 V-dc	See Figure 11 for typical drive currents	Note 3
HI-Z Output Leakage Data Bits (B1-B22)	±10 μA maximum	Output capacitance = approximately 5 pF	Note 3
Analog Outputs	**Typical, unless specified**		
V (Bias Voltage)	1/2 (V_L-0.7) ±10%	2.15 V-dc ±10% for 5 V-dc supply	Note 3
Drive Capability	± 1 mA minimum		Note 3
$\dot{\theta}$ **Velocity Output (Coarse)**	**Typical, unless specified**	**dc voltage referenced to V (bias)**	
Polarity	Negative for increasing angle		Note 3
Scale Factor (Gain) @ 25°C	0.835 mV/deg/sec typical 1.22 mV/deg/sec typical 6.11 mV/deg/sec typical	800 Hz Models 400 Hz Models 60 Hz Models	Note 2
Temperature Coefficient	±500 PPM/°C typical		Note 3
Power Supply Dependence	-1% per percent maximum		
Full Scale Output @ 25°C	1.5 V-dc @ 1800°/sec typical 1.1 V-dc @ 900°/sec typical 1.1 V-dc @ 180°/sec typical	800 Hz Models 400 Hz Models 60Hz Models	
Linearity @ 25°C	± 5% of full scale maximum ± 2% of full scale maximum ± 1% of full scale maximum	800 Hz Models 400 Hz Models 60Hz Models	Note 2
Temperature Coefficient	± 200 PPM/°C typical		Note 3
Power Supply Dependence	0.1% per percent typical		
Output Noise Static Input	3 mV-rms typical	All Models	Note 3
Maximum tracking rate	15 (30) mV-rms typical	For 800, 400, (60) Hz Models	Note 3
Output Offset @ 25°C	± 5mV-dc typical ± 20mV-dc maximum	All Models	Note 2
Temperature Coefficient	± 30 μV/°C typical		Note 3
Power Supply Dependence	± 20 μV per percent typical		
Δ Gain vs. Polarity	10% maximum	All Models	Note 2
Temperature Coefficient Power Supply Dependence	± 200 PPM/°C typical 0.1% per percent typical		Note 3

Specifications Continued

PARAMETER	VALUE	REMARKS	TEST LEVEL
Dynamic Characteristics	**Typical, unless specified**	**For coarse channel, use (16-) bit values**	
Velocity Constant (K_V)	∞	Type II servo loop	Note 3
Tracking Rate (minimum)	7200 (1800) °/sec 3600 (900) °/sec 720 (180) °/sec	800 Hz Models, for 14- (16-) bit mode 400 Hz Models, for 14- (16-) bit mode 60 Hz Models, for 14- (16-) bit mode	Note 1
Maximum Acceleration (typical)	1,600,000 (400,000) °/sec^2 400,000 (100,000) °/sec^2 16,000 (4,000) °/sec^2	800 Hz Models, for 14- (16-) bit mode 400 Hz Models, for 14- (16-) bit mode 60 Hz Models, for 14- (16-) bit mode	Note 3
Acceleration Constant (nominal)	768,000 (192,000) /sec^2 192,000 (48,000) /sec^2 7,680 (1,920) /sec^2	800 Hz Models, for 14- (16-) bit mode 400 Hz Models, for 14- (16-) bit mode 60 Hz Models, for 14- (16-) bit mode	Note 3
Acceleration for 1 LSB error (LSB = 0.0055°/16-bit) (LSB = 0.022°/14-bit)	16,875 (1,055) °/sec^2 typical 4,219 (264) °/sec^2 typical 169 (11) °/sec^2 typical	800 Hz Models, for 14- (16-) bit mode 400 Hz Models, for 14- (16-) bit mode 60 Hz Models, for 14- (16-) bit mode	Note 3
Settling time to 1 LSB (for 179° step change)	50 (150) ms maximum 100 (300) ms maximum 450 (1,350) ms maximum	800 Hz Models, for 14- (16-) bit mode 400 Hz Models, for 14- (16-) bit mode 60 Hz Models, for 14- (16-) bit mode	Note 2
Settling time to 1 LSB (small signal step < 1.4°)	8 (25) ms maximum 16 (50) ms maximum 100 (250) ms maximum	800 Hz Models, for 14- (16-) bit mode 400 Hz Models, for 14- (16-) bit mode 60 Hz Models, for 14- (16-) bit mode	Note 2
Converter Bandwidth	400 (200) Hz typical 200 (100) Hz typical 40 (20) Hz typical	800 Hz Models, for 14- (16-) bit mode 400 Hz Models, for 14- (16-) bit mode 60 Hz Models, for 14- (16-) bit mode	Note 3
Power Supply			
Voltage	5 V-dc ±10%	Without degradation in accuracy specification	Note 3
Current	60 mA typical, 90 mA maximum 20 mA typical, 40 mA maximum	800 Hz Models 400, 60 Hz Models	Note 1
Thermal Characteristics			
Junction Temperature Rise Above Case	2°C typical, 4°C maximum 10°C maximum (800 Hz Models)	For component with highest temperature rise	Note 3
Case Temperature Rise Above Ambient	4°C typical, 8°C maximum 16°C maximum (800 Hz Models)	Without any heat sink	Note 3
Power Dissipation	100 mW typical, 200 mW maximum 450 mW maximum (800 Hz Models)	For V_L = 5 V-dc	Note 3
Physical Characteristics			
Type	40-pin Hermetic Triple Dip		
Size	1.14 X 2.14 X 0.23 inch (29 X 54.4 X 5.9 mm)	3 Standoffs are added to the package to insulate it from the printed circuit board traces (Standoffs included in 0.23 inch height dimension)	Note 3
Weight	0.9 oz (26 g) maximum		Note 3

NOTE 1: Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, this key parameter is 100% tested.

NOTE 2: Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level in the range of one to five percent.

NOTE 3 Compliance of each component to this specification is 100% guaranteed by Natel. To assure compliance, AQL levels are verified using a lot sample level of less than one percent. Note 3 parameters are maximum design limits.

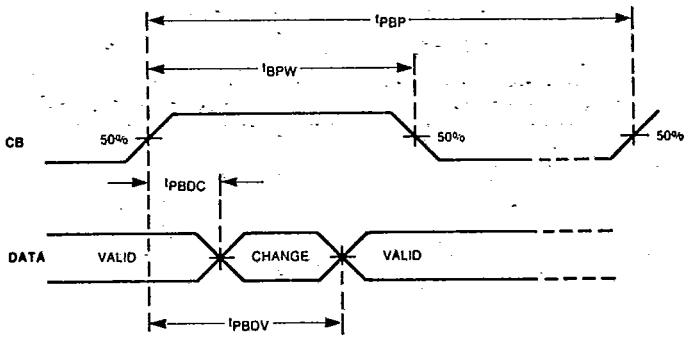
If your application requires 100% testing of any additional parameters of this specification or requires non-standard input or output characteristics, please contact a Natel Applications Engineer or the Sales Department.

Data Transfer

R_L = 200 KΩ Input t_r t_f = 20 ns V_L = 5 V-dc C_L = 50 pF

(Specifications apply over full operating temperature range)

CHARACTERISTIC	LIMITS			UNITS	FIG.
	MIN	TYP	MAX		
Busy Pulse Width (t_{BPW})	0.4	0.7	1.2	μs	6
Busy Period (t_{PBP})	2.0	Note 1	Inf	μs	6
Busy to Data Change (t_{PBDC})	100	350	–	ns	6
Busy to Data Valid (t_{PBDV})	–	350	600	ns	6
Inhibit to Data Stable (t_{PIDS})	0	400	700	ns	7, 8
Inhibit to Data Update (t_{PIDU})	10	–		ns	7, 8
Inhibit Update Pulse Width (t_{IPW})	1.3	0.7	–	μs	8
3-State High Z to Low Z (t_{PHZL})	3	10	30	ns	9
3-State Low Z to High Z (t_{PLZH})	3	10	30	ns	9
Output Select Time (t_{MUX})	–	15	40	ns	10
Output Transition Time (10%-90%) (B1-B16), CB, BIT	–	6	20	ns	–



NOTE 1: Busy Period (t_{PBP}) = $\frac{K \cdot 10^6}{2^N \cdot R}$ (μs)

For Reference:

Busy Frequency = $\frac{2^N \cdot R}{K}$ (Hz)

Rate (R) = $\frac{K \cdot \text{Busy Frequency}}{2^N}$

Where,

N = Converter Resolution (14 or 16)

K = 360 (For Degrees) or = 2π (For Radians)

and

R = Rate (Degrees / Second) or = Rate (Radians / Second)

FIGURE 6 Converter Busy and Data Timing

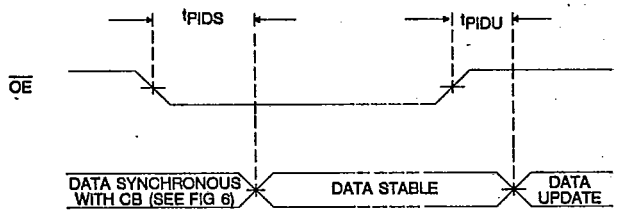


FIGURE 7 Inhibiting Output Data Update

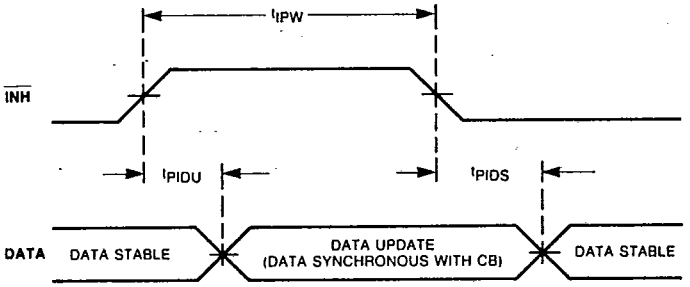


FIGURE 8 Enabling Output Data Update

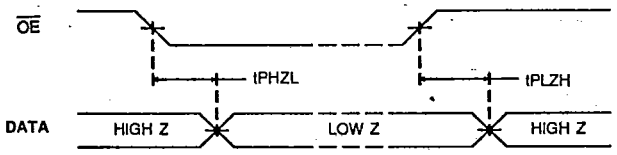


FIGURE 9 3-State Output Timing

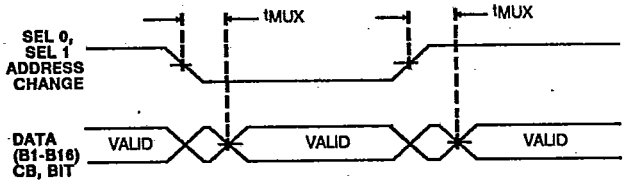


FIGURE 10 Output Select Time

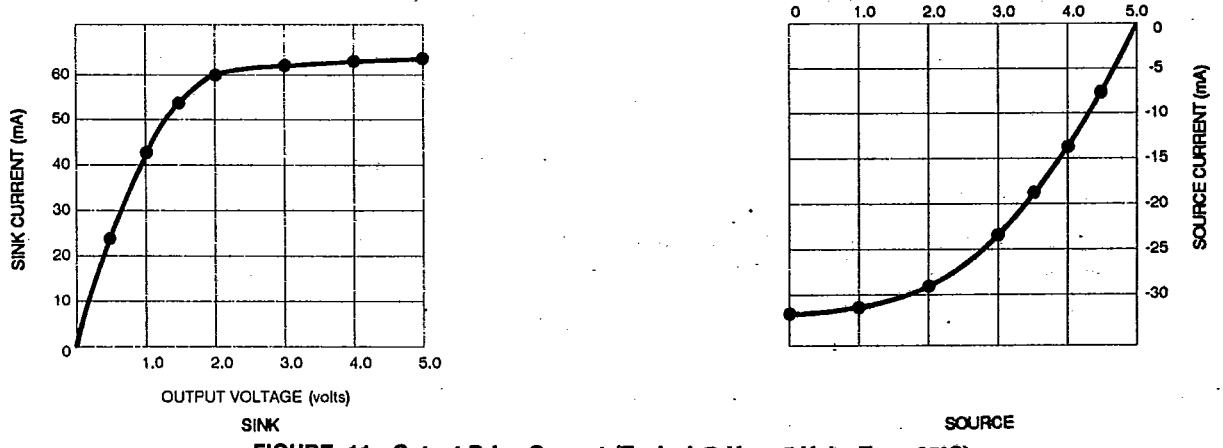


FIGURE 11 Output Drive Current (Typical @ V_L = 5 V-dc, Ta = 25°C)

Coarse / Fine Synchro Alignment

Model 1626 will correct for coarse-to-fine synchro(resolver) shaft misalignment of up to 135 degrees of fine or 135/RATIO degrees of coarse angle (see table 4).

This range is so wide that coarse/fine shaft alignment tolerances can literally be ignored in the system design. For applications in which the user may want to check alignment, the digital output "alignment error" bits are available as part of the "2-Speed LSB" data byte word (see table 2). B13 is the MSB, equivalent to 180° of Fine shaft alignment error. For proper alignment, the reading should be 0 ±135° (or 360 ±135°) = 225° to 360° or 0° to 135°. See table 4 for a summary of the alignment bits and the corresponding coarse-fine shaft misalignment.

If polarity (B12) = 0, then alignment is positive and the coarse angle is greater than the fine angle.

If polarity (B12) = 1, then alignment is negative, and the coarse angle is less than the fine angle.

NOTE: This table is valid for SEL 0 = 0 and SEL 1 = 1. The shaded area indicates poor alignment which will result in two-speed angular output error.

TABLE 4. Alignment Error Data Table

POLARITY BIT12	180° BIT13	90° BIT14	45° BIT15	22.5° BIT16	ALIGNMENT ERROR (° of fine rotation)
see note	0	0	0	0	0
	0	0	0	1	22.5
	0	0	1	0	45
	0	0	1	1	67.5
	0	1	0	0	90
	0	1	0	1	112.5
	0	1	1	0	135
	0	1	1	1	157.5
	1	0	0	0	180
	1	0	0	1	202.5
	1	0	1	0	225
	1	0	1	1	247.5
	1	1	0	0	270
	1	1	0	1	292.5
	1	1	1	0	315
	1	1	1	1	337.5

Testing 2-Speed Synchro(Resolver)-to-Digital Converters

Model 1626 testing is most effectively accomplished through the use of a computer interface to the digital I/O of the hybrid since there are four possible modes to the digital outputs. For added testing ease and flexibility, the Natel L200 IEEE-488 programmable dynamic angle synchro(resolver) simulator should be used. A block diagram of the recommended test set-up for **Model 1626** is shown in figure 12.

The coarse-channel L200 is set for internal reference operation and drives the reference voltage into the RL and RH inputs of the **1626**, and also into the external reference input of the 2nd L200. The 2nd (fine-channel) L200 is configured for "slave" operation by selecting "external" reference input.

When checking "2-speed" data, prior to reading output, always change the fine angle after a coarse angle change is made.

The independent fine-and coarse-channel tracking converters are checked by setting SEL 0 = 0 and SEL 1 = 0 for fine-channel angle or by setting SEL 0 = 1 and SEL 1 = 0 for the coarse-channel. The two-speed digital angle is checked by first reading the 16 MSBs (SEL 0 = 1, SEL 1 = 1) and then the 6 LSBs (SEL 0 = 0, SEL 1 = 1) and combining them in software using the following algorithm:

Read 2-speed MSBs (M)	Input data
Read 2-speed LSBs (L)	Input data
Mask lower 10 bits of (L) = (L')	Separate angular data from other bits
Scale LSBs (L') by dividing by 65,536	$(L'/2^{16})$
Combine MSBs and LSBs (A)	$= (M) + (L'/2^{16})$
Convert into desired format	BCD, Hexidecimal, ETC.

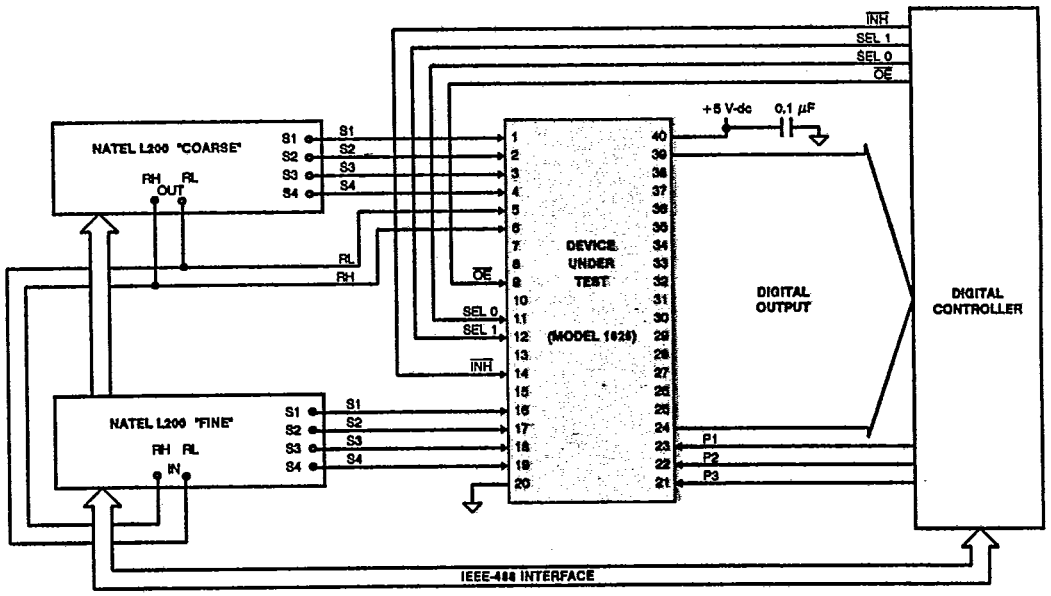


FIGURE 12 Model 1626 Test Setup

Data Transfer

Due to the nature of the Type II servo conversion mechanism incorporated in the 1626, the output data angle always tracks the synchro(resolver) input shaft angle within the converter's rated maximum tracking rate (angular velocity) and bandwidth. Both "coarse" and "fine" input angles are continuously converted (independently) to digital words representing the equivalent "coarse", "fine" or "combined 2-speed" angle. The desired digital angle is output at B1-B16 using the address select lines "SEL 0" and "SEL 1" (the appropriate CB and BIT is also selected). See Table 1 and 2 on Page 5.

Theoretically, for every 0.0055° of "coarse" or "fine" input angle change there will be a corresponding "coarse" or "fine" data output change of one LSB (both converters are 16 bit when "14B" control input is at logic "0" . . . fine channel is 14 bit when "14B" is at logic "1"). When a "fine" data output change occurs, the "combined 2-speed" output data will also change accordingly (fine/ratio). Note that a "coarse" data change alone (without fine data change) will NOT change the "combined 2-speed" output data. Additionally, a change in the "ratio select" control inputs (P1, P2, P3) will NOT change the "combined 2-speed" output data until a "fine" data output change of at least 1 LSB occurs.

To prevent reading data during an output change or transition, the following methods of data transfer can be used.

1) Synchronous transfer with shaft angle change.

   Use CB (Converter Busy) pulse to clock data into an external register. Use the falling edge of CB as an edge triggered clock. (Rising edge of CB could be used but data would have an additional error of ±1 LSB.) Data changes within 600 ns after the rising edge of the CB pulse.

2) Asynchronous transfer with shaft angle change (using $\overline{INH}$).

   The simplest method of data transfer (which is completely independent of input shaft angle change) is to use the inhibit ($\overline{INH}$) function to hold or freeze the current data output angle. Set the $\overline{INH}$ input to logic "0" . . . wait a minimum of 700 ns . . . transfer the data . . . return $\overline{INH}$ to logic "1" for a minimum of 1.3 µs. This method of asynchronous data transfer from the 1626 is shown in Figure 13.

It should be noted that the $\overline{INH}$ control does not affect the conversion process . . . it only affects the transparent output latches. If the synchro (resolver) angle input changes while an inhibit is applied ($\overline{INH}$ = "0"), the internal S(R)-to-D will still track the input. Fresh output data (B1-B16) will be available within 1.3 µs after the $\overline{INH}$ input returns to logic "1" (uninhibit), regardless of the previous $\overline{INH}$ logic "0" duration.

Note: The CB output (Converter Busy) will always produce a pulse for every LSB of internal S(R)-to-D angle change, regardless the state of the $\overline{INH}$ (inhibit) input.

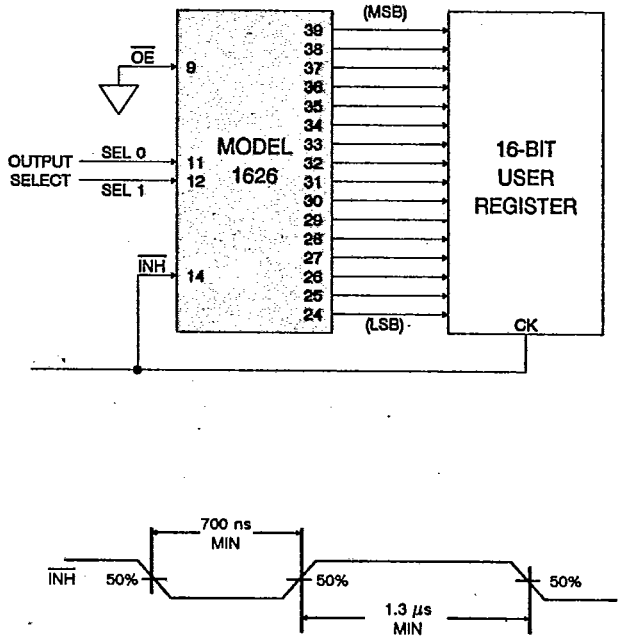


FIGURE 13 Asynchronous Data Transfer

Single-Byte Data Transfer on 16-Bit Data Bus

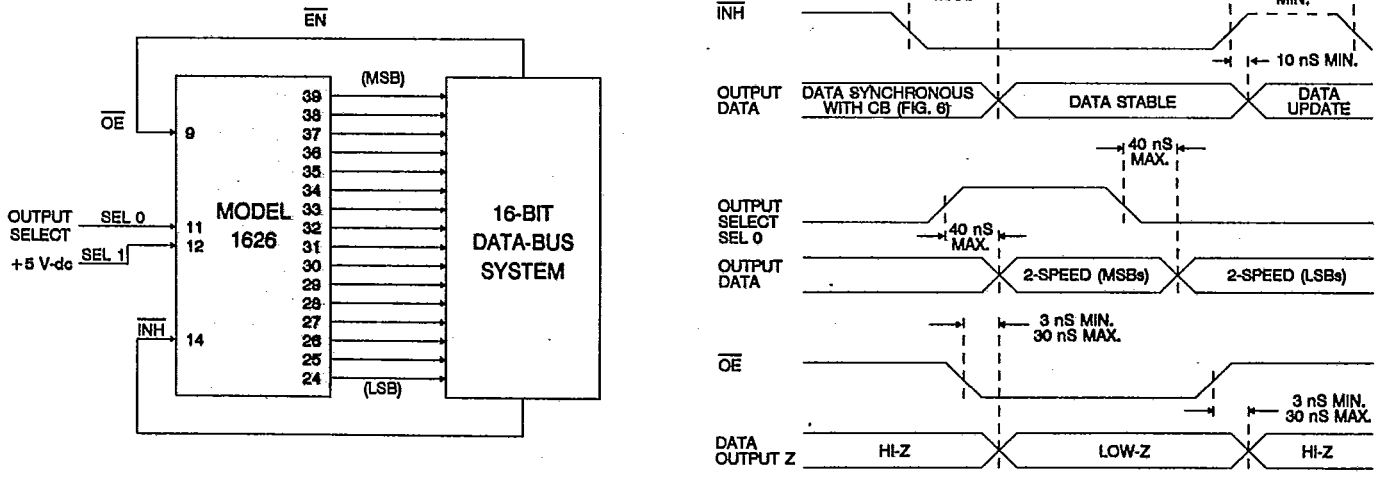


FIGURE 14 Digital Connections and Timing for Single-Byte Data Transfer

The circuit configuration and timing diagram for transferring data from the **Model 1626** to a 16-bit 3-state data-bus system is shown in Figure 14. A typical sequence of events would be as follows:

1) Apply the $\overline{INH}$ input for a minimum of 700 ns before transferring valid data.
2) Set SEL 0 (Output Select) to logic "1" (2-speed MSBs) for a minimum of 40 ns before transferring valid data.
3) Set $\overline{OE}$ (3-state enable) to logic "0" for a minimum of 30 ns before transferring valid data.
4) Transfer 2-speed MSB Data.
5) Set SEL 0 to logic "0" (2-speed LSBs) for a minimum of 40 ns before transferring valid data.
6) Transfer 2-speed LSB Data.
7) Return $\overline{OE}$ to logic "1" at least 30 ns before the next device is put on the data bus.
8) Return $\overline{INH}$ to logic "1" no earlier than 10 ns before valid data is transferred. The $\overline{INH}$ input may remain at logic "0" indefinitely . . . but must return to logic "1" for a minimum of 1.3 µs to allow update of fresh accurate output data.

Notes:

- $\overline{INH}$ and SEL 0, SEL 1 input functions are independent from $\overline{OE}$ (3-state) inputs.
- The CB output (Converter Busy) will always produce a pulse for every LSB of converter angle change, regardless of the state of the $\overline{INH}$ input or $\overline{OE}$ inputs.
- Converter "Ouput Selection" (SEL 0, SEL 1) can be done in any sequence with repect to $\overline{INH}$ and $\overline{OE}$ controls.

Two-Byte Data Transfer on 8-Bit Data Bus

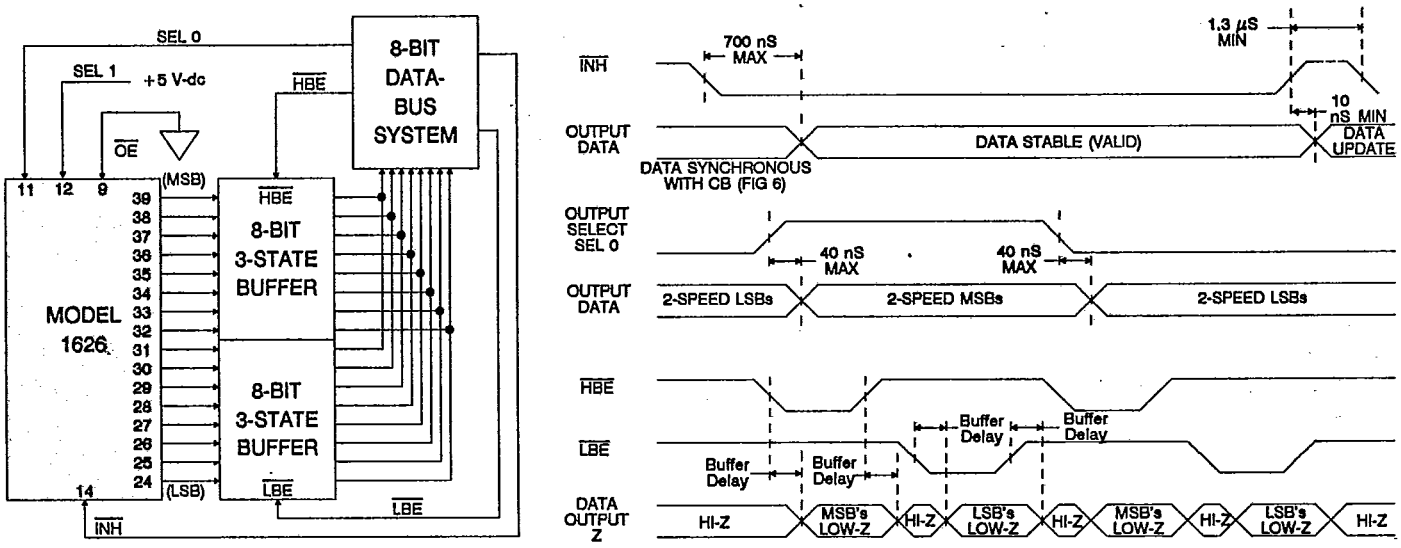


FIGURE 15 Digital Connections And Timing For Two-byte Data Transfer

The circuit configuration and timing diagram for transferring data from **Model 1626** to an 8-bit 3-state data-bus system is shown in Figure 15. A typical sequence of events would be as follows:

1) Apply the $\overline{INH}$ input for a minimum of 700 ns before transferring valid data.
2) Set SEL 0 (Output Select) to logic "1" (2-speed MSBs) for a minimum of 40 ns plus buffer delay before transferring data.
3) Set $\overline{HBE}$ (high-byte-enable) to logic "0" for a minimum of that required by the 3-state buffer before transferring valid data (MSB's).
4) Transfer MSB's.
5) Return $\overline{HBE}$ to logic "1".
6) Set $\overline{LBE}$ (low-byte-enable) to logic "0" for a minimum of that required by the 3-state buffer before transferring valid data (LSB's).
7) Transfer LSB's.
8) Return $\overline{LBE}$ to logic "1".
9) Set SEL 0 to logic "0" (2-speed LSBs) for a minimum of 40 ns plus buffer delay before transferring data.
10) Repeat steps 3 through 8.
11) Return $\overline{INH}$ to logic "1" no earlier than 10 ns before valid data is transferred. The $\overline{INH}$ input may remain at logic "0" indefinitely . . . but must return to logic "1" for a minimum of 1.3 µs to allow update of fresh accurate output data.

Notes:

$\overline{HBE}$ and $\overline{LBE}$ data bytes can be transferred in any sequence ($\overline{HBE}$ or $\overline{LBE}$ first).

$\overline{INH}$ and SEL 0, SEL 1 input functions are independent from $\overline{OE}$ (3-state) input.

The CB output (Converter Busy) will always produce a pulse for every LSB of converter angle change, regardless of the state of the $\overline{INH}$ input or $\overline{OE}$ input.

Converter "Output Selection" (SEL 0, SEL 1) can be done in any sequence with respect to $\overline{INH}$ and $\overline{OE}$ controls (selection of 2-speed MSB's, 2-speed LSB's, coarse or fine data).

Converter Tracking in 2-Speed Systems

In 2-speed synchro(resolver) systems, the tracking rate of each (coarse, fine) converter is specified with respect to the electrical angle presented to the signal inputs. Therefore, when determining the effect on the fine converter channel in the **1626**, either the specified converter tracking rate must be reduced by the "speed" ratio to determine the effective tracking rate on the main (coarse) shaft; or the effective shaft speed presented to the fine-channel converter must be increased by the "speed ratio" to compare it to the fine converter tracking rate.

Example:

Coarse (main) shaft speed = 100°/sec. maximum.
Speed Ratio (N) = 16:1

therefore,

Effective fine channel tracking rate = 100 x 16 = 1600°/sec and, from pages 8, and 11, **Model 1626**, 800 Hz version can be used in the 16-bit mode, with maximum tracking rate of 1800°/second and a highest available accuracy of 5.0 arc-seconds.

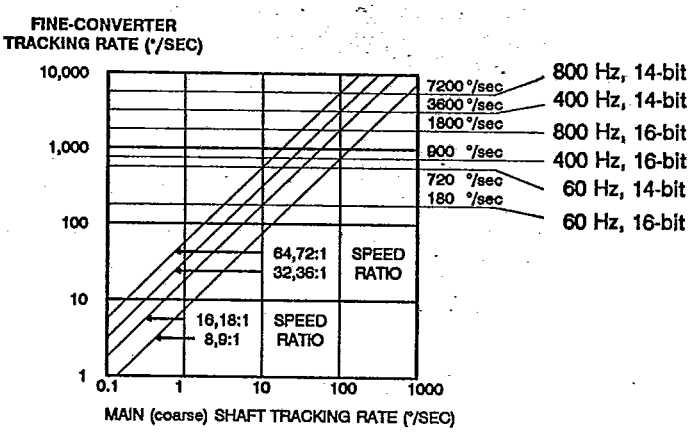


FIGURE 16 Fine Converter Tracking Rate

Alternatively, For this example, The **Model 1626**, 400 Hz version can also be used in the 14-bit mode, with maximum tracking rate of 3600°/second and highest-available accuracy of 10.0 arc-seconds.

Figure 16 shows the relationship between tracking rate, speed ratio, and required fine converter tracking rate.

Velocity Output

As a by-product of the conversion process, the **Model 1626** produces an analog velocity signal. This signal has proven useful in various applications and is therefore brought out. This analog signal is biased with respect to the **Model 1626's** internal analog ground (V).

- V (pin 8), Internal analog ground (Bias)
- $\dot{\theta}$ (pin 7), velocity output coarse channel

The system velocity signal is brought out from the internal coarse converter channel in the **1626**. Therefore, it's scale factor is independent of the "speed ratio" and the 14B resolution-programming input.

$\dot{\theta}$ is a dc voltage proportional to the velocity of the digital output angle (thereby the input shaft angle). The voltage goes negative for increasing digital angle and goes positive for decreasing digital angle.

At maximum tracking velocity, the output voltage is 1.1 volts-dc (1.5 volts-dc for 800 Hz model). Detailed specification for the velocity function is provided on page 10. Dynamic characteristics including open loop and closed loop transfer functions are provided on the following pages.

"V," internal analog ground, also referred to as the "bias voltage" provides a reference point for all analog functions. The typical value of the bias voltage, V, is:

$V = 1/2\ (V_L - 0.7\ \text{V-dc})$

$= 2.15\ \text{V-dc} \pm 10\%\ (\text{for } V_L = +5\ \text{V-dc})$

The $\dot{\theta}$ has a minimum output drive of ±1 mA. For a power supply of +5 V-dc, the minimum output swing is ±1.1 V peak (±1.5 V peak for 800 Hz model) with respect to V (bias).

If a bipolar signal, with respect to power supply ground, is required for the velocity, a difference circuit, as shown in Figure 17, may be used. The output can be scaled to a desired value by selecting the gain of the circuit. Also if reverse polarity output is desirable, the bias and signal connections to the difference amplifier should be reversed.

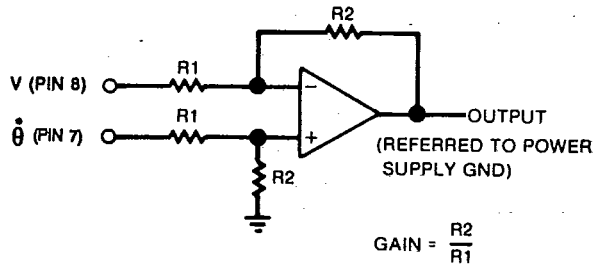


FIGURE 17 Difference Circuit for Bipolar Analog Outputs

For improved velocity signal characteristics (lower ripple and noise), a lower-frequency model (i.e. 60 Hz) can be used at a higher carrier frequency (i.e. 400 Hz). In this situation, tracking rate and dynamic performance will be the same as that specified for the 60 Hz model.

Dynamic Performance

HSD/HRD1626 incorporates a high gain, Type II, servo loop to provide accurate real-time Synchro (Resolver)-to-Digital conversion. Both fine and coarse converters are characterized for the following dynamic input angle conditions:

(1) Static Input Angle

(2) Constant Rate of Change of Input Angle Position (Constant Velocity)

(3) Constant Rate of Change of Input Angular Velocity (Constant Acceleration)

(4) Variable Rate of Change of Angular Velocity (Sinusoidal Modulation)

(5) Infinite Rate of Change of Angular Velocity (Step Input)

The **1626** accuracy specification applies for **Static (1)** and **Constant Velocity (2)** input conditions, as long as the maximum converter tracking rate is not exceeded.

For **Constant Acceleration (3)** of input angle, the digital output will lag the input by the following amount:

$$\text{Acceleration Lag (error)} = \frac{\text{Input Angle Acceleration}}{K_A}$$

The values of maximum tracking rate and acceleration constant (K_A) for different frequency options are given in the specification table (page 11). Note that the specified K_A is typical and is not a tightly controlled parameter (converter K_A is analogous to the open-loop gain of an operational amplifier).

For **Sinusoidal Shaft Angle Modulation (4)**, the digital angle output will lag the input by the following amount:

$$\text{Sinusoidal lag (error p-p)} = \frac{2 \times \pi^2 \times \text{Amp (p-p)} \times Fo^2}{K_A}$$

Where: Amp (p-p) = peak-peak angle modulation level
Fo = modulation frequency (Hz)
K_A = converter acceleration constant

The Peak Rate (Velocity) for a given sinusoidal modulation is:

Rate (degrees/sec) = π x Amp (degrees p-p) x Fo (Hz)

For **Step Inputs (5)**, the digital angle output will respond as a function of the converter's Large Signal and Small Signal transient response.

The **Large Signal** transient response is dependent solely on the maximum velocity (ω_{max}) and the maximum acceleration (α_{max}) of which the converter is capable. The large signal parameters are defined in Figure 18. The synchronizing time (t_{SYNC}) for large signals can be partitioned into three distinct intervals. Acceleration time (t_{ACC}) Slew time (t_{SLEW}) and Overshoot time (t_{OS}).

Acceleration time is the time interval from application of the step-input to the point at which the converter reaches its maximum velocity.

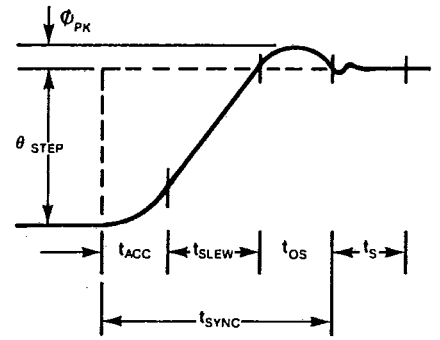
Slew time is the time interval from the point at which maximum velocity is obtained to the point at which the output angle is first equal to the input angle.

Overshoot time is the time interval from the point at which the converter output angle first equals the input angle (and applies constant acceleration in the opposite direction) to the point at which the output angle again reaches the input angle.

At the end of overshoot time, the small signal response becomes dominant and the converter will settle to the final value according to its small signal transient response function.

The Small Signal settling time (t_S) is specified for step inputs of less than 1.4° (coarse or fine). For small signal steps, the settling time is a function of the transient response of the converter.

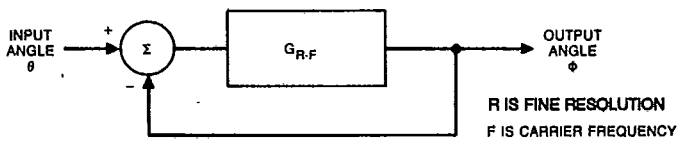
Since the **1626** is a two speed converter, the dynamics of the fine-channel will dominate the overall conversion dynamic response, since it rotates faster (by the speed ratio) than the coarse channel. For example, a step of 5° on the main (coarse) axis (which would not actually occur in practice due to inertia) is equivalent to a 180° step on the fine-channel if the speed ratio is 36:1.



$$\theta \text{ PK} = \frac{\omega^2 \text{ max}}{2\,\alpha \text{ max}}$$

$$t \text{ SYNC} = \frac{\theta \text{ STEP}}{\omega \text{ max}} + \frac{5}{2} \cdot \frac{\omega \text{ max}}{\alpha \text{ max}}$$

FIGURE 18 Large Signal (≥ 1.4°) Response Parameters



$$G_{14\text{-}60} = \frac{7{,}680\,(1+\frac{s}{20})}{s^2\,(1+\frac{s}{200})} \qquad G_{14\text{-}400} = \frac{192{,}000\,(1+\frac{s}{100})}{s^2\,(1+\frac{s}{1000})} \qquad G_{14\text{-}800} = \frac{768{,}000\,(1+\frac{s}{200})}{s^2\,(1+\frac{s}{2000})}$$

$$G_{16\text{-}60} = \frac{1{,}920\,(1+\frac{s}{20})}{s^3\,(1+\frac{s}{200})} \qquad G_{16\text{-}400} = \frac{48{,}000\,(1+\frac{s}{100})}{s^3\,(1+\frac{s}{1000})} \qquad G_{16\text{-}800} = \frac{192{,}000\,(1+\frac{s}{200})}{s^3\,(1+\frac{s}{2000})}$$

FIGURE 19 Transfer Functions for 1626

Transfer Function

The basic control loop model and transfer functions for 60-Hz, 400-Hz and 800-Hz models for coarse and fine converters are shown in Figure 19. A more detailed model with corresponding transfer functions for both position and velocity output is shown in Figure 20. Typical values for transfer function parameters for different frequency options are shown in Table 5.

Transfer function parameters are determined by the specified frequency option of the converter. When a converter is operated at a frequency higher than that specified, these parameters remain the same. For some applications it may be advantageous to use a lower bandwidth converter operating at a higher carrier frequency.

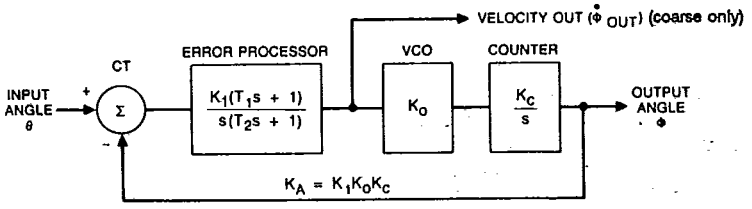
For example, to improve the position noise rejection, velocity output noise/ripple and velocity linearity, a 60-Hz frequency (option 6) could be used and operated at higher carrier frequencies such as 400-Hz.

For a better understanding of the dynamics of the **1626**, bode plots for converter gain and output phase for 60-Hz, 400-Hz and 800-Hz options are shown in Figures 21 and 22.

Results of actual performance of step responses for both large and small signal inputs performed on typical converters are shown in Figure 23.

TABLE 5. Transfer Function Parameters (Typical Values)

PARAMETER	UNITS	FREQUENCY OPTION					
		60 Hz		400 Hz		800 Hz	
		16-BIT	14-BIT	16-BIT	14-BIT	16-BIT	14-BIT
K_A	sec^{-2}	1,920	7,680	48,000	192,000	192,000	768,000
K_O	$\frac{Counts}{Volt \cdot Sec}$	29,800	29,800	149,000	149,000	218,000	218,000
K_C	$\frac{Radians}{Count}$	9.587×10^{-5}	3.835×10^{-4}	9.587×10^{-5}	3.835×10^{-4}	9.587×10^{-5}	3.835×10^{-4}
K_1	$\frac{Volts}{Radian}$	672	672	3360	3360	9187	9187
T_1	ms	50.0	50.0	10.0	10.0	5.0	5.0
T_2	ms	5.0	5.0	1.0	1.0	0.5	0.5
K_OK_C	$\frac{Radians}{Volt \cdot Sec}$	2.857	11.43	14.28	57.14	20.90	83.60



POSITION GAIN (OPEN LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{K_A(T_1s + 1)}{s^2(T_2s + 1)}$

VELOCITY GAIN (OPEN LOOP) $\frac{\dot{\Phi}_{OUT}}{\theta_{IN}} = \frac{K_1(T_1s + 1)}{s(T_2s + 1)}$

POSITION GAIN (CLOSED LOOP) $\frac{\Phi_{OUT}}{\theta_{IN}} = \frac{T_1s + 1}{\frac{T_2s^3}{K_A} + \frac{s^2}{K_A} + T_1s + 1}$

VELOCITY GAIN (CLOSED LOOP) $\frac{\dot{\Phi}_{OUT}}{\theta_{IN}} = \frac{T_1s^2 + s}{\frac{T_2s^3}{K_1} + \frac{s^2}{K_1} + T_1K_OK_Cs + K_OK_C}$

FIGURE 20 Detailed Transfer Function Model for Coarse and Fine Converters

Bode Plots

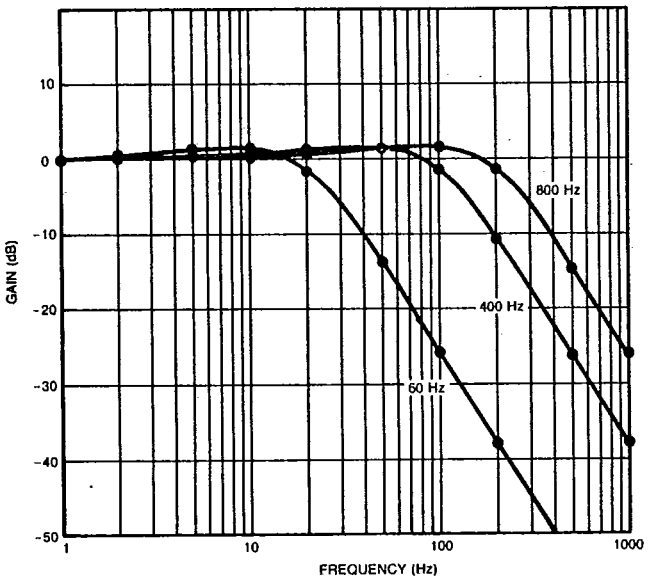


FIGURE 21 Gain Plot (16-bit Mode)

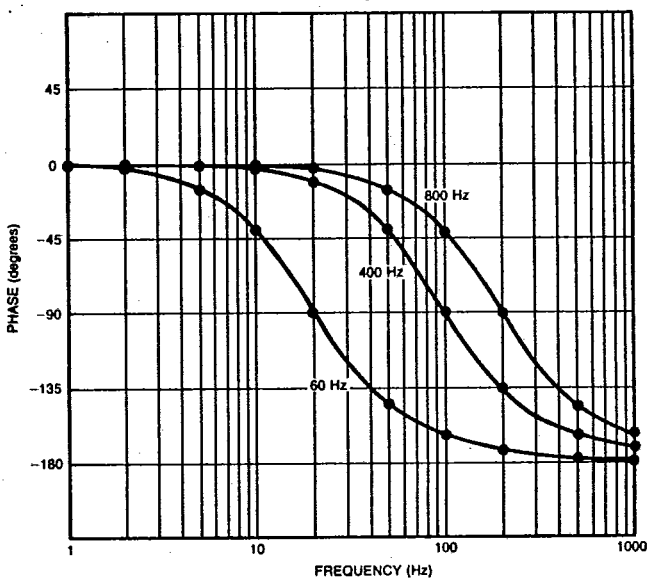
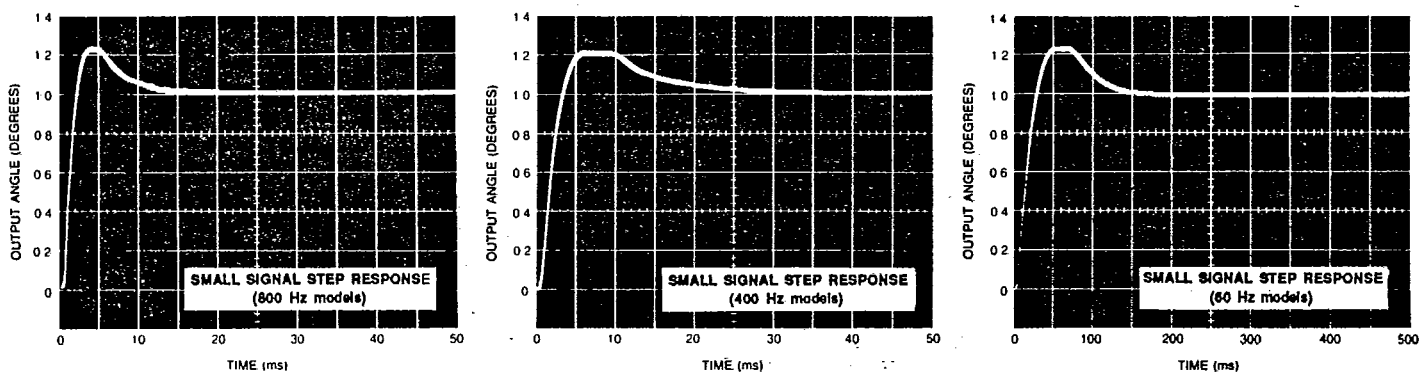


FIGURE 22 Phase Plot (16-bit Mode)

Step Response

V_L = +5 V-dc, T_a = 25°C

Small Signal Input Step = 1.0 Degree



Large Signal Input Step = 179 Degree

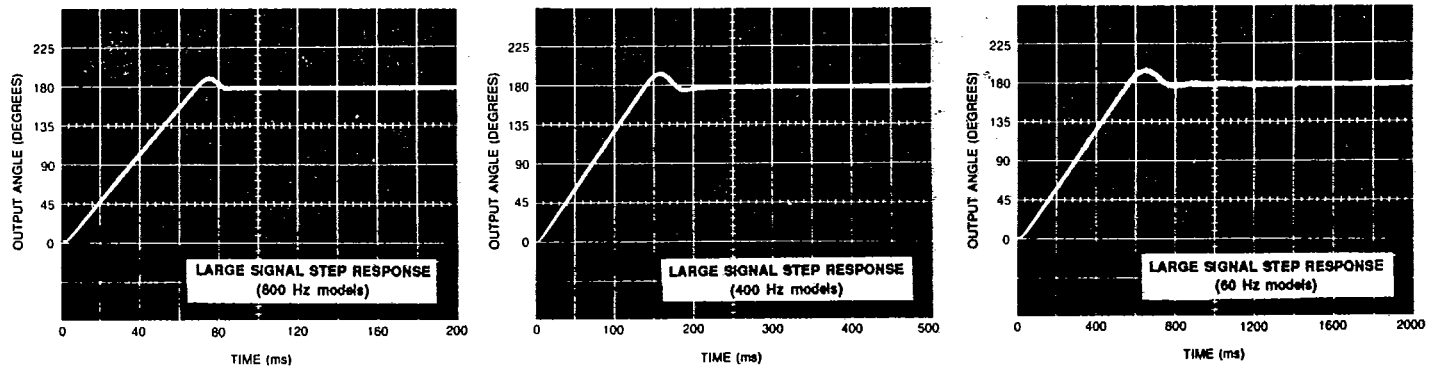
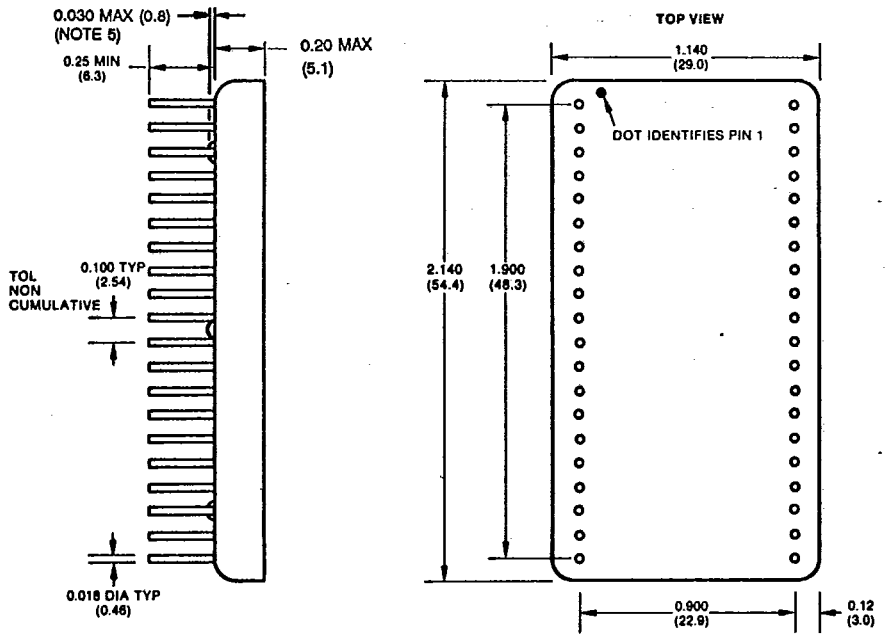


FIGURE 23 Small Signal and Large Signal Step Response (Coarse or Fine – 16-bit Mode)



TOLERANCES:
.XX = ±.01 (±.25)
.XXX = ±.005 (±.13)

NOTES:
1. CASE IS ELECTRICALLY FLOATING.
2. PINS ARE KOVAR WITH GOLD PLATING: (50 µINCH MIN.)
3. PACKAGE IS KOVAR WITH ELECTROLESS NICKEL PLATING.
4. DIMENSIONS SHOWN IN INCHES AND (MM).
5. STANDOFFS (3) CERAMIC OR GLASS.

MECHANICAL OUTLINE (40 PIN TRIPLE DIP)

Ordering Information

H2SD1626 – T F I A

Temperature Range
1 = 0°C to + 70°C
2 = −25°C to + 85°C
3 = −55°C to +125°C

Frequency
4 = 400 Hz
6 = 60 Hz
8 = 800 Hz

Fine-Channel Accuracy*
S = ±5.2 arc-minutes
H = ±2.6 arc-minutes
V = ±1.3 arc-minutes

Input Signal
1 = 11.8 V-rms
2 = 26 V-rms
9 = 90 V-rms
0 = Ext. Signal XFMRS
5 = Ext. Signal and Reference XFMRS

SPECIFY **H2RD1626** FOR RESOLVER INPUT

*2-speed accuracy is specified on page 8 of data sheet (to 0.0004°)

As a standard practice, all converters are built in accordance with requirements of MIL-STD-883B, including 160 hours of active burn-in.

Other products available from NATEL

- **3 arc-second accurate,** Programmable Dynamic Angle Simulator that includes 4 Related Instruments and is totally A.T.E. Programmable (L200).
- Hybrid (36-pin DDIP size) Synchro(Resolver)-to-Digital converters that operate from a **single +5V power supply** and offer excellent features such as BIT, AGC, low power dissipation and more (Models 1006, 1056, 1046 and 1044).
- 1.3 arc-minute accuracy, high power, Digital-to-Synchro converters that **do not require any DC power supplies** (Models 5031 and 5131).
- Second generation Four Quadrant Multiplying Sin/Cos DAC (HDSC2026).
- **2-channel** Digital-to-Sin/Cos Converter in a single 36-pin hybrid (HDSC2036)
- **2-channel** Synchro(Resolver)-to-Digital Converter in a single 40-pin TDIP (HRD/HSD1606).
- Resolver Control Differential Transmitter in a single 36-pin package (HCDX3106).

A wide range of applications assistance is available from Natel. Application notes can be requested when available . . . and Natel's applications engineers are at your disposal for solving specific problems.

TEL: (805) 581-3950

NATEL ENGINEERING CO., INC.
4550 RUNWAY STREET • SIMI VALLEY, CA 93063-3493
TWX: (910) 494-1959 FAX: (805) 584-4357