# NNR1 DIE
# N-Channel JFET Dual Monolithic

Siliconix incorporated

T-31-27

The NNR is a high-performance monolithic dual JFET features extremely low noise, tight offset voltage and drift over temperature specifications. It is targeted for use in a wide range of precision instrumentation applications. Die are supplied with 100% visual sort to the criteria of MIL-STD-750C, Method 2072.

For additional design information please consult the typical performance curves NNR.

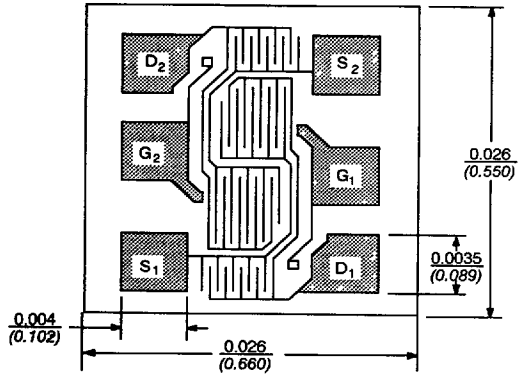
| NNR1CHP* |
|---|
| U404<br>U405<br>U406 |
| *Meets or exceeds specification for all part numbers listed below |

## DESIGNED FOR:

- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

## FEATURES

- Minimum System Error and Calibration
  15 mV Offset (U404)
  100 dB Typical CMRR
- Low Drift with Temperature
  25 μV/°C (U404)
- Simplifies Amplifier Design
  Output Conductance < 2 μS




Back of Chip is Substrate

Nominal Thickness
0.009 inches
0.228 mm

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C Unless Otherwise Noted)

| PARAMETERS/TEST CONDITIONS | SYMBOL | LIMITS | UNITS |
|---|---|---|---|
| Gate-Drain Voltage | $V_{GD}$ | -50 | V |
| Gate-Source Voltage | $V_{GS}$ | -50 | |
| Gate Current | $I_G$ | 10 | mA |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | -55 to 150 | °C |

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| SPECIFICATIONS[a] | | | LIMITS | | | |
|---|---|---|---|---|---|---|
| PARAMETER | SYMBOL | TEST CONDITIONS | TYP[b] | MIN | MAX | UNIT |
| **STATIC** | | | | | | |
| Gate-Source Breakdown Voltage | $V_{(BR)GSS}$ | $I_G$ = −1 µA, $V_{DS}$ = 0 V | −58 | −50 | | V |
| | $V_{(BR)G1-G2}$ | $I_G$ = ±1 µA, $V_{DS}$ = 0 V, $V_{GS}$ = 0 V | −58 | ±50 | | |
| Gate-Source Cutoff Voltage | $V_{GS(OFF)}$ | $V_{DS}$ = 15 V, $I_D$ = 1 nA | −1.5 | −0.5 | −2.5 | |
| Saturation Drain Current[c] | $I_{DSS}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V | 3.5 | 0.5 | 10 | mA |
| Gate Reverse Current | $I_{GSS}$ | $V_{GS}$ = −30 V, $V_{DS}$ = 0 V | −2 | | | pA |
| | | $T_A$ = 125°C | −1 | | | nA |
| Gate Operating Current | $I_G$ | $V_{DG}$ = 15 V, $I_D$ = 200 µA | −2 | | | pA |
| | | $T_A$ = 125°C | −0.8 | | | nA |
| Drain-Source On-Resistance | $r_{DS(ON)}$ | $V_{GS}$ = 0 V, $I_D$ = 0.1 mA | 250 | | | Ω |
| Gate-Source Voltage | $V_{GS}$ | $V_{DG}$ = 15 V, $I_D$ = 200 µA | −1 | | | V |
| Gate-Source Forward Voltage | $V_{GS(F)}$ | $V_{DS}$ = 0 V, $I_G$ = 1 mA | 0.7 | | | |
| **DYNAMIC** | | | | | | |
| Common-Source Forward Transconductance | $g_{fs}$ | $V_{DG}$ = 15 V, $I_D$ = 200 µA, f = 1 kHz | 1.5 | | | mS |
| Common-Source Output Conductance | $g_{os}$ | | 1.3 | | | µS |
| Common-Source Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 kHz | 4 | | | mS |
| Common-Source Output Conductance | $g_{os}$ | | 5 | | | µS |
| Common-Source Input Capacitance | $C_{iss}$ | $V_{DG}$ = 15 V, $I_D$ = 200 µA, f = 1 MHz | 4 | | | pF |
| Common-Source Reverse Transfer Capacitance | $C_{rss}$ | | 1.5 | | | |
| Equivalent Input Noise Voltage | $\bar{e}_n$ | $V_{DG}$ = 15 V, $I_D$ = 200 µA f = 10 Hz | 10 | | | $nV/\sqrt{Hz}$ |
| **MATCHING** | | | | | | |
| Differential Gate-Source Voltage | $\lvert V_{GS1} - V_{GS2} \rvert$ | $I_D$ = 200 µA, $V_{DG}$ = 10 V | 7 | | 15 | mV |
| Gate-Source Voltage Differential Change with Temperature | $\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$ | $I_D$ = 200 µA, $V_{DG}$ = 10 V, T = −55 to 25°C | 10 | | | µV/°C |
| | | T = 25 to 125°C | 10 | | | |
| Common Mode Rejection Ratio | CMRR | $V_{DG}$ = 10 to 20 V, $I_D$ = 200 µA | 100 | | | dB |

NOTES:
a. $T_A$ = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

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